Application Report
SLVA491 – January 2012

Improved Load Current Capability for Cap-Drop Off-Line Power Supplies for E-Meter Using the TPS5401

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Power DC/DC Controllers

ABSTRACT

Standard electronic electricity meters (e-meters) have traditionally used a capacitive-drop power supply (cap-drop) plus linear regulator topology to provide a cost-effective power supply. Today, opposing forces such as an increase in load currents due to more complex AMR and AMI communications circuitry and tighter power consumption regulations, force e-meter designers to limit consumption to below 4VA (~1.2W) for single-phase or 8VA (~2.4W) for 3-phase e-meters. Employing an innovative, yet simple, solution using a switching DC/DC converter, such as the TPS5401 in place of the linear regulator allows the e-meter designer to avoid the costly move to expensive switch mode power supply (SMPS) solutions. This application note goes through the step-by-step decisions a designer must make to complete a cap-drop power supply with a DC/DC converter. A design calculator tool, SLVC392, is also available with the application note to assist the designer, when the design criteria are different than the application note.

The concept shown in this application note can also be expanded to a 3-phase application that requires more load current. Both applications have been built and tested and are available for download as PMP6960 (single phase with the TPS5401) and PMP3692 (three phase with the TPS54060).

Figure 1. Single Phase Cap Drop E-Meter Design (PMP6960) using the TPS5401

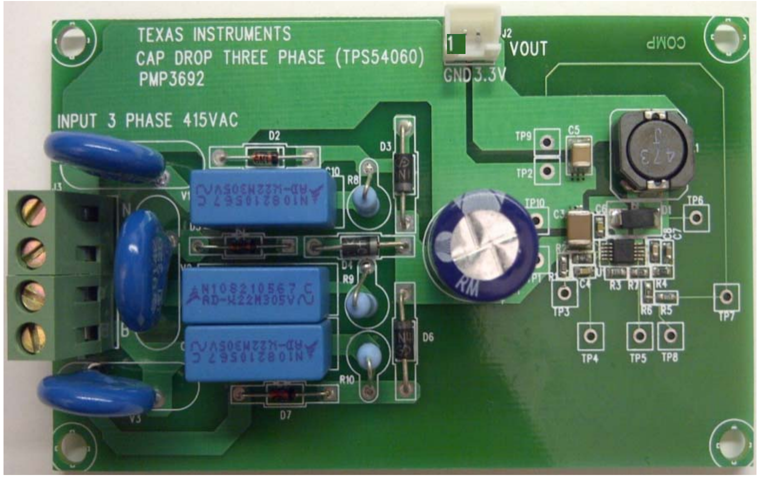

Figure 2. Three Phase Cap Drop E-Meter Design (PMP3692) using the TPS54060

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Table 1. Power Supply Requirements

Input Voltage (V_{IN})	230VAC 50Hz (nominal) – 50mA Load 80VAC 50Hz (min)– 12.5mA load 305VAC 50Hz (max)– 66.8mA load
Input Current (4VA limit)	17.4mA
Output Voltage	3.3V
Output Voltage Ripple	1%
Maximum Output Current	50mA
Switching Frequency	365kHz

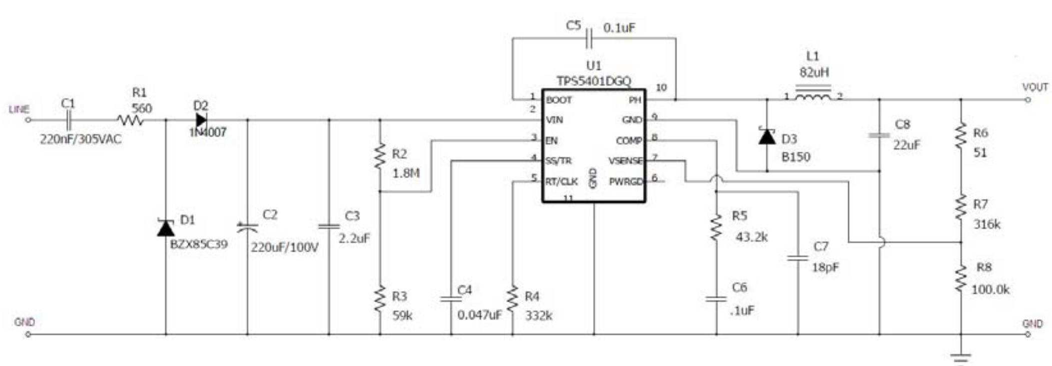

Figure 3. Schematic of Cap Drop E-Meter Design (PMP6960) using the TPS5401

Note: There was no Metal Oxide Varistor (MOV) at the input to demonstrate robust performance without any additional components.

Capacitor Drop Design

Isolation Cap Selection and Input Current Considerations

Apparent Power, described in Volt-Amperes (VA) = V_{RMS} x I_{RMS}. Under the existing restrictions, if the apparent power must be limited to 4VA with an AC line voltage (VRMS) of 230V, then I_{RMS} needs to be limited to 17.4mA. The size of the input capacitor will limit the amount of AC current into the system. Using equation (1), where V_{RMS} = 230V, f = 50Hz, and I_{RMS} = 17.4mA, then CIN must be ≤ 240nF. A standard value of 220nF is chosen for this design, with a voltage rating of 305VAC.

$$C_{IN} = \frac{I_{RMS}}{\left(V_{RMS} \times 2 \times \pi \times f\right)} \quad (1)$$

If chosen correctly, the capacitor drop and half wave rectifier will protect the circuit from line surges. (See appendix A.7)

Input Voltage

The resulting DC current through a half-wave rectifier into the voltage regulator can be calculated with equations 2-5. With VAC = 230V, C_{IN} = 220nF, Vz = 39V and D = .5, the resulting I_{DCIN} = 7mA. For a linear regulator, I_{DCOUT} = I_{DCIN}; therefore, at ~7mA max, linear regulators can be used with a cap-drop supply for only the simplest of single phase e-meters. For higher load demands, a switching DC/DC converter, such as the TPS5401, is required.

$$I_{IN\ HRMS} = \left(V_{PEAK} - Vz\right) \times \pi \times 50Hz \times C_{IN} \quad (2)$$

$$V_{IN\ RMS} = Vz \times \sqrt{D} \quad (3)$$

$$P_{IN} = I_{IN\ RMS} \times V_{IN\ RMS} \quad (4)$$

$$I_{INDC} = \frac{P_{IN}}{V_{INDC}} \quad (5)$$

When a switching DC/DC converter is used, a boost in efficiency complements the design. By predicting the efficiency and using equations 6 and 7, the power out and I_{OUT} can be found. The higher the regulator input voltage and the higher the efficiency, the larger the output current can be. In this example, the TPS5401 is chosen, with an input voltage of 42V. Other devices can be used, such as the TPS54060 or TPS54062 for higher input voltage and higher efficiency. These additional devices are supported in the calculator tool, SLVC392.

$$I_{OUTDC} = \frac{P_{OUT}}{V_{OUT}} \quad (6)$$

$$P_{OUT} = P_{IN} \times \eta \quad (7)$$

(where η = efficiency of the converter at the intended DC load current)

Using the equations 2-7 with the TPS5401 (with a V_{IN} max of 41V to account for variation in the zener diode, η ≈ 60% at desired operating point, and a desired V_{OUT} of 3.3V), we can get as much as 50mA into the load at 230VAC. This is reduced to 12.5mA at 80VAC.

The efficiency can be optimized by choosing the switching frequency, output cap and inductor, as well as minimizing losses through other components such as the output voltage setting resistors and adjustable UVLO resistors. Equations 8 and 9 will derive the UVLO resistor values. Use equation 10 to find the power dissipated through the resistors. If the Vstart and Vstop values are too low, there will not be enough current to charge the input capacitors and operate the converter at start up. In order to prevent this, set Vstart as close as possible to V_{INMIN} and Vstop to be within 20% of V_{INMIN}. For this design, Vstart = 37V and Vstop = 32V. Using equations 8 and 9 R2 = 1.7M, but a 1.8M was used and R3 = 58K, but a 59K was used.

$$R2 = \frac{Vstart - Vstop}{Ihys} \tag{8}$$

$$R3 = \frac{Vena}{\frac{Vstart - Vena}{R1} + I1} \tag{9}$$

Output Voltage and Output Current

Most loads require a single input voltage of 3.3V. Adjusting the output voltage of the TPS5401 is done easily by using equation 10 below.

$$R7 = R8 \times \frac{V_{OUT} - 0.8V}{0.8V} \tag{10}$$

For higher efficiency, larger values for R8 and R7 are desired. However, if too high of resistors are selected the converter can be vulnerable to noise. Limit the max R8 and R7 to be 775kΩ. Assume 100kΩ for R8, and R7 is calculated at 316kΩ. The output will still read 3.3V after the 4kV surge test.

Duty Cycle and Frequency Set Resistor

The switching frequency (Fsw) is adjustable over a wide range for the TPS5401. To balance efficiency and size, a switching frequency must be chosen that meets the minimum on time requirements of the converter, the short circuit protection requirements, and also results in a reasonable value for the inductor. The minimum controllable on time for the TPS5401 is typically 120ns. See the “Selecting the Switching Frequency” section of the TPS5401 datasheet for more details on the frequency shift. By choosing a Fsw of 365kHz, all conditions for meeting the current limit protections and minimum on time are met.

Inductor

To determine the inductor value, calculate the average inductor current at the minimum and maximum output currents and minimum and maximum input voltages. Assuming a 41V V_{INMAX}, 37 V_{INMIN}, 3mA I_{OMIN}, and 50mA I_{OMAX}, the minimum and maximum inductance for the application can be calculated using equations 11 and 12.

$$L_{ONMIN} = \frac{\left(V_{INMIN} - V_O\right) \times V_O}{2 \times V_{INMIN} \times f sw \times I_{OMAX}} \tag{11}$$

$$L_{ONMAX} = \frac{f sw \times \left(V_{INMAX} - V_O\right) \times V_{INMAX} \times t_{ONMIN}^2}{2 \times V_O \times I_{OMIN}} \tag{12}$$

Using a V_{INMAX} of 41V, V_{INMIN} of 37V, V_{OUT} of 3.3V, I_{OMAX} of 50mA, I_{OMIN} of 3mA, and Fsw of 365kHz, a minimum inductor value of 82.3µH and a maximum inductor value of 410µH is calculated. Choosing an inductor closest to the minimum, results in an 82µH inductor with an R_{DC} of 261Ω. Use equations 13 through 16 to verify that D1 + D2 is less than 1; otherwise, in DCM operation, and inductor is rated up and beyond IL_{RMS} and IL_{PEAK}.

$$IL_{PEAK} = \sqrt{\frac{2 \times V_O \times I_{OMAX} \times \left(V_{INMAX} - V_O\right)}{V_{INMAX} \times L_O \times f sw}} \tag{13}$$

$$D1 = \sqrt{\frac{2 \times V_O \times I_O \times L_O \times f sw}{V_{IN} \times \left(V_{IN} - V_O\right)}} \tag{14}$$

$$D2 = \left(\frac{V_{IN} - V_O}{V_O}\right) \times D1 \tag{15}$$

$$IL_{RMS} = IL_{PEAK} \times \sqrt{\frac{D1 + D2}{3}} \tag{16}$$

Output Capacitor

The output capacitance is chosen to handle the expected load step requirements of the load. Since the e-meter application is not demanding, a load step of less than 50mA can be expected. This will result in a lower capacitance than if a large load step is required, as the output cap maintains the output voltage during the load step. The C_{OUT} should be sized by meeting the most demanding of equations 17, 18, and 19.

$$C_O \geq \frac{IL_{PEAK} \times (D1 + D2)}{V_{ORIPPLE} \times f sw \times 8} \tag{17}$$

$$C_O \geq L_O \times \frac{I_O^2}{\left(V_O + \Delta V\right)^2 - V_O^2} \tag{18}$$

$$C_O \geq L_O \times \frac{I_O}{\Delta V - f co} \tag{19}$$

The most stringent of these is equation 17, which results in a requirement of 1.04µF. The capacitor standard size is chosen to be 22µF. Keep in mind that ceramic capacitors have a reduction in capacitance based on the bias of the output voltage, so using a larger value than calculated is advised. The output capacitor also provides the pole for the Type II compensation, so to accurately predict the crossover; it is required to de-rate the output capacitance based on the output voltage and capacitor voltage rating.

Diode Selection

The diode must have a reverse voltage rating equal to or greater than V_{INMAX}. The peak current rating of the diode must be greater than the maximum inductor current. The diode should also have a low forward voltage. For this design example, the B150-E3 Schottky diode with 50V reverse voltage is selected for its lower forward voltage of 0.75V.

Compensation and Frequency Response

To stabilize the closed-loop circuit, a compensation network is required. Because the TPS5401 is a current mode converter, the compensation can be Type IIA, which consists of a resistor and capacitor in parallel with another capacitor on the COMP pin.

The first step is to determine the Kdcm, DCM gain, and the Fm, modulator gain. These can be calculated using equations 20 and 21.

$$Kdcm = \frac{2 \times V_{OUT} \times \left(V_{IN} - V_{OUT}\right)}{D1 \times V_{IN} \times \left(2 + \frac{Rdc \times I_{OUT}}{V_{OUT}}\right) - V_{OUT}} \tag{20}$$

$$Fm = \frac{gmps}{\left[\frac{V_{IN} - V_O}{L_O \times f\,sw}\right] + .805} \tag{21}$$

Since, gmps = 1.9 and R_{DC} (DCR of L_O) = .261Ω, Kdcm = 37.37 and Fm = .951.

Next, determine the power stage pole and zero frequencies. These can be calculated using equations 22 and 23.

$$f\,pmod = \frac{I_{OMAX}}{2 \times \pi \times V_{OUT} \times C_{OUT}} \times \frac{\left(2 - \frac{V_{OUT}}{V_{IN}}\right)}{\left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \tag{22}$$

$$f\,zmod = \frac{1}{2 \times \pi \times Resr \times C_{OUT}} \tag{23}$$

For C_{OUT}, the derated value of 18.3µF is used. In this case, f_{Pmod} = 276Hz, and f_{Zmod} = 2.91MHz. Then, determine the geometric mean of the modulator pole and the ESR zero (equation 24), and the mean of the modulator pole and the switching frequency (equation 25).

$$f_{co} = \sqrt{f_{pmod} \times f_{zmod}} \tag{24}$$

$$f_{co2} = \sqrt{f_{sw} \times f_{pmod}} \tag{25}$$

In this case, f_{co1} = 28.3 kHz, and f_{co2} = 10 kHz. Choose the smaller of the two as a starting point for the crossover frequency. The target crossover frequency chosen is 10 kHz.

Finally, calculate the compensation pole (resistor), use equation 26. To calculate the compensation zero (capacitor), use equation 27.

$$R5 = \frac{f_{co2} \times V_{OUT}}{Kdcm \times Fm \times f_{pmod} \times gema \times V_{REF}} \tag{26}$$

$$C6 = \frac{1}{2 \times \pi \times R5 \times Kdcm \times Fm} \tag{27}$$

In this case, R5 = 43.3kΩ, and C6 = .1µF. The nearest standard values for R5 and C6 are 43.2kΩ and .1µF, so these are used. Using equations 28 and 29, the Cpole or C7 in this circuit, may be calculated. Use the larger of the two calculated values.

$$Cpole1 = \frac{C_{OUT} \times Resr}{R5} \tag{28}$$

$$Cpole2 = \frac{1}{R5 \times f_{sw} \times \pi} \tag{29}$$

In this case, the calculated values are 1.27pF and 20.2pF. In this case, a standard value of 18pF was chosen. The resulting bode plot is shown in the results section of the application note.

Input Capacitors

The TPS5401 requires a high quality ceramic, type X5R or X7R, input decoupling capacitor of at least 3µF, and in some cases a bulk capacitance. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the TPS5401, which can be calculated using equation 30.

$$IC_{RMS} = IL_{PEAK} \sqrt{\left(\frac{D1}{3} - \left(\frac{D1}{4}\right)^2\right)} \tag{30}$$

In this case, two 2.2µF/50V capacitors in parallel are selected. These capacitors must be placed as close as possible to the input pin of the switching power device.

Slow Start Time

The slow start capacitor determines the minimum amount of time it will take for the output voltage to reach its nominal programmed value during power up. The slow start time must be long enough to allow the regulator to charge the output capacitor up to the output voltage without drawing excessive current. Equation 31 can be used to find the minimum slow start time, tss, necessary to charge the output capacitor, C_{OUT}, from 10% to 90% of the output voltage with an average slow start current Issavg. In the example, to charge the 22μF output capacitor up to 3.3V while only allowing the average input current to be 5mA would require at least 11.6ms slow start time.

$$tss > \frac{C_{OUT} \times V_{OUT} \times 0.8}{I_{SSavg}} \tag{31}$$

Once the slow start time is known, the slow start capacitor value can be found with equation 32.

$$Css(nF) = \frac{tss(ms) \times I_{SS}(\mu A)}{V_{REF}(V) \times 0.8} \tag{32}$$

In this case, to achieve a 12 ms minimum slow start time, Iss of 2μA, and V_{REF} of 0.8V, a 0.047 μF capacitor is chosen.

Power Dissipation

In order to measure power dissipation from the AC line, a power meter must be used. Measure the real power in as PinM. The P_D, total power dissipation, is calculated in equation 33.

$$P_D = real(PinM) - I_{OUT} \times V_{OUT} \tag{33}$$

At I_{OUT} = 40mA, V_{OUT} = 3.291, and measured real Pin = 454.4mW, PD = 322.8mW. For a theoretical power dissipation calculation, equations 34 – 47 will provide a rough estimate.

$$PDcal = Pfet + Pd1 = Pdriver + Pcontroller + Puvlo + Pd2 \text{ and } 3 + Prin + Pcap + Pind \tag{34}$$

FET

$$1fet = \sqrt{D1 \times \left(I_{OUT}^2 + \frac{IL_{PEAK}^2}{12} \right)} \tag{35}$$

$$Pfet_{cond} = Ifet^2 \times R_{DS(on)} \tag{36}$$

$$Pfet_{sw} = \frac{1}{4} \times fsw \times switch_{time} \times V_{INMAX} \times \left(I_{OUT} + \frac{IL_{PEAK}}{2} \right) \tag{37}$$

$$Pfet = Pfet_{sw} + Pfet_{cond} \tag{38}$$

Assuming I_{OUT} = 40mA, $R_{DS(on)}$ = .2Ω, Ipeak and D1 equal values calculated before, $I\mathit{f}et$ = 14.3mA and $P\mathit{f}et_{cond}$ = 41.1μW. With fsw = 365kHz, switch_time = 10ns, V_{INMAX} = 41V, $P\mathit{f}et_{sw}$ is calculated to be 3.37mW and the resultant $P\mathit{f}et$ totals to be 3.41mW.

Internal IC

$$\text{Pdriver} = \mathit{f}\text{sw} \times \text{Vdrive} \times \text{Qgfet} \tag{39}$$

$$\text{Pcontroller} = I_{non\text{-}sw} \times V_{IN} \tag{40}$$

Assuming Vdrive = 6V, Qgfet = 15nC, and $I_{non\text{-}sw}$ = 116μA, Pdriver = 32.85mW and Pcontroller = 4.5mW.

Pre-Converter

$$\text{Pd1 and 2} = P_{IN} - \frac{V_{OUT} \times I_{OUT}}{\eta} \tag{41}$$

Since, V_{OUT} = 3.3V and I_{OUT} = 40mA we can assume for this analysis, $\eta \approx$ 57%. Using the value calculated earlier in this application note for Pin, 272.8mW, Pd2 and 3 = 32.8mW. Power dissipation in input resistance and cap drop should be done using the RMS current. RMS current will be approximately full wave rectifier current, given in equation 33.

$$I_{IN\ frms} = V_{RMS} \times 2 \times \pi \times 50\text{Hz} \times \text{Cap} \tag{42}$$

$$\text{Prin} = I_{IN\ frms}{}^{2} \times \text{Rin} \tag{43}$$

$$\text{Pcap} = I_{IN\ frms}{}^{2} \times \text{Rcap} \tag{44}$$

$I_{IN\ frms}$ calculates to 15.9mA so, the 560Ω resistor will dissipate 141.57mW of power. Estimating Rcap ~50Ω, results is Pcap dissipation of 12.64mW.

Low Side Catch Diode and Inductor

During the converter on time, the output current is provided by the internal switching FET. During the off time, the output current flows through the catch diode. The average power in the diode is given by equation 20.

$$\text{Pd3} = \sqrt{= \frac{2 \times I_O \times L_O \times \mathit{f}\text{sw}}{V_{IN}{}^2 \times V_O - V_O{}^2 \times V_{IN}}} \left(V_{INMAX} - V_{OUT}\right) \times I_{OUT} \times V\mathit{f}\text{d} + \frac{\text{Cj} \times \mathit{f}\text{sw} \times \left(V_{IN} + V\mathit{f}\text{d}\right)^2}{2} \tag{45}$$

The selected diode will dissipate 69.1mW assuming a 40mA output current, diode junction capacitance of 150pF, $V\mathit{f}d$ of 0.75V, Fsw of 365kHz and V_{INMAX} of 41V. Power dissipated through the inductor is calculated below in equation 46.

$$P_{IND} = I_{OUT}{}^{2} \times R_{DC} + I_{NDcorelosses} \tag{46}$$

Inductor core loses were calculated from the manufacturer to be about 8mW bring the total power dissipated through the inductor to ~9mW.

Input of Converter

The UVLO resistors are the only components on the converter's input dissipating enough power to consider in this analysis. The power dissipated through the UVLO resistors is calculated using equation 10.

$$P_{UVLO} = \frac{V_{IN}^{2}}{R2 + R3} \tag{47}$$

Calculated power dissipated totals to a value of 306.1 mW.

Appendix A. Experimental Results

All results are to be assumed at 3.3V output, 40mA load, and 230VAC input unless specified otherwise.

A.1 Efficiency

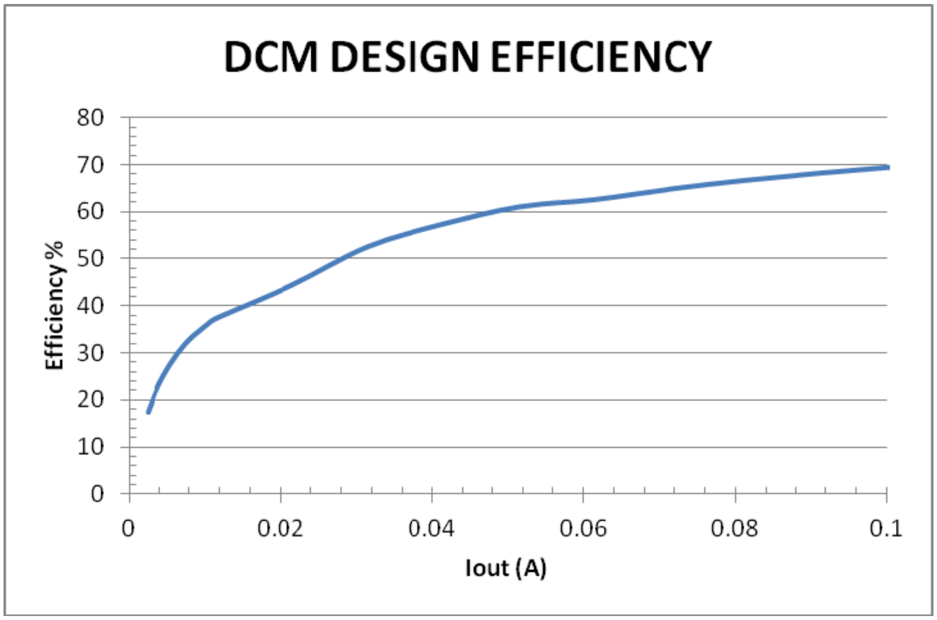

Figure A-1. DCM Design Efficiency

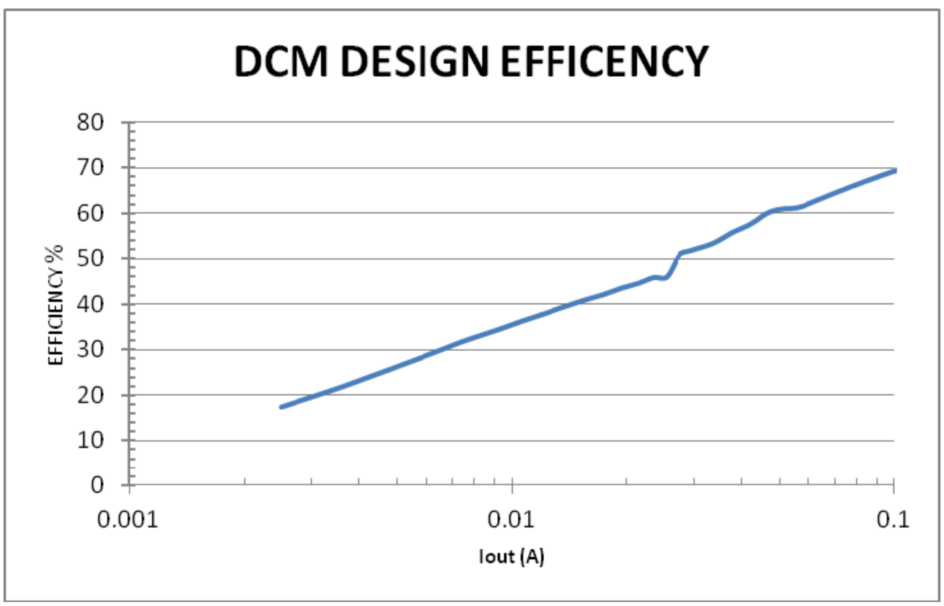

Figure A-2. Logarithmic DCM Design Efficiency

A.2 Control Loop

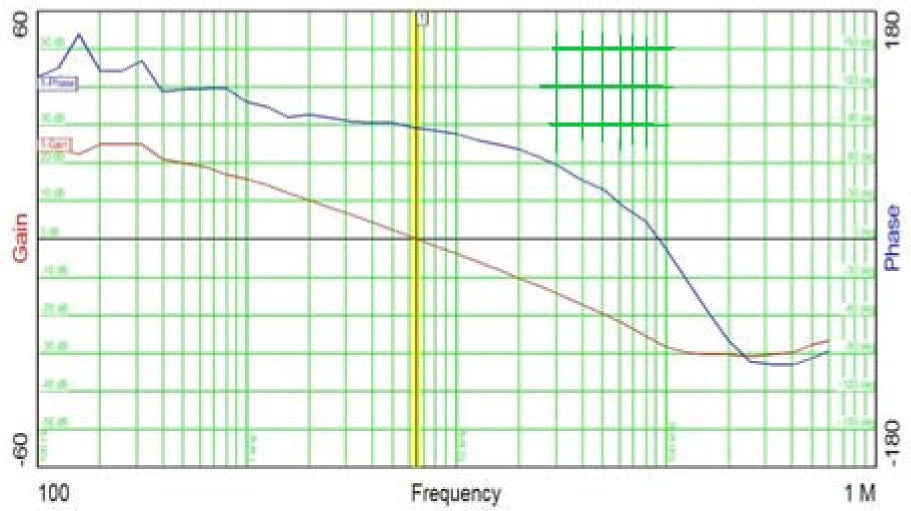

Figure A-3. Frequency Response at 40mA Load

The de-rated value of the capacitor was smaller than the value used by 3.5µF. However, it is doubtful that this would cause the variation of the graph between theoretical and actual data. The target crossover frequency is also smaller. The graph shows 6.5kHz, when 10kHz was the target. Most of the variation between the actual and theoretical data is due to the fact that when a simulated graph is produced it has ideal conditions and when the data is actually found in the lab, it can have some variation.

V_{OUT} Regulation

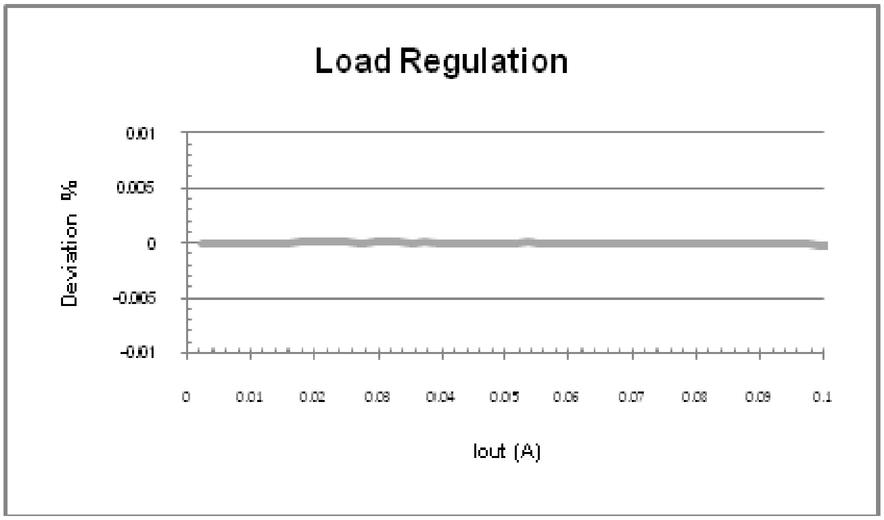

Figure A-4. Load Regulation at 3.3V$_{OUT}$.

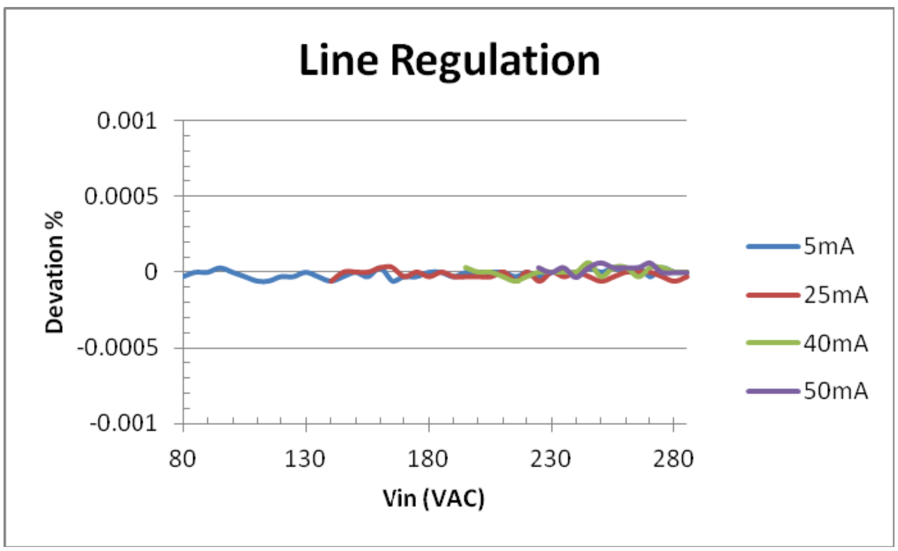

Figure A-5. Line Regulation at 3.3V$_{OUT}$.

A.3 V_{IN} Ripple

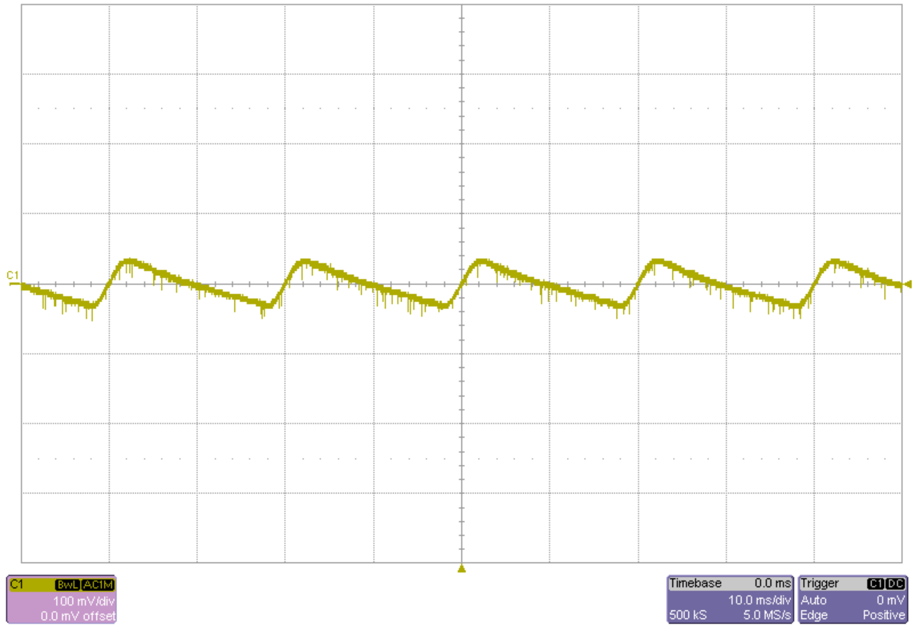

Figure A-6. V_{IN} Ripple at 5mA Load

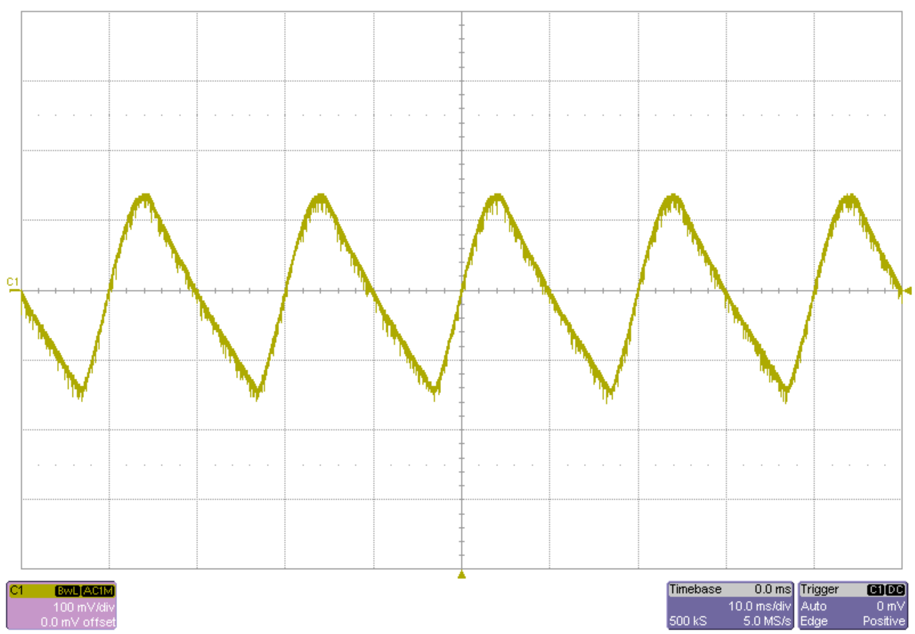

Figure A-7. V_{IN} Ripple at 40mA Load

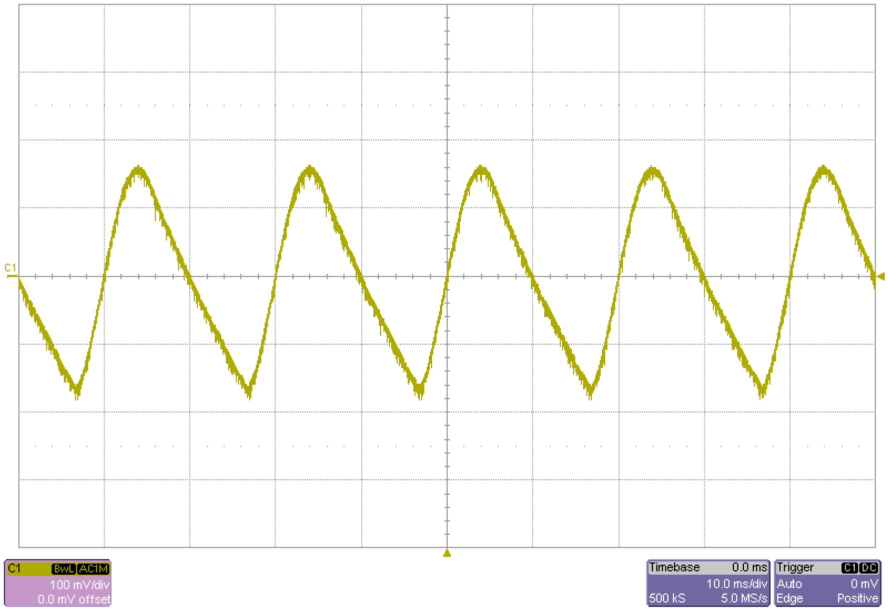

Figure A-8. V_{IN} Ripple at 50mA Load

A.4 V_{OUT} Ripple

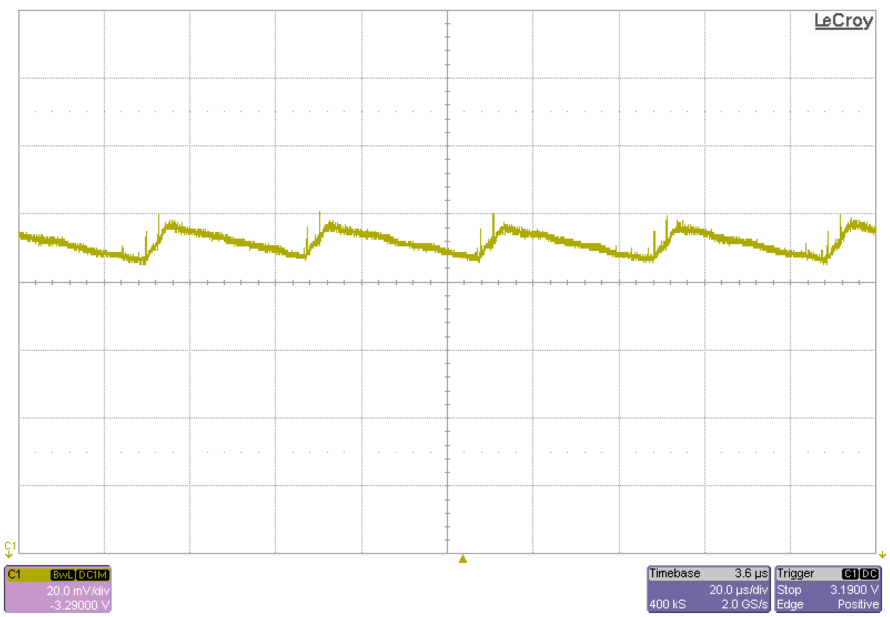

Figure A-9. V_{OUT} Ripple at 5mA

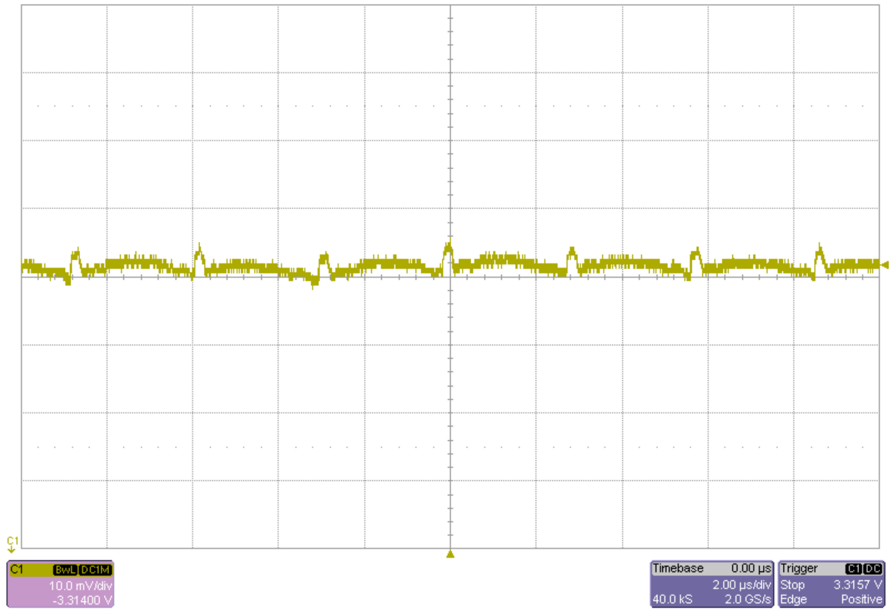

Figure A-10. V_{OUT} Ripple at 40mA

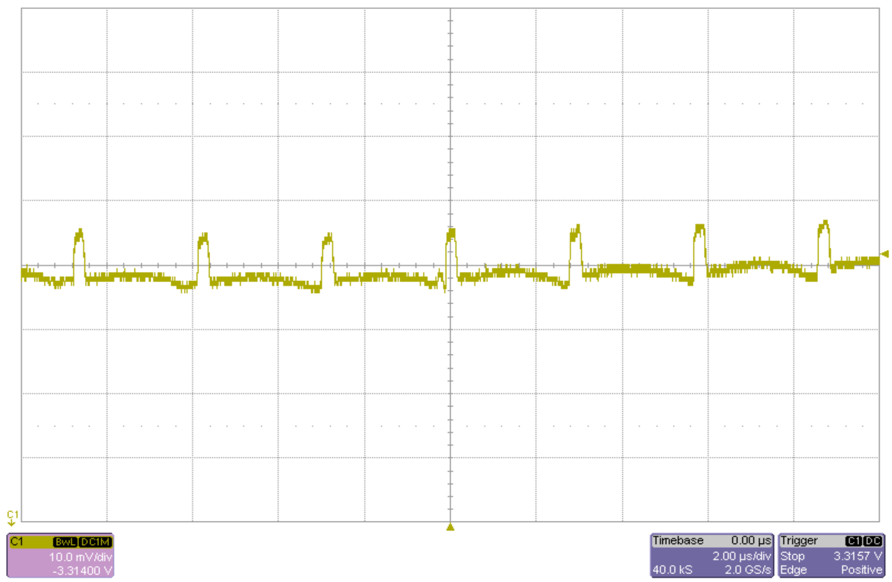

Figure A-11. V_{OUT} Ripple at 50mA

A.5 Slow-Start

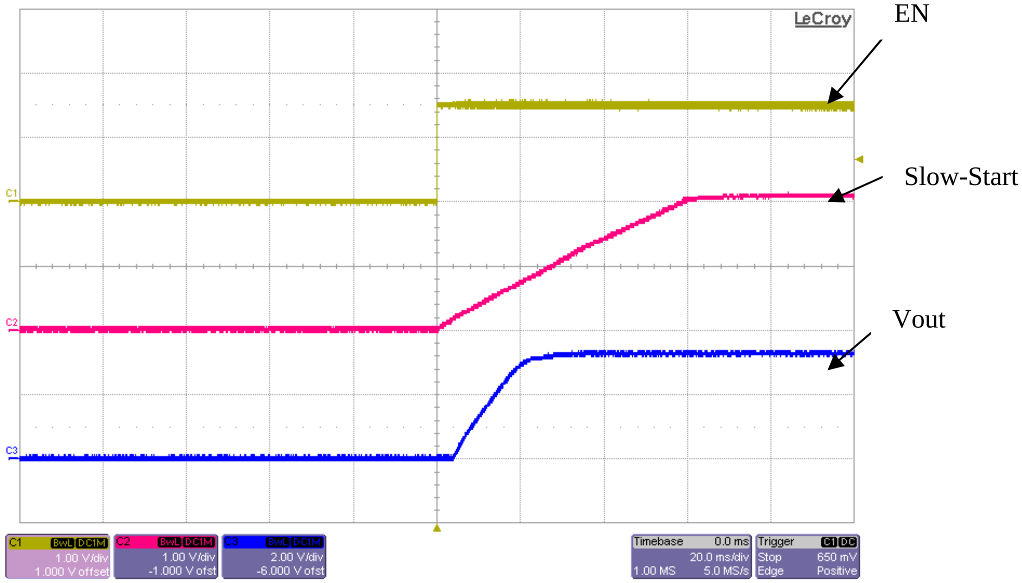

Figure A-12. Slow-Start vs. EN

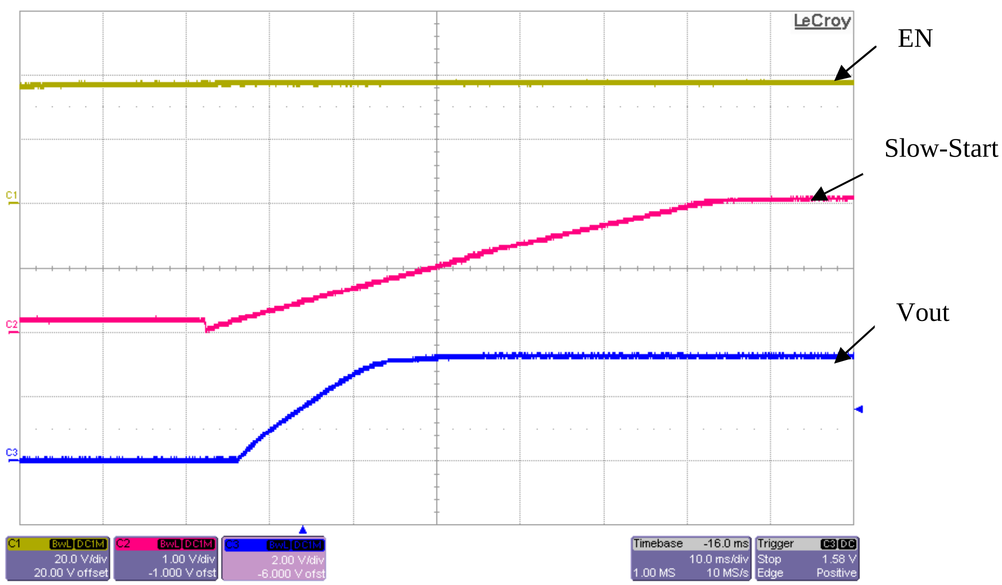

Figure A-13. Slow-Start vs. V_{IN}

A.6 Surge Test

The reference circuit was tested for line surges using the 4kV IEC-61000-4-5 standard and it passed. All functions work properly after testing. Also note that there was no Metal Oxide Varistor (MOV) at the input.

IMPORTANT NOTICE