Texas Instruments

Application Report
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USB Power Switch Reverse Current Protection

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ABSTRACT

With the proliferation of PC based devices furnishing power over USB ports, the odds of one device reverse powering a second device is increasing. How can reverse current flow from one USB powering device into another be prevented? This application report outlines a method of blocking the reverse current that can occur when a USB cable with two Type A connectors, is used to connect two devices capable of sourcing power.

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1 Introduction

The proposed circuit utilizes the INA202 current shunt monitor to sense reverse current on +5USB, latch the fault, and disable the USB power switch. This disconnects the host power supply from the external source until the current shunt monitor unlatches. The latching scheme can be chosen by altering the connection made with the $\overline{RST}$ pin.

Schematic, test results, formula used to set the current trip, and different methods of latching the enable pin of the USB power switch are provided. The proposed circuit is demonstrated using the TPS2552DBV1EVM-364, but works with any USB power switch with active low enable, including the TPS2552. Figure 1 shows the circuit schematic diagram.

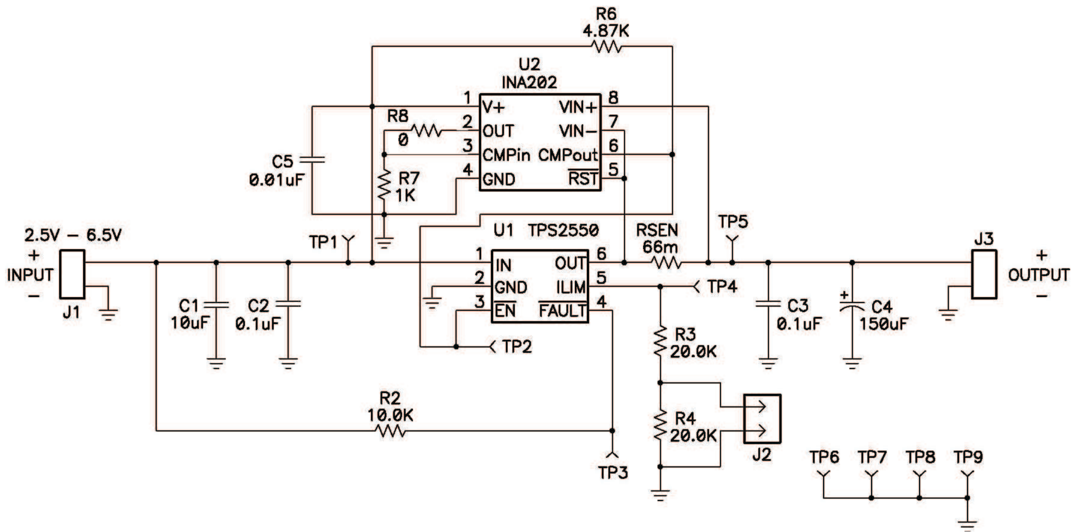

Figure 1. USB Power Switch Schematic with Reverse Current Protection

2 Initial Considerations

2.1 *Circuit Components*

The circuit components needed for this application are INA202 or similar device (INA200 or INA201), four resistors (RSEN, R6, R7, and R8), and a filter capacitor (C5). The INA20X is a family of current shunt monitors with different internal gains and built in fixed reference voltage comparators. Resistor RSEN is a resistor placed in series with the +5USB line used to sample current. Resistor R6 is a pull up resistor for the output of the comparator. The output of the comparator is used to control the enable pin on the USB power switch. Resistors R7 and R8 can be used as a resistive voltage divider to reduce the voltage entering the CMPin pin.

2.2 *Choosing Component Values from a Reverse Current Threshold*

To help choose the current shunt monitor gain, the expected maximum forward load current must be known. The largest acceptable forward voltage drop at maximum loading must also be determined. Once these two system variables are determined, circuit component values can be calculated.

NOTE: The application provided works when it is acceptable to have at least a 6 mV drop across the sense resistor when reverse current limit occurs. This is set by the internal voltage reference for the comparator of 0.6 volts. Another consideration is that when the forward load current is an order of magnitude larger than the reverse trip point, then the corresponding forward voltage drop is proportionally larger.

When a reverse voltage drop in excess of 6 mV is allowable then different members of the INA20x current shunt monitors can then be considered which have smaller built in gains. The INA20x current shunt monitor family consists of three fixed internal gain amplifiers as shown in Table 1. All three have the same internal comparator reference voltage.

Table 1. Current Monitor Internal Gains

Current Monitor	Gain (V/V)
INA200	20
INA201	50
INA202	100

For cases where efficiency is a large concern the INA202 is the best solution and for this reason testing was performed using this current shunt monitor. To choose the value of the sense resistor the threshold for reverse current needs to be chosen. Once the value has been chosen the calculation for the sense resistor can be made.

$$R_{SEN} = \frac{0.6}{Gain \times I_{THRESH}} \tag{1}$$

If using the INA202, the equation simplifies to:

$$R_{SEN} = \frac{0.006}{I_{THRESH}} \tag{2}$$

In cases with larger current thresholds and corresponding larger voltage drop across RSEN occurs, a resistive network consisting of R7 and R8 can be used to reduce the voltage that is fed into the comparator. If using the resistive network, Equation 3 can be used to calculate the value of RSEN.

$$R_{SEN} = \frac{0.6 \times (R_7 + R_8)}{(I_{Trip}) \times Gain \times R_7} \tag{3}$$

For the purpose of testing, R8 was chosen to be 0 Ω (a short), R7 1kΩ, and I_{Trip} 90 milliamps. With these values the sense resistor calculation is shown in Equation 4.

$$R_{SENSE} = \frac{0.6 \times (1000 + 0)}{(0.090) \times 100 \times 1000} = 0.066\ \Omega \tag{4}$$

NOTE: If efficiency is a large concern then resistor R8 should always be 0 Ω and the INA202 current shunt monitor should be used. These enable the smallest possible voltage drop on the +5USB line.

The maximum allowable voltage on the CMPin pin is GND – 0.3 to (V+) + 0.3.

2.3 Latching the Current Trip

Through the use of the $\overline{RST}$ pin the fault can either be latched until power is cycled, latched until the output voltage drops to the lower limit of the $\overline{RST}$ pin (1.1 V), or can auto retry.

If the $\overline{RST}$ pin is tied to V+, the circuit remains latched until power to the board is cycled. This only occurs if the +5USB line that feeds into the input of the USB power switch drops below 1.1 volts.

When the $\overline{RST}$ pin is tied to ground the board is set to auto retry. A problem that can arise with auto retry is that the circuit can start to oscillate on and off. If the voltage at the output is high enough to cause the reverse current threshold to occur, the circuit trips, turning off the USB power switch. This causes current to immediately stop flowing. As soon as the current stops the voltage across the current sense resistor stops and the circuit turns back on, regardless of whether the output voltage is still present. Upon turning the USB power switch back on, reverse current returns until the circuit trips again. This occurs repeatedly if the voltage on the output remains high.

For the circuit to remain latched only until the output voltage drops below 1.1 volts, the $\overline{RST}$ pin can be tied to the output voltage of the USB power switch. Therefore when the circuit trips and latches, it remains latched until the voltage on the output subsides to less than 1.1 volts. When this occurs the circuit unlatches and the USB power switch turns back on, upon turning back on from the fault there is no longer the threat of reverse current present. For the testing of this application the $\overline{RST}$ pin is tied to the output voltage of the power switch.

3 Laboratory Performance

3.1 Overall Response to a Fault

Figure 2 shows the circuit responded to a reverse current that reached the threshold. The circuit first senses the reverse current (IOUT) reaching the threshold of 0.090 amps in the reverse direction (–). Once this occurs the enable (EN) gets asserted, and the current turns to zero. The enable remains high and the circuit remains off until the voltage at the output (VOUT) drops below 1.1 volts. When the output voltage drops below 1.1 volts, the enable drops and the circuit is turned back on.

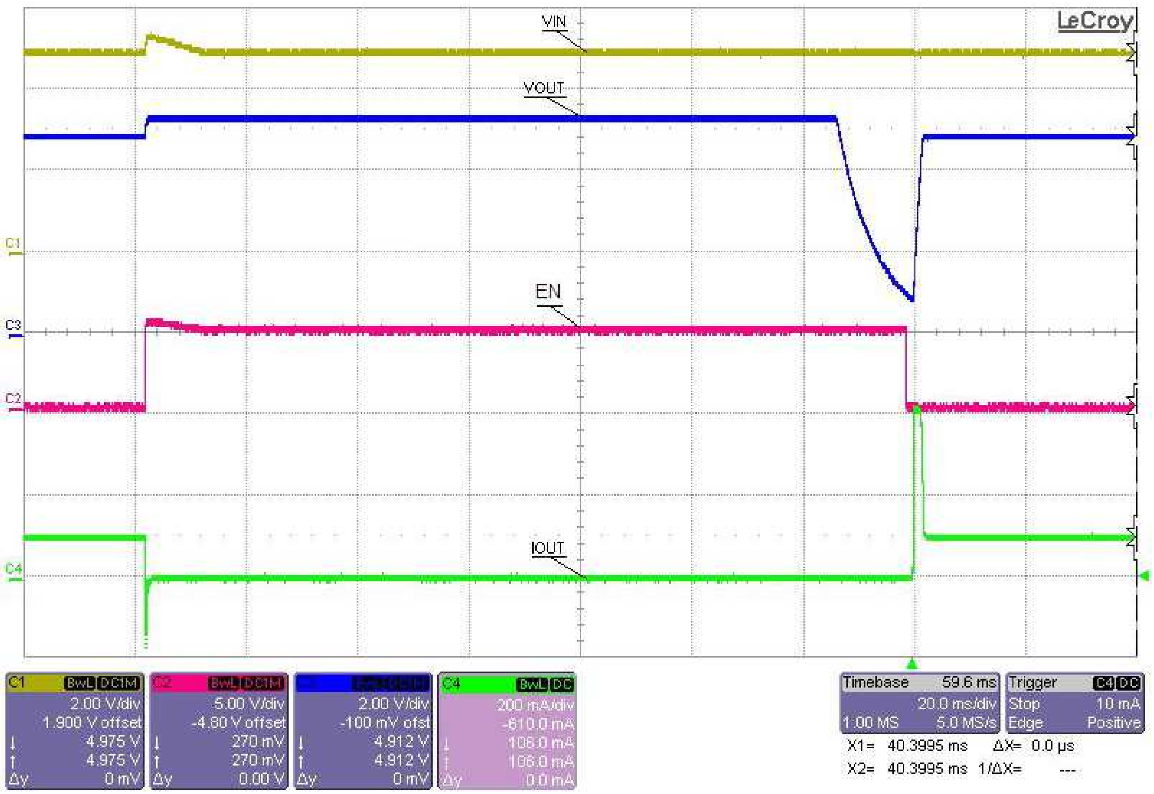

Figure 2. Responding to Reverse Current

NOTE: Some voltage feed through occurs which can be seen on the input voltage trace (VIN). When the output voltage increases and the reverse current occurs, the input voltage increases as well until the power switch is disabled and the voltage dissipates.

3.2 Responding to a Fault

Figure 3 shows the circuit responding to a fault, latching, and voltage feed through that occurs in more detail. It can be seen that the input voltage (pink trace) returns to its original value after about 11.25 ms, and at this point the current has already returned to zero amps (green trace).

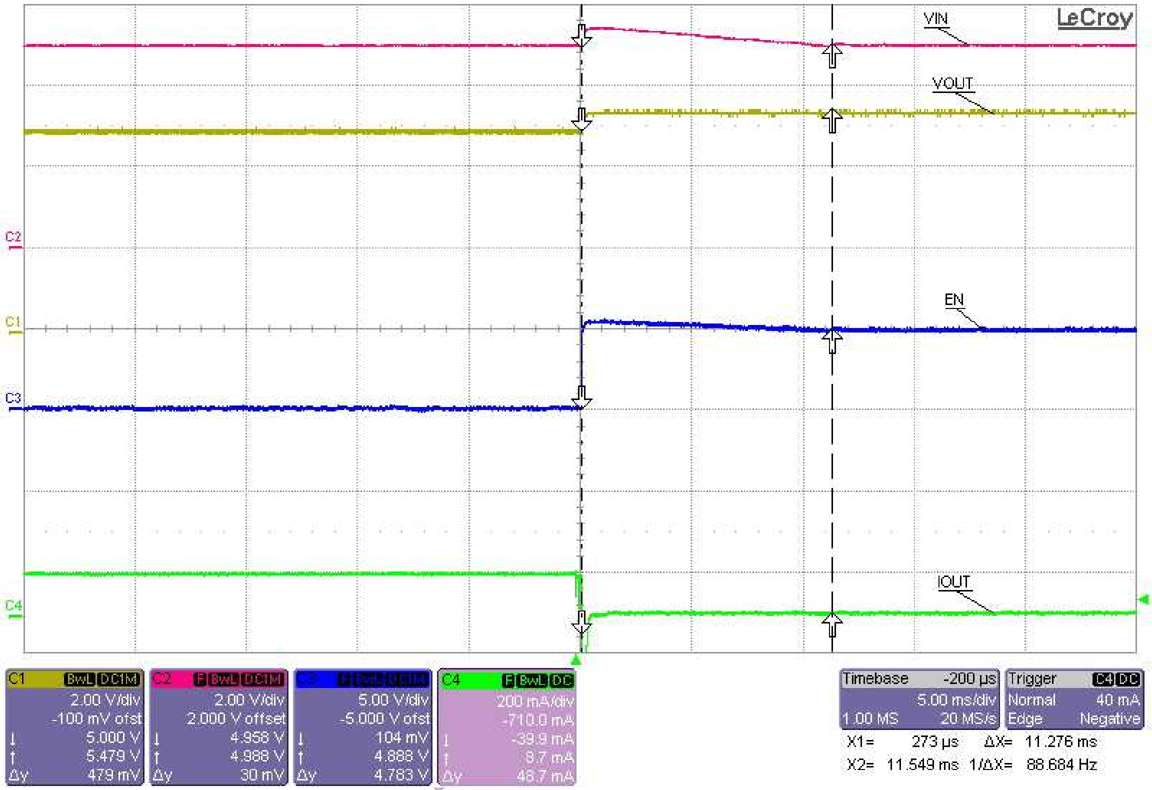

Figure 3. Responding to a Fault

The cursors in Figure 4 show the amount of time it takes for the circuit's output current to return zero amps from the time the fault is triggered.

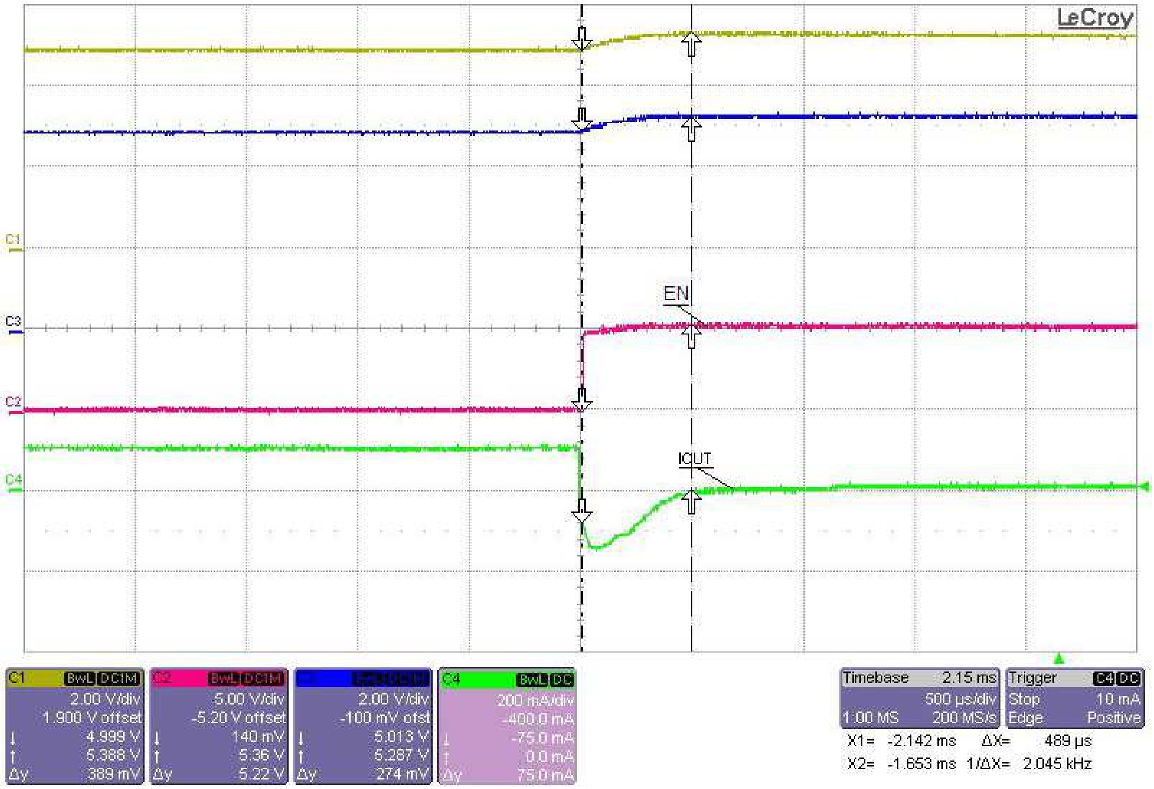

Figure 4. Time Between Fault and Zero Current

Figure 4 shows a close up on the fault being latched showing that it takes the circuit 489 μs to return to zero amps once the fault has been latched.

3.3 Returning from a Fault

Figure 5 starts with the circuit latched from a fault, then unlatching when the output voltage (VOUT) drops lower than 1.1 volts. Once this occurs the enable drops first and then the USB power switch turns back on to allow current to flow in the forward direction.

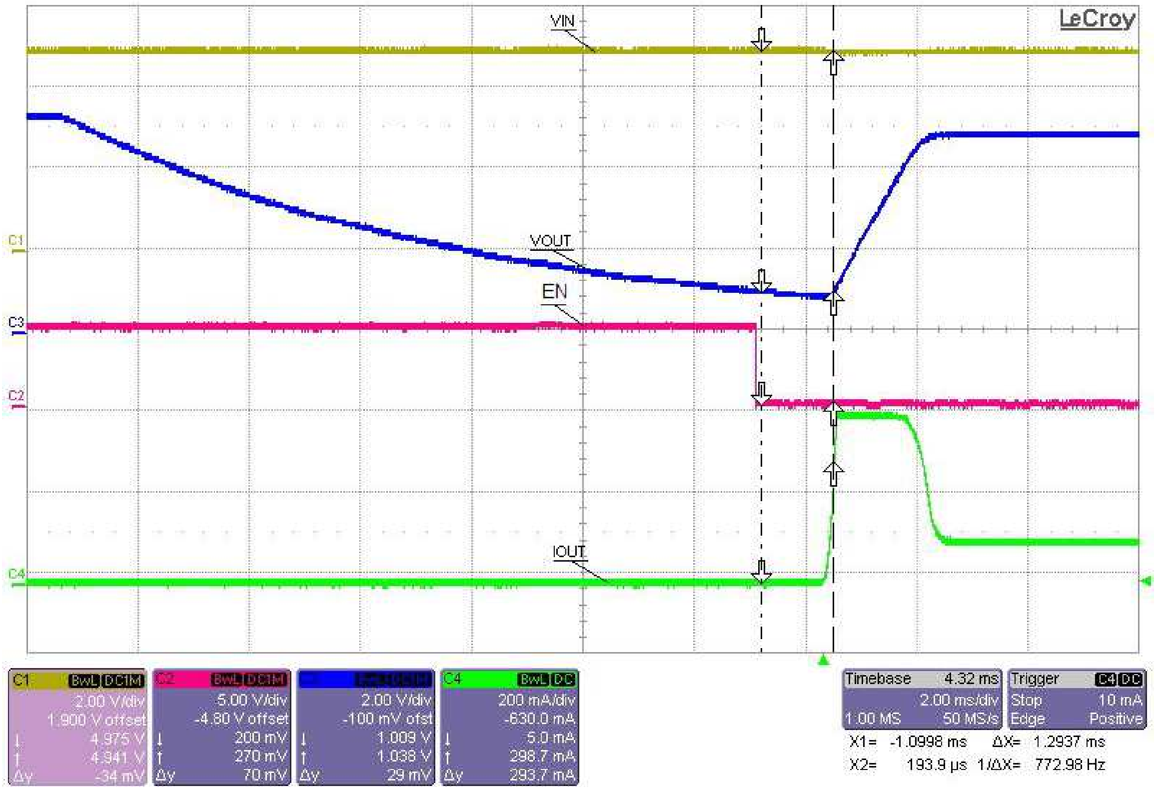

Figure 5. Unlatching When Output Decays

Figure 5 shows that once the output voltage (VOUT) drops below 1.1 volts the enable (EN) is disserted. The measurement was then made showing that it took 1.3 ms for the USB power switch to turn on and allow current to begin flowing in the forward direction.

4 Final Considerations

Depending on the ability to deal with a forward voltage drop on the +5USB line, a larger resistor can be used. In the example circuit shown in this application if there was a two amp load current there would be a 0.132 volt drop across the sense resistor.