Application Report
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TPD12S015 PCB Layout Guidelines

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ABSTRACT

The TPD12S015 is a multifunction ESD protection device targeting portable HDMI (High Definition Multimedia Interface) applications. This application note focuses on layout guidelines for using the TPD12S015 DSBGA (Die Sized Ball Grid Array) 28 ball package mapped to HDMI C-type and D-type connectors. This solution is geared toward the smallest possible board area. To meet that goal, the TPD12S015 provides integrated level shifter capabilities from 1.1V – 3.6V (V_{CCA} range) to 5V. Additionally, the device is capable of generating 5V from a 2.3V-5V battery using internal boost converter circuitry.

To provide guidance in layout, HDMI signals are explained and detailed. Best practices for preserving signal integrity are given for layout of high speed HDMI lines when using this space saving 0.4mm pitch packaging. Additionally, layout guidelines are given for positioning discrete components DC/DC step-up converter circuitry. An example layout from the TI TPD12S015 EVM is also detailed.

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1 Introduction

The TPD12S015 is a multiple function HDMI ESD protection device. There are several advantages to using this multifunction integrated device.

Key features and benefits of the TPD12S015:

- Internal boost converter generates 5V from a 2.3V – 5.5V battery voltage, which eliminates the need for an on-board 5V supply to drive the HDMI 5VOUT pin.
- Matched HDMI Class C and D pin-mapping eliminates board design layout skew.
- Directionless level shifter with integrated pull-ups and a one-shot circuit (drives at least 750pF load) eliminates the need for additional on board I^2C cable driver circuit.

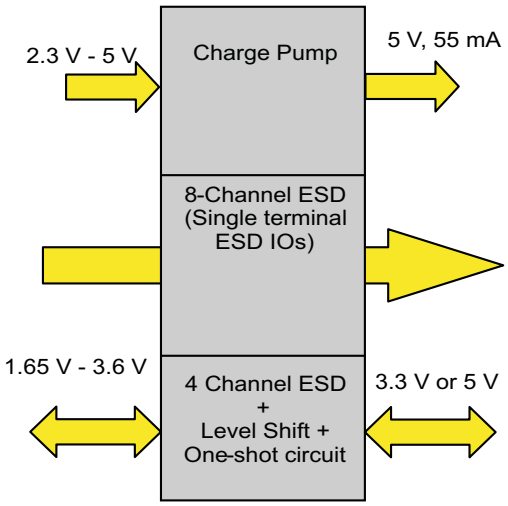

Figure 1. Device Switching Levels

The integrated ESD clamps and resistors provide good matching between each differential signal pair to provide an advantage over discrete ESD clamp solutions, where variations between ESD clamps degrade the differential signal quality. The TPD12S015 allows HDMI 1.3 data rates and provides IEC61000-4-2 (Level 4) ESD protection.

2 Signal Types and Guidelines

In this section the signals are grouped as follows:

High-speed TMDS signals, DDC/CEC I^2C signals, HPD, the control lines, which include the DC/DC enable and the level shifter enable, and power and DC/DC converter pins are detailed.

2.1 TMDS

There are four sets of high-speed TMDS (Transition Minimized Differential Signaling) lines. These consist a range of three data lines D0, D1 and D2 and the clock, CLK lines. In HDMI 1.3 these lines can reach speeds in the 340MHz. The relatively high frequency of these signals makes routing of the lines critical.

There a several things to keep in mind when dealing with high speed lines in PCB design.

- The number of vias and stubs should be kept to a minimum.
- Trace lengths should also be kept to a minimum.
- Special care needs to be made to match length in all these lines. Any significant difference in the trace lengths will introduce skew, which could violate the HDMI specification.

The high speed lines can be routed differentially or separately. If the lines are going to be in a noisy environment, it may be beneficial to route them differentially. The 50Ω trace impedance should be used if they are routed separately. The 100Ω matched impedance is recommended if routed differentially.

2.2 DDC/CEC

The display data channel lines (DDC) are made up of SDA, SCL and CEC. These lines are bi-directional I^2C communication lines between the transmitter and receiver. There are internal 10kΩ pull-ups on the A side of the TPD12S015 and 1.75kΩ pull-up resistors on the B side for the SDA and SCL lines. The CEC line has an internal 26kΩ resistor on the B side and a 10kΩ resistor on the A side. External pull up resistors are not required on the B side lines and should NOT be used on the A side due to adverse affects on the device switching thresholds.

These are low speed signal lines, typically only reaching around 400 kHz. Less care is needed in routing these lines; vias and longer trace lengths can be used with minimal risk of signal distortion.

2.3 HPD

The hot plug detect (HPD) signal is a single direction signal sent from HDMI receiver to HDMI transmitter. This signal indicates to a transmitter that there is a receiver device connected on the line. When a receiver is connected to the transmitter, the line is driven to 5V indicating a device is connected. This signal is internally translated by the TPD12S015 to the A-side voltage of the transmitter. This line is not sensitive or high speed. It's routing can be irregular and will not be negatively impacted by longer trace lengths or vias.

2.4 Control Lines

The TPD12S015 has two control pins, which enable and disable internal device circuitry. These two pins are LS_OE (level-shifter enable) and CT_CP_HPD (DC/DC converter and HPD output enable.) These are referenced to V_{CCA}. The pins have internal 470kΩ pull-down resistors. These internal resistors ensure that, when left floating externally, the pins are pulled down. This eliminates unwanted current consumption that can result from floating CMOS logic.

2.5 DC/DC Pins – VCC VBAT SW PGND

Layout of the DC/DC circuitry is detailed in the *DC/DC Circuitry* section of this guide; however, the following is a quick description of the corresponding pins. PGND should be connected to the board ground. VBAT can range from 2.3V to 5V. 5VOUT will track any voltage above 5V at the VBAT pin. VCCA can range from 1.1V to 3.6V. SW is the inductor input for the DC/DC inverter.

3 Example Layout

An EVM (evaluation module) was created using the TPD12S015. This six layer board is shown below. In actual implementation, shorter trace lengths should be used and the device should be placed as close to the external connector as possible to provide optimum performance, both in terms of signal integrity and ESD protection.

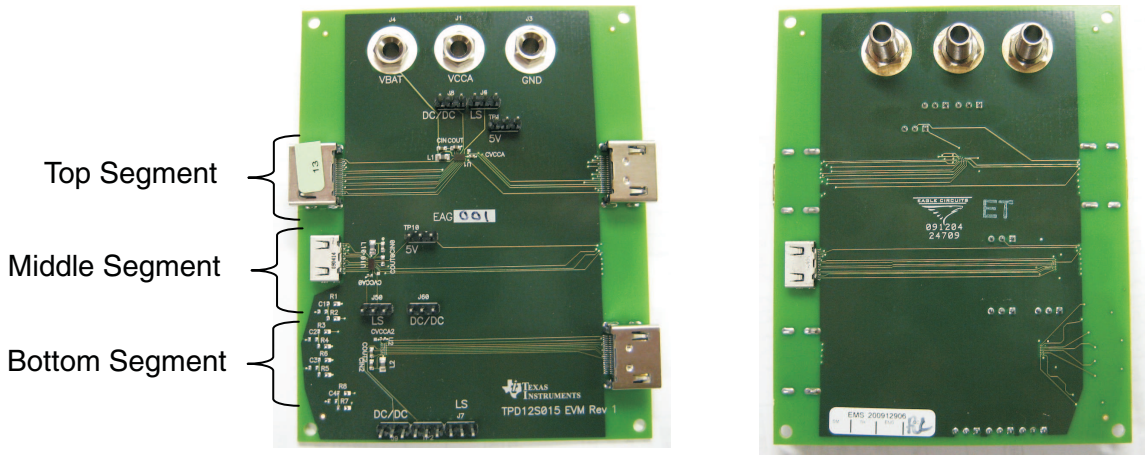

Figure 2. TPD12S015EVM

Table 1. Board Stackup

BOARD LAYER	DESCRIPTION
Layer 1	High-speed signal layer
Layer 2	Ground plane
Layer 3	Control signal layer
Layer 4	Control signal layer
Layer 5	Power plane
Layer 6	High-speed signal layer

It is important to work closely with your board manufacturer to determine what their capabilities are and understand their recommendations for 0.4mm pitch layout. This is discussed further in the section titled *DSBGA Package and Board Manufacture*.

As is shown in Figure 2, the EVM has three sections. The top segment of the layout uses HDMI-A type connectors. The middle board segment has 2 HDMI-C type connectors. The bottom configuration was designed for eye-pattern testing. This third board segment includes an HDMI-A type connector on one side and high speed traces fanned out for probe testing and loading on the other. The results of this eye pattern testing are shown in Figure 6 and Figure 7.

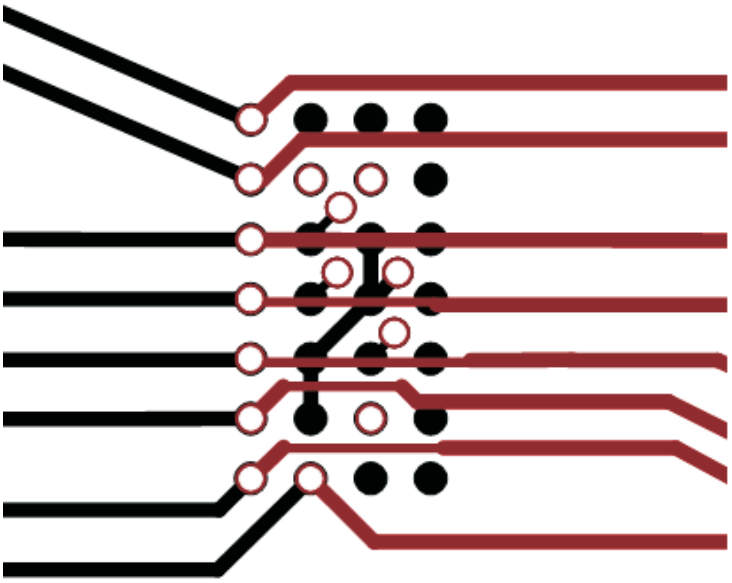

Figure 3. EVM High-speed Lines

Figure 3 shows the routing technique used on the HDMI high-speed lines. Black traces indicate that the trace is routed on the top layer and red traces indicates that the trace is routed on the bottom layer. Placing the high speed lines on the top and bottom layers was deliberate. This minimizes the number of vias needed, a good practice when routing high speed traces. Keeping the high-speed lines on the top and bottom also completely eliminates the need for blind or buried vias on these lines. Blind and buried vias can create stubs, which will increase the chances for reflections that could degrade signal quality.

There are potential advantages to placing the high speed lines internally. If the board environment is excessively noisy, by placing the lines internally the GND and power planes will shield them from external noise.

The 2.5mil trace width with 2.5mil spacing was used while routing the device through the 0.4mm pitch grid area. This is the width of the narrower portions of the traces shown in Figure 3. Filled vias with a 6mil drill diameter and an 8.6mil pad diameter were used for VIP (via in pad.) Outside of the device area, a 4mil width was used for signal traces.

For this device, VIP, with filled vias, was used on all the signal lines. VIP are shown as unfilled circles in Figure 3. However, the VIP must be filled on the board to ensure mechanical stability as well as good electrical connection and connectivity.

Trace lengths were matched within 10mil. This was done to minimize skew and is essential to preserving signal integrity. Trace impedance was 50 Ω.

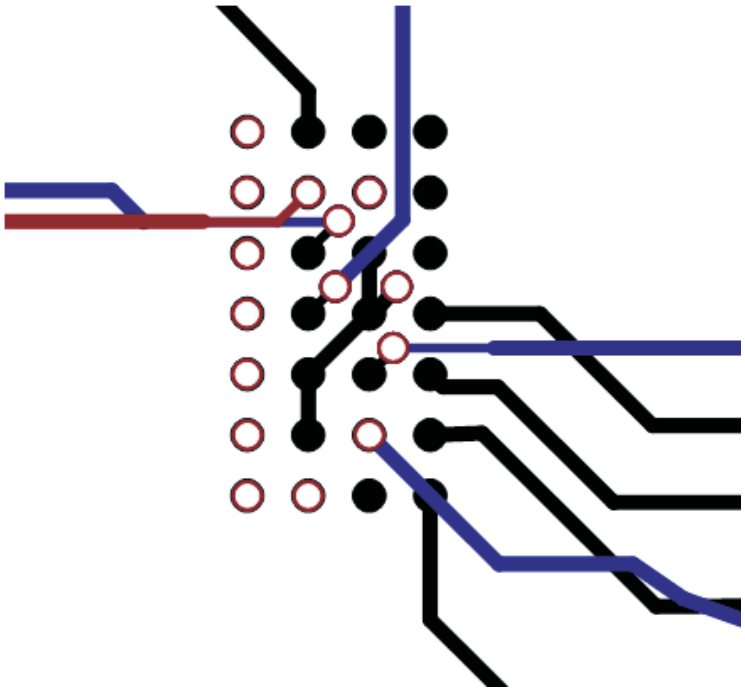

Figure 4. Low Speed Signal Routing

Control signal layers were placed on top and bottom, as well as on internal layers. The internal layer is designated in blue. These 'low speed' signals included the HPD, CEC and I^2C communication lines, as well as some of the control lines for the TPD12S015 device. Because these signals are only around 400 kHz, they are less sensitive to distortion caused by vias and longer or mismatched trace lengths. Again, 2.5mil trace widths and clearances were used in the space constrained device area, and 4mil was used outside the footprint.

4 DC/DC Circuitry

The DC/DC external circuitry is shown in the figure below. These discrete components should be kept as close to the device as possible and Figure 5 shows the optimum layout.

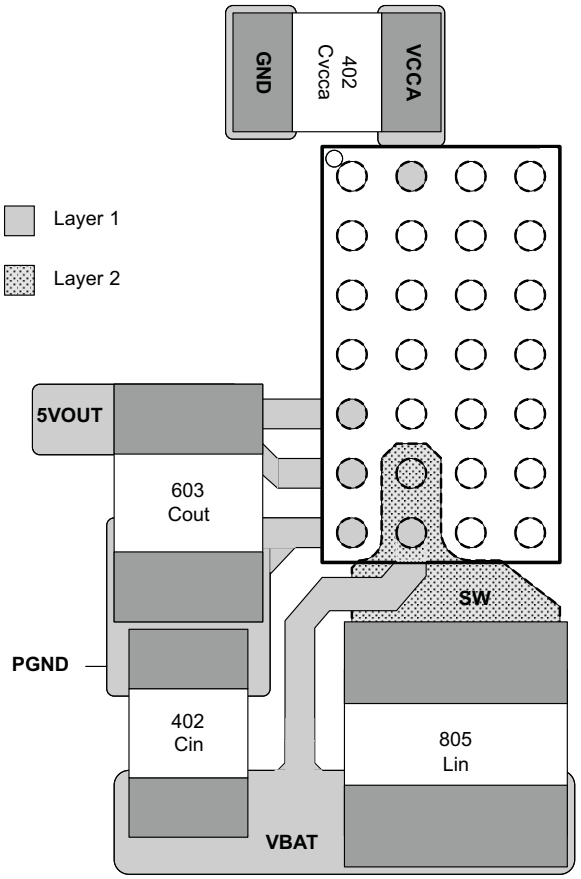

Figure 5. DC/DC Circuitry

Table 2. Recommended Values: External DC/DC Circuitry Components

COMPONENT	MIN	TARGET	MAX	UNIT
C_{IN}	1.2	4.7	6.5	µF
C_{OUT}	1.2	4.7	10	µF
L_{IN}	0.7	1	1.3	µH

The TPD12S015 cannot be used without these components. It was not designed to take 5V into the device 5VOUT pin. If a 5V supply is available this should be connected to VBAT and the discrete components laid out as shown in Figure 5. If the input voltage exceeds 5V, the output will track the input.

Table 3. Type C Connector Pin Assignment

PIN	SIGNAL ASSIGNMENT
1	TMDS Data2 Shield
2	TMDS Date 2+
3	TMDS Date 2–
4	TMDS Data1 Shield
5	TMDS Date 1+
6	TMDS Date 1–
7	TMDS Data0 Shield
8	TMDS Date 0+
9	TMDS Date 0–
10	TMDS Clock Shield
11	TMDS Clock+
12	TMDS Clock–
13	DDC/CEC Ground
14	CEC
15	SCL
16	SDA
17	Utility
18	+5V Power
19	Hot Plug Detect

Table 4. Type D Connector Pin Assignment

PIN	SIGNAL ASSIGNMENT		PIN	SIGNAL ASSIGNMENT
1	Hot Plug Detect		2	Utility
3	TMDS Data2+		4	TMDS Data2 Shield
5	TMDS Data2–		6	TMDS Data1+
7	TMDS Data1 Shield		8	TMDS Data1–
9	TMDS Data0+		10	TMDS Data0 Shield
11	TMDS Data0–		12	TMDS Clock+
13	TMDS Clock Shield		14	TMDS Clock–
15	CEC		16	DDC/CEC Ground
17	SCL		18	SDA
19	+5V Power			

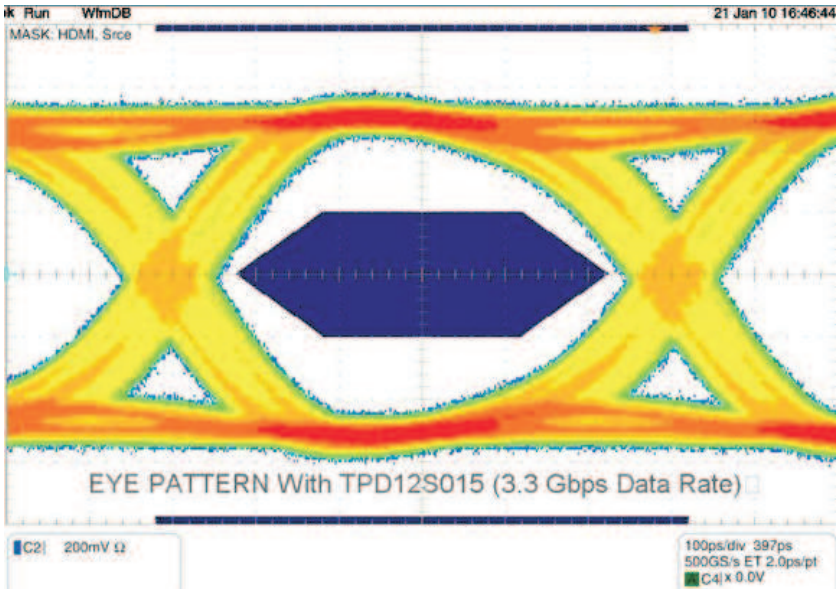

Figure 6. EVM Eye Diagram With Device Populated

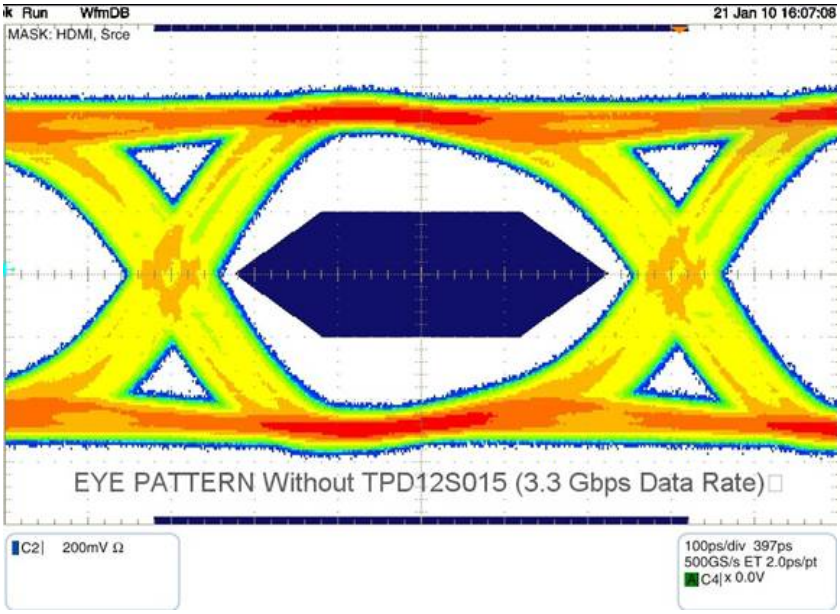

Figure 7. EVM Eye Diagram Without Device Populated

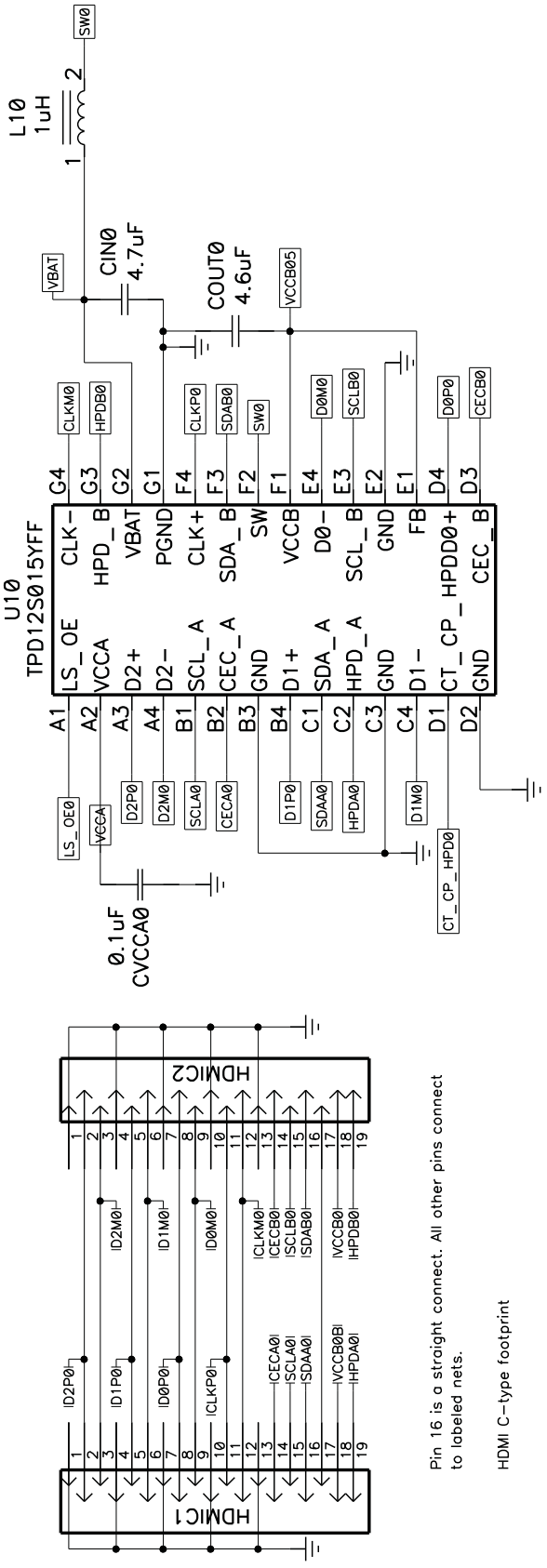

Figure 8. EVM Middle Segment Schematic

5 DSBGA Package and Board Manufacture

The following information is only a basic overview. Reading PCB Design Guidelines for 0.4mm Package-On-Package (PoP) Packages, Part I (SPRAAV1B) is highly recommended. The document goes in detail into the complexities of board design with 0.4mm pitch BGA devices and offers valuable suggestions.

In portable HDMI devices, board space is at a premium. With this in mind, the TPD12S015 is packaged in a 28 ball 0.4mm pitch DSBGA (die-sized ball grid array). It is important to work closely with your board manufacturer before beginning layout to determine their capabilities and their experience working with 0.4mm pitch packaging.

The manufacturing capabilities and suggestions of your board shop will determine such factors as footprint pads for the DSBGA, minimum trace width and clearance, and via sizing.

In 0.5mm packaging, NSMD (non-solder-mask-defined) pads are recommended. However, the TI OMAP group has had better success in 0.4mm packaging using solder mask defined pads. Your board manufacturer can provide information on the method that they have had best success with.

Figure 9 illustrates the difference between SMD and NSMD pads. In SMD pads, the opening in the solder mask (A) is smaller than the metal physical pad itself (B). The solder mask 'defines' the actual pad size. In NSMD pads, the solder mask opening is larger than the pad.

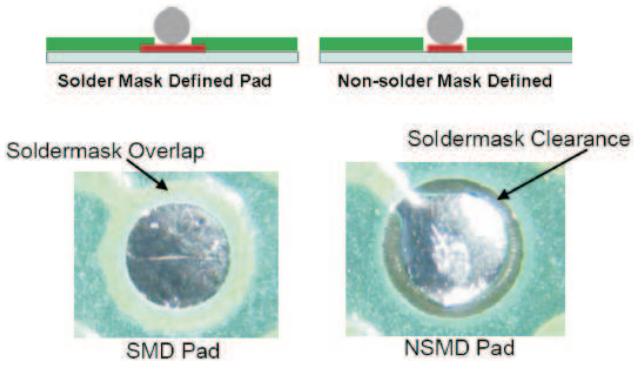

Figure 9. SMD and NSMD Pads

Via sizing is also an issue that requires consideration before beginning board design. Small via size is extremely important when working with the WCSBGA because device implementation relies heavily on the use of VIP (via in pad). There are two drilling methods used by board manufacturers, mechanical drilling and laser drilling. Avoiding the use of laser drilled vias can keep the price of board manufacture down. For the EVM discussed in the previous section, the board shop was capable of drilling 6 mil hole sizing without the use of a laser. Under pad vias were 8mil pad diameter and 6mil hole diameter.

Laser vias can be used smaller than the 6 mil hole, however this will raise board cost. The 2.5 mil tapers traces can be used between the balls in this package with 2.5 clearance on each side. The pads on the device itself were 8.6mil.

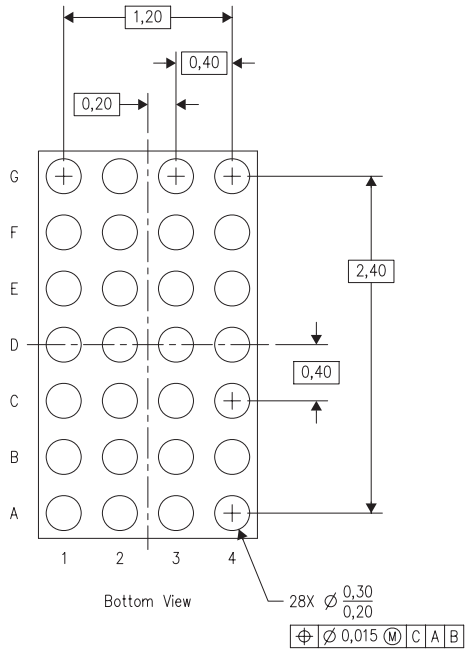

Figure 10. TPD12S015 Package Dimensions

6 General Layout Guidelines

As with all PCBs, there are some general 'good practice' rules that should be followed during layout. Unfortunately this list is by no means comprehensive; there are numerous resources which go into more detail, a few of which are listed in the reference section. Some of these guidelines are more important for specific HDMI lines and were detailed in the signal type in the Signal Types and Guidelines section.

Right angles should not be used on the board. Care should be used to keep angles no sharper than 45 degrees. Curved traces can also be used. Right angles are detrimental to signal integrity at high speeds because the width of the trace, and therefore it's electrical characteristics, change at a right angle.

Bypass capacitors should be placed on the V_{CCA} lines as close as possible to the device. This reduces the amount of noise from the V_{CCA}. Typical values for these bypass capacitors are 0.1uF.

Signal traces should not be routed over split planes. The trace impedance is in relation to the plane below the signals so split planes create a change in impedance on the line.

Trace lengths should be kept short. Longer trace lengths increase the amount of delay on the lines and can increase EMI radiation. Long traces can also corrupt signal integrity.

7 Summary

The three most important things to keep in mind when routing for the TPD12S015 are as follows:

1. Signal integrity on the high speed lines.
2. Attention to placement of the DC/DC circuitry.
3. Board shop capabilities in 0.4mil pitch devices.

Successful implementation of the TPD12S015 is a result of conscientious routing and working closely with the board manufacturer.

This is by no means a complete guide to PCB layout. Other sources of guidance are given in the references at the end. Specifically recommended are the PCB design guidelines for POP.

Visit www.ti.com for data sheets for all bit-width TXB translators along with the full line of Texas Instruments voltage translators.

8 References

- TPD12S015 Datasheet (SLLSE19B)
- High-Definition Multimedia Interface Specification Version 1.3a
- PCB Design Guidelines for 0.4mm Package-On-Package (PoP) Packages, Part I (SPRAAV1B)
- nFBGA Packaging SPRAA99

9 Appendix – A

9.1 HDMI Spec Testing

With the TPD12S015 The HDMI Test Specification allows for two device configurations during the HDMI DDC capacitance line testing (7.13) – 'device under test' (DUT) power on and DUT power off. The testing configuration to be used is declared in the 'Source Characteristics' section of the 'Capabilities Declaration Form' which is completed prior to testing and submitted to the testing house.

If the TPD12S015 is to be tested while the DUT is powered, level shifters must be disabled. This is done by keeping the LS_OE pin low.

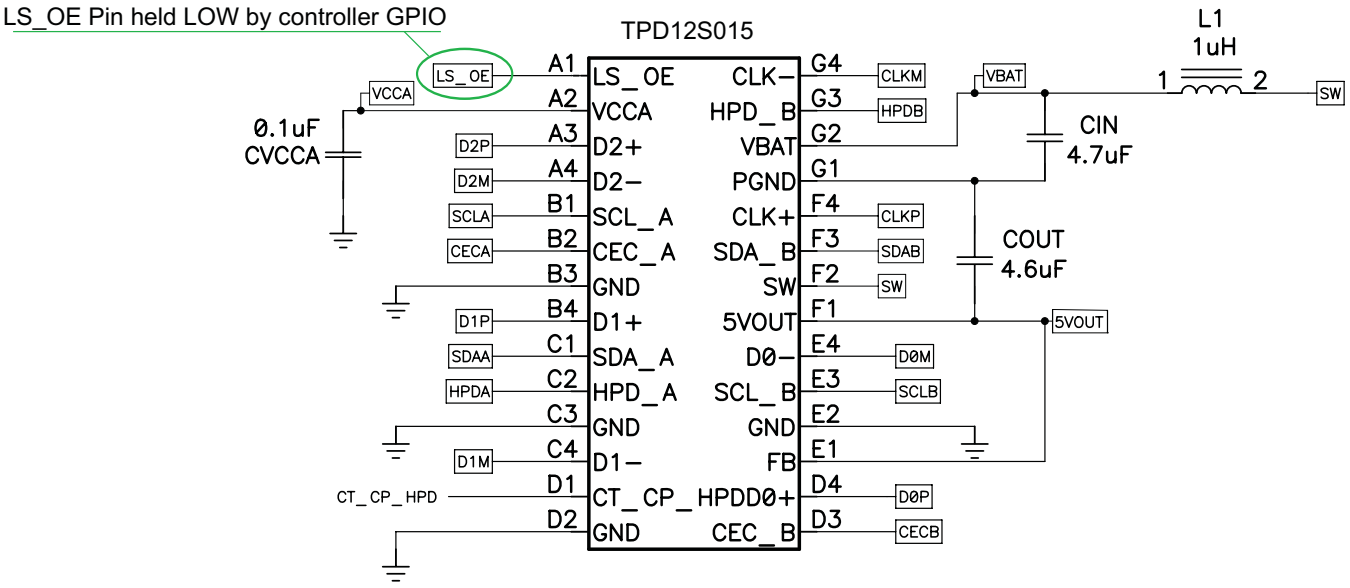

Figure 11. DUT Testing Device Powered

Testing the DUT unpowered requires an additional resistor connected as shown in the figure below. This resistor (R1) ensures that the voltage at the 5VOUT is kept low and the internal level-shifter circuitry remains unpowered.

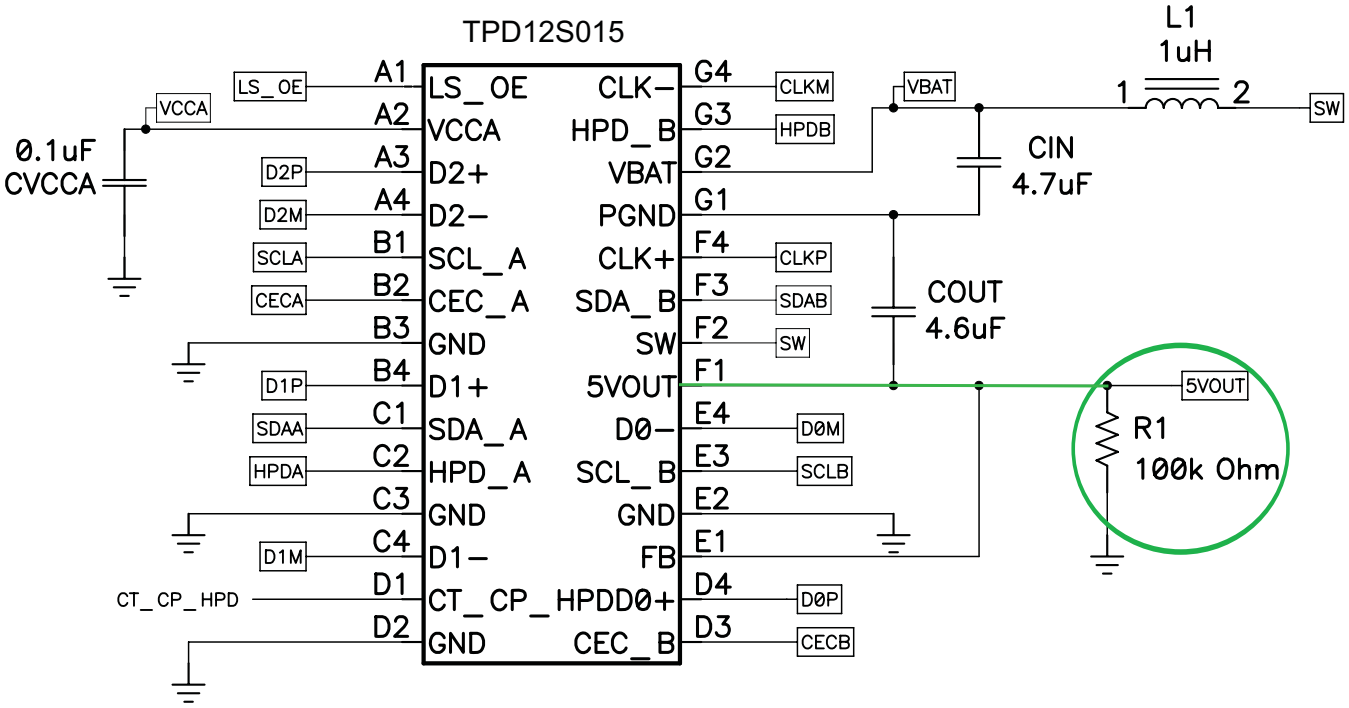

Figure 12. DUT Testing Device Unpowered

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