Application Report
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DC Output Errors in a Fully-Differential Amplifier

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ABSTRACT

This report gives a brief analysis and the results for DC output error calculations for a fully-differential voltage feedback amplifier. For additional information on operation and design applications for fully-differential amplifiers consult the application report Fully-Differential Amplifiers (SLOA054,[2]). Many of the assumptions and quantities used in this analysis are borrowed directly from the applications report mentioned above.

This report is divided into several sections. The first section describes the model and lists the associated sources of DC output error that are considered in the analysis. The second section gives the detailed analysis which concludes with a single and expression for the total DC output error resulting from all of the associated error sources. Subsequent sections give the individual error source contributions to the total output error, and discuss the implications of some simplifying assumptions, such as resistor matching.

A subsection with examples is also included. It shows a numerical comparison between the analytical model and a TINA simulation for one of the validating test cases, and an example of using the model to predict the worst-case output error for the THS4521, a high-speed, low-power fully-differential amplifier. The last section is a summary table of the individual error source contributions to the total output error.

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1 DC Error Model for a Fully-Differential Amplifier

Figure 1 shows the equivalent DC model for input offset and bias currents for a fully-differential amplifier. The DC errors in the output of a fully-differential voltage feedback amplifier shown in the circuit diagram in Figure 1 are due to six factors:

1. Input offset voltage (V_{IO}).
2. Input bias currents (I_{IB+}, I_{IB-})
3. Mismatch between input and output common-mode voltages (V_{OCM} –V_{ICM})
4. Common-mode rejection ratio (CMRR)
5. Power supply rejection ratio (PSRR)
6. Resistor mismatch

The voltage source V_{IO} represents input offset voltage, while the bias current sources I_{IB+} and I_{IB-} are the input bias currents for the non-inverting and inverting input terminals respectively. The offset voltage is evenly split between the two input pins to facilitate the analysis.

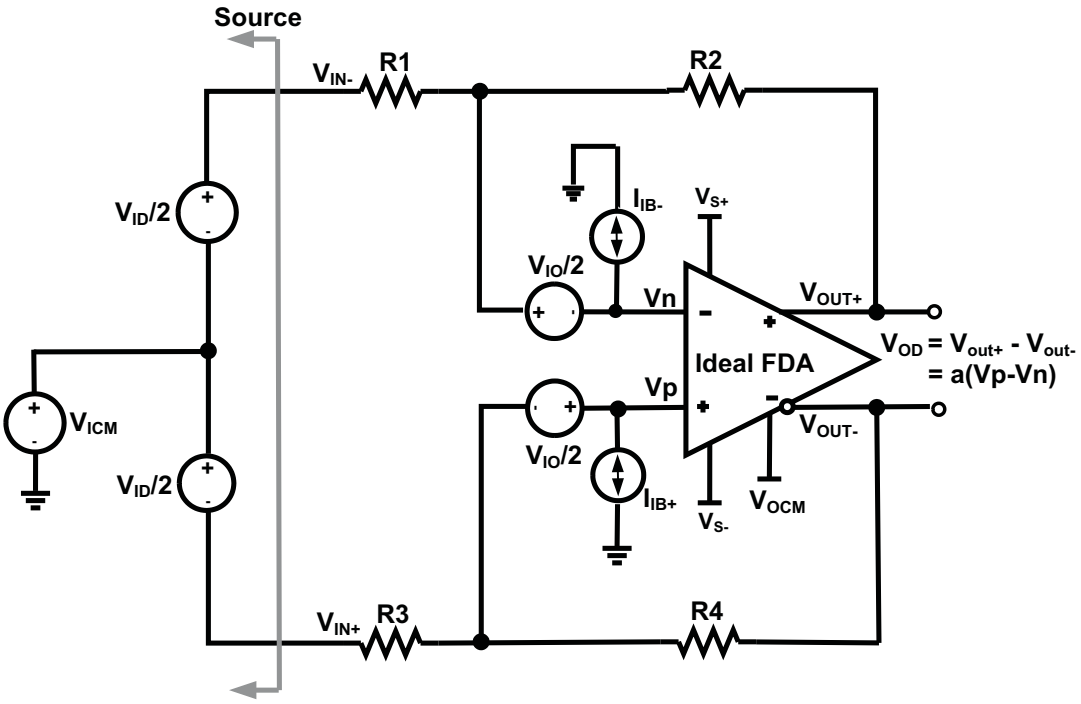


Figure 1. DC Error Model of a Fully-Differential Amplifier

2 Analysis of Total Output Error

The ideal differential and common-mode outputs of the fully-differential amplifier are given respectively by the relationships:

$$V_{OD,IDEAL} = V_{OUT+} - V_{OUT-} - = a\,(Vp - Vn)$$
$$V_{OCM} = (V_{OUT+} + V_{OUT-})/2 \quad (1)$$

where the parameter *a* is the open-loop gain of the device and Vp and Vn are the voltages at the non-inverting and inverting input terminals of the device.

Not shown in the schematic diagram are the DC errors because of an input common-mode signal and because of power supply variations. The device input common-mode signal is given by the mean value of the two input voltages at the device input pins: $V_{CM,IN}$ = (Vp+Vn)/2. The output of an ideal device (see

Equation 1) depends only on the difference of the input voltages, and the input common-mode voltage is rejected by the ideal device. In an actual device, some component of the input common-mode voltage appears at the device output as an error. Following the definition by Franco [1], the differential output error due to the incomplete rejection of the input common-mode voltage can be expressed as an effective common-mode gain that multiplies the common-mode voltage at the device input pins Vn and Vp:

$$\Delta V_{OD}\left(V_{CM,IN}\right) = a_{CM} V_{CM,IN} \tag{2}$$

Note the *device* input common-mode ($V_{CM,IN}$) is not the same as the *applied input* common-mode voltage of the circuit from the signal source (V_{ICM}). If CMRR = a/a_{CM}, then the expression for the output error due to the input common-mode voltage is:

$$\Delta V_{OD}\left(V_{CM,IN}\right) = a\frac{V_{CM,IN}}{CMRR} = a\frac{(Vp + Vn)/2}{CMRR} \tag{3}$$

The output error due to power supply fluctuations can be expressed in a similar manner:

$$\Delta V_{OD}\left(V_S\right) = a\frac{\Delta V_S}{PSRR} \tag{4}$$

Adding these errors to the open-loop expression in Equation 1 gives:

$$V_{OD} = a\left[Vp - Vn + \frac{(Vp + Vn)/2}{CMRR} + \frac{V_{O,PS}}{PSRR}\right] \tag{5}$$

The common-mode and power supply effects are referenced back to the device input pins via the open-loop gain *a*, which allows modeling these terms as additional input offsets. Rearranging and grouping like terms gives:

$$\begin{aligned} V_{OD} &= a\left[\left(1 + \frac{1}{2CMRR}\right)Vp - \left(1 - \frac{1}{2CMRR}\right)Vn + \frac{\Delta V_S}{PSRR}\right] \\ &= a\left[b_1 Vp - b_2 Vn + \frac{\Delta V_S}{PSRR}\right] \end{aligned}$$

where:

$$\begin{aligned} b_1 &= \left(1 + \frac{1}{2CMRR}\right) \\ b_2 &= \left(1 - \frac{1}{2CMRR}\right) \end{aligned} \tag{6}$$

Using the relationships in Equation 1 gives:

$$\begin{aligned} V_{OD} &= V_{OUT+} - V_{OUT-} \\ &= 2V_{OUT+} - 2V_{OCM} = a\left[b_1 Vp - b_2 Vn + \frac{\Delta V_S}{PSRR}\right] \end{aligned} \tag{7}$$

The corresponding voltages at the input terminals (Vp and Vn) that result from input signal and feedback voltages are given by:

$$\begin{aligned} Vn &= V_{IN-}\left(1-\beta_2\right) + V_{OUT+}\beta_2 + I_{IB-}R_{EQ1} - V_{IO}/2 \\ Vp &= V_{IN+}\left(1-\beta_1\right) + V_{OUT-}\beta_1 + I_{IB+}R_{EQ2} + V_{IO}/2 \end{aligned} \tag{8}$$

Where β_1 = R3/(R3+R4) and β_2 = R1/(R1+R2) represent the feedback factors for the circuit in Figure 1. The equivalent resistances

R_{EQ1} = R1 || R2 = R1R2/(R1 + R2) and R_{EQ2} = R3 || R4 = R3R4/(R3 + R4)

represent the parallel resistances of the gain-setting and feedback resistors. The parameters V_{IO}, I_{IB+} and I_{IB-} are the input offset voltage and input bias currents as described above.

Substituting the equations in Equation 8 into Equation 7 gives:

$$V_{OUT+}\left(b_1\beta_1 + b_2\beta_2 + \frac{2}{a}\right) = b_1V_{IN+}\left(1 - \beta_1\right) - b_2V_{IN-}\left(1 - \beta_2\right) + 2V_{OCM}\left(b_1\beta_1 + \frac{1}{a}\right)$$
$$+ b_1I_{IB+}R_{EQ2} - b_2I_{IB-}R_{EQ1} + \frac{V_{IO}}{2}\left(b_1 + b_2\right) + \frac{V_{O,PS}}{PSRR} \quad (9)$$

A similar equation may be derived for the inverting output (V_{OUT-}) by applying the relationship $V_{OD} = 2V_{OUT-} - 2V_{OCM}$ and working though the same series of manipulations as before, beginning with Equation 8:

$$-V_{OUT-}\left(b_1\beta_1 + b_2\beta_2 + \frac{2}{a}\right) = b_1V_{IN+}\left(1 - \beta_1\right) - b_2V_{IN-}\left(1 - \beta_2\right) - 2V_{OCM}\left(\beta_2 + \frac{1}{a}\right)$$
$$+ b_1I_{IB+}R_{EQ2} - b_2I_{IB-}R_{EQ1} + \frac{V_{IO}}{2}\left(b_1 + b_2\right) + \frac{V_{O,PS}}{PSRR} \quad (10)$$

Summing Equation 9 and Equation 10 for a dependency on the differential output V_{OD} gives:

$$V_{OD}\left(b_1\beta_1 + b_2\beta_2 + \frac{2}{a}\right) = 2b_1V_{IN+}\left(1 - \beta_1\right) - 2b_2V_{IN-}\left(1 - \beta_2\right) + 2V_{OCM}\left(b_1\beta_1 - b_2\beta_2\right)$$
$$+ 2b_1I_{IB+}R_{EQ2} - 2b_2I_{IB-}R_{EQ1} + V_{IO}\left(b_1 + b_2\right) + 2\frac{V_{O,PS}}{PSRR} \quad (11)$$

Expressing the circuit inputs (V_{IN+}, V_{IN-}) in terms of the balanced sources and the applied common-mode voltage (V_{ICM}) shown in the schematic above gives:

$$V_{IN+} = V_{ICM} + V_{ID}/2$$
$$V_{IN-} = V_{ICM} - V_{ID}/2 \quad (12)$$

It can be convenient to express the bias currents (I_{IB+}, I_{IB-}) in terms of their common components and differential (offset) components:

$$I_{IB+} = I_{IB} + I_{IO}/2$$
$$I_{IB-} = I_{IB} - I_{IO}/2 \quad (13)$$

The equivalent schematic of a fully-differential amplifier first presented in Figure 1 can be redrawn to reflect the identical bias currents and offset current.

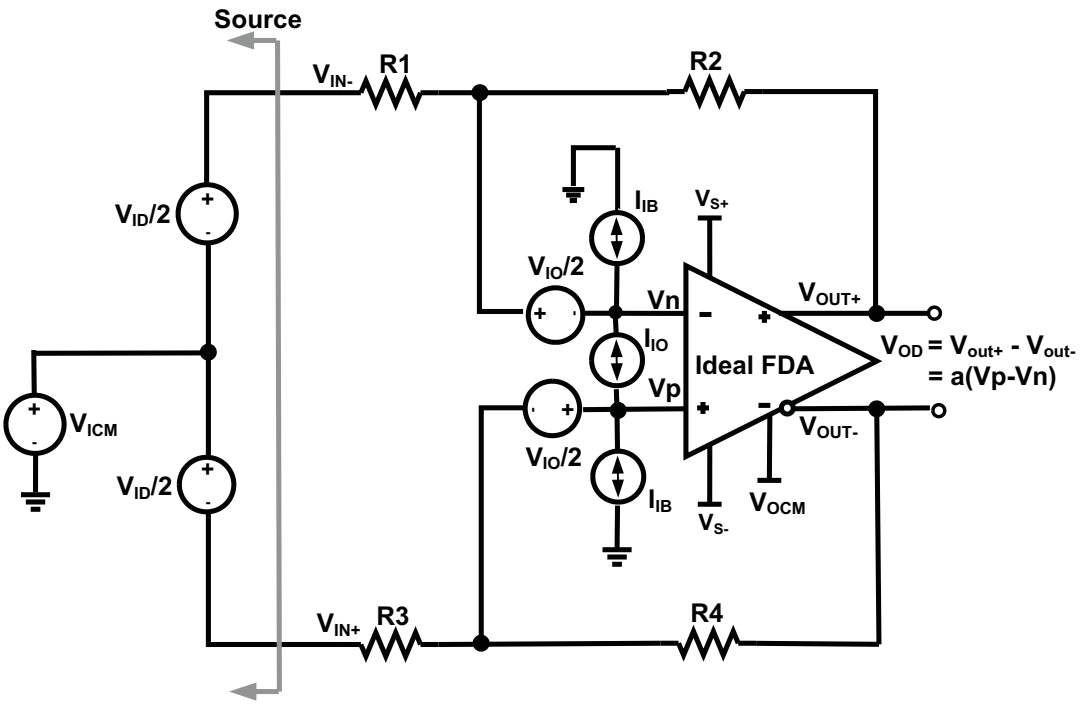


Figure 2. DC Error Model of a Fully-Differential Amplifier with Input Offset Current

Substituting Equation 12 and Equation 13 into Equation 11 and combining terms results in an expression for the desired differential output as well as the sources of output error:

$$V_{OD} = \frac{\left[\begin{array}{c} V_{id}\left(2 - b_1\beta_1 - b_2\beta_2\right) \\ +V_{IO}\left(b_1 + b_2\right) \\ +2I_{IB}\left(b_1R_{EQ1} - b_2R_{EQ2}\right) \\ +I_{IO}\left(b_1R_{EQ1} + b_2R_{EQ2}\right) \\ +2\left(V_{OCM} - V_{ICM}\right)\left(b_1\beta_1 - b_2\beta_2\right) \\ +\frac{2V_{ICM}}{CMRR} + 2\frac{V_{O,PS}}{PSRR} \end{array}\right]}{\left(b_1\beta_1 + b_2\beta_2 + \frac{2}{a}\right)}$$

Desired Output Signal

Output error

where: b_1 and b_2 were first defined in equation (6)

$$b_1 = 1 + \frac{1}{2CMRR}$$

$$b_2 = 1 - \frac{1}{2CMRR} \quad (14)$$

The total output of the FDA can be divided into a single desired output signal and six sources of output error that are caused by input offsets and bias (V_{IO}, I_{IO}, I_{IB}), finite common-mode and power supply rejection (CMRR, PSRR) and joint mismatch between common-mode voltages (V_{ICM}, V_{OCM}) and feedback paths (β_1, β_2). The contribution of each error source to the total output error is given in the following sections.

3 The Impact of Individual Error Sources on the Output Error

3.1 Desired Signal

The term $V_{id}\left(2 - b_1\beta_1 - b_2\beta_2\right) / \left(b_1\beta_1 + b_2\beta_2 + 2/a\right)$ in Equation 14 represents the desired output and the remainder of the numerator terms represent differential output error. Substituting the quantities b_1 and b_2 gives an expression which shows the impact of the imbalanced feedback paths ($\beta_1 \neq \beta_2$) and the finite common-mode rejection (CMRR < ∞) on the output level of the desired signal:

$$V_{OD}\left(\text{desired}\right) = V_{id}\frac{2 - \left(\beta_1 + \beta_2\right) - \frac{1}{2CMRR}\left(\beta_1 - \beta_2\right)}{\left(\beta_1 + \beta_2\right) + \frac{1}{2CMRR}\left(\beta_1 - \beta_2\right) + 2/a} \quad (15)$$

Note that the combination of imbalanced feedback paths and finite CMRR can affect the desired signal output level. If the feedback paths are balanced (R1=R3, R2=R4 → $\beta_1 = \beta_2 = \beta$) and the open-loop gain a >> 1, the desired output simplifies to:

$$V_{OD}\left(\text{desired}\right) \underset{a \approx \infty}{\overset{\beta_1 = \beta_2}{\Rightarrow}} V_{id}\left(\frac{1 - \beta}{\beta}\right) \quad (16)$$

Equation 16 is a general result also reported in [2]. Note that for matched feedback paths, the effects of finite CMRR have no impact on the desired signal component.

3.2 Output Error Due to Input Offset Voltage (V_{IO})

The output error due to the input offset voltage can be taken from Equation 14 and is given by:

$$\Delta V_{OD}\left(V_{IO}\right) = \frac{V_{IO}\left(b_1 + b_2\right)}{b_1\beta_1 + b_2\beta_2 + \frac{2}{a}} \quad (17)$$

Substituting the expressions for b_1 and b_2 gives:

$$\Delta V_{OD}(V_{IO}) = \frac{2V_{IO}}{(\beta_1 + \beta_2) + \frac{1}{2CMRR}(\beta_1 - \beta_2) + \frac{2}{a}} \tag{18}$$

Note that effects of finite common-mode rejection can increase or decrease the offset-induced output error if the feedback paths are not balanced (e.g., $\beta_1 \neq \beta_2$). If the feedback paths are balanced (R1=R3, R2=R4 $\rightarrow \beta_1 = \beta_2 = \beta$) and the open-loop gain a >> 1, the output error due to the input offset voltage simplifies to:

$$\Delta V_{OD}(V_{IO})\Big|_{\substack{a\to\infty \\ R1=R3 \\ R2=R4}} = \frac{V_{IO}}{\beta} = V_{IO}\frac{R1+R2}{R1} \tag{19}$$

The ratio (R1+R2)/R1 is sometimes referred to as the *noise gain* [1].

3.3 Output Error Due to Bias Current (I_{IB})

An expression for the output error due to the input bias current I_{IB} is shown below, adapted from Equation 14:

$$\Delta V_{OD}(I_{IB}) = \frac{2I_{IB}(b_1R_{EQ1} - b_2R_{EQ2})}{\left(b_1\beta_1 + b_2\beta_2 + \frac{2}{a}\right)} \tag{20}$$

Substituting the expressions for b_1 and b_2 gives:

$$\Delta V_{OD}(I_{IB}) = 2I_{IB}\frac{(R_{EQ1} - R_{EQ2}) + \frac{1}{2CMRR}(R_{EQ1} + R_{EQ2})}{(\beta_1 + \beta_2) + \frac{1}{2CMRR}(\beta_1 - \beta_2) + \frac{2}{a}} \tag{21}$$

The parameters R_{EQ1} = R1 || R2 and R_{EQ2} = R3 || R4 represent the parallel resistances formed by the gain-setting and feedback resistors. If the feedback paths are not symmetrical (e.g., $\beta_1 \neq \beta_2$), the output error can increase or decrease, depending on the values for the associated resistors.

If the feedback paths are symmetric (R1=R3, R2=R4 $\rightarrow \beta_1 = \beta_2 = \beta$) and CMRR effects are negligible, there is no bias-induced output error. If CMRR effects are not negligible, there is an output error term, even if the feedback paths are symmetric. If the open-loop gain *a* >> 1, the output error caused by the bias current is:

$$\Delta V_{OD}(I_{IB}) \underset{a\approx\infty}{\overset{\beta_1=\beta_2}{\Rightarrow}} \frac{I_{IB}}{\beta}\frac{R_{EQ}}{CMRR} = I_{IB}\frac{R2}{CMRR} \tag{22}$$

Which shows that for finite common-mode rejection, the bias current interacts with the feedback resistance to produce an output error, even if the feedback paths are symmetric.

3.4 Output Error Due to Input Offset Current (I_{IO})

An expression for the output error due to the input offset current I_{IO} is shown below, adapted from Equation 14:

$$\Delta V_{OD}(I_{IO}) = \frac{I_{IO}(b_1R_{EQ1} + b_2R_{EQ2})}{\left(b_1\beta_1 + b_2\beta_2 + \frac{2}{a}\right)} \tag{23}$$

Substituting the expressions for b_1 and b_2 gives:

$$\Delta V_{OD}(I_{IO}) = I_{IO}\frac{(R_{EQ1} + R_{EQ2}) + \frac{1}{2CMRR}(R_{EQ1} - R_{EQ2})}{(\beta_1 + \beta_2) + \frac{1}{2CMRR}(\beta_1 - \beta_2) + \frac{2}{a}} \tag{24}$$

If the feedback paths are symmetric (R1=R3, R2=R4 → $\beta_1 = \beta_2 = \beta$ and $R_{EQ1} = R_{EQ2} = R_{EQ}$), the output error due to the input offset current becomes independent of the CMRR and depends only on the offset current flowing through the feedback resistor:

$$\Delta V_{OD}(I_{IO}) = I_{IO}R2 \tag{25}$$

3.5 Input and Output Common-Mode Mismatch (V_{OCM},V_{ICM})

The contribution of mismatch between the input and output common-mode voltages to the output error is given by:

$$\Delta V_{OD}(V_{OCM},V_{ICM}) = \frac{2(V_{OCM} - V_{ICM})(b_1\beta_1 - b_2\beta_2)}{\left(b_1\beta_1 + b_2\beta_2 + \frac{2}{a}\right)} \tag{26}$$

Two specific cases are worth considering. First, if CMRR is ideal and the open-loop gain a >> 1, then the output error reduces to:

$$\Delta V_{OD}(V_{OCM},V_{ICM}) \underset{a>>1}{\overset{CMRR=\infty}{\Rightarrow}} \frac{2(V_{OCM} - V_{ICM})(\beta_1 - \beta_2)}{(\beta_1 + \beta_2)} \tag{27}$$

So if the CMRR is large and the feedback paths are symmetrical or the input and output common-mode voltages are matched, there is no contribution to output error. A frequent application for FDAs is to provide a common-mode level shift from input to output, such as when an FDA is used as a dc-coupled driver for an analog-to-digital converter (ADC). Such an application precludes matched input and output common-mode voltages ($V_{OCM} \neq V_{ICM}$). In such a case, the related output error may be made negligible by selecting symmetric feedback paths (R1 = R3, R2 = R4).

Second, if the CMRR is finite, and the feedback paths are symmetric, the output error becomes dependent solely on the mismatch of the common-mode voltages, and the common-mode rejection:

$$\Delta V_{OD}(V_{OCM},V_{ICM}) \underset{a>>1}{\overset{\beta_1=\beta_2}{\Rightarrow}} \frac{(V_{OCM} - V_{ICM})}{CMRR} \tag{28}$$

3.6 Input Common-Mode and Power Supply Rejection

Output error due to the incomplete rejection of the input common-mode voltage and to power supply fluctuations is adapted from Equation 14:

$$\Delta V_{OD}(V_{ICM},\Delta V_S) = \frac{2\frac{V_{ICM}}{CMRR} + 2\frac{\Delta V_S}{PSRR}}{\left(b_1\beta_1 + b_2\beta_2 + \frac{2}{a}\right)} \tag{29}$$

If the feedback paths are symmetric and the open-loop gain *a* is large, the output error due to the combined factor becomes:

$$\Delta V_{OD}(V_{ICM},\Delta V_S) \underset{a>>1}{\overset{\beta_1=\beta_2}{\Rightarrow}} \frac{1}{\beta}\left(\frac{V_{ICM}}{CMRR} + \frac{\Delta V_S}{PSRR}\right) \tag{30}$$

4 Numerical Examples

4.1 Validation of the Analytical Model

The general analysis was validated with TINA simulations using an idealized model of the differential amplifier as shown in Figure 1. One of the test cases is included as an example. The total output offset error shows precise agreement between the analytical model and TINA simulations.

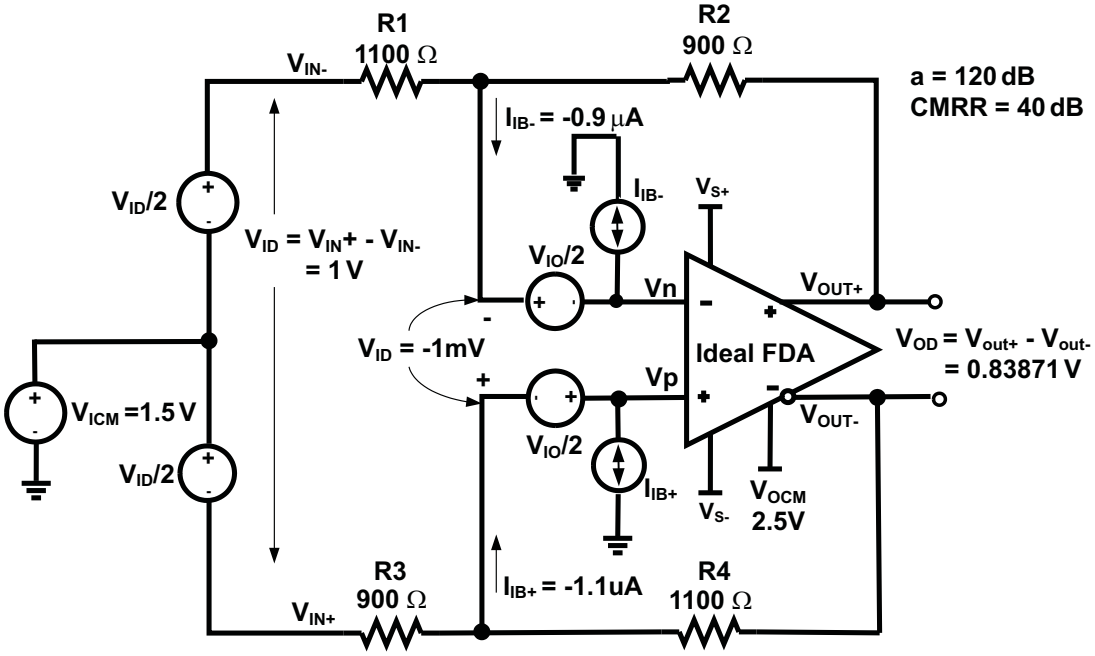


Figure 3. Circuit for Example Calculation of Output Error

Table 1. Circuit and Device Parameters Shown in Figure 3

Device/Circuit Parameters	Value		Derived/Calculated Parameters	Value
V_{ID}	1 V			
V_{ICM}	1.5 V			
V_{OCM}	2.5 V		I_{IB}	–1 µA
R1	1100 Ω		I_{IO}	–0.2 µA
R2	900 Ω		b_1	1.005
R3	900 Ω		b_2	0.995
R4	1100 Ω		β_1	0.45
V_{IO}	–1 mV		β_2	0.55
I_{IB+}	–1.1 µA		R_{EQ1}	495 Ω
I_{IB-}	–0.9 µA		R_{EQ2}	495 Ω
a	120 dB			
CMRR	40 dB			
Results:				
V_{OD} – model	**0.83871V**			
V_{OD} – TINA	**0.83871V**			

4.2 Example with the THS4521

The THS4521 is a low-power FDA with a rail-to-rail output (RRO) and a negative rail input. The THS4522 and THS4524 are dual and quad versions of this device. The RRO feature, high dynamic range, and low noise make the THS4521 an excellent driver amp for successive approximation register (SAR) and delta-sigma A/D converters. The THS4521 can also serve as a low-power audio amplifier and has excellent DC precision for a high-speed FDA. This subsection shows some example calculations based on data sheet parameters of this device and on the application circuit shown in Figure 4. (Figure 68 from the device data sheet).

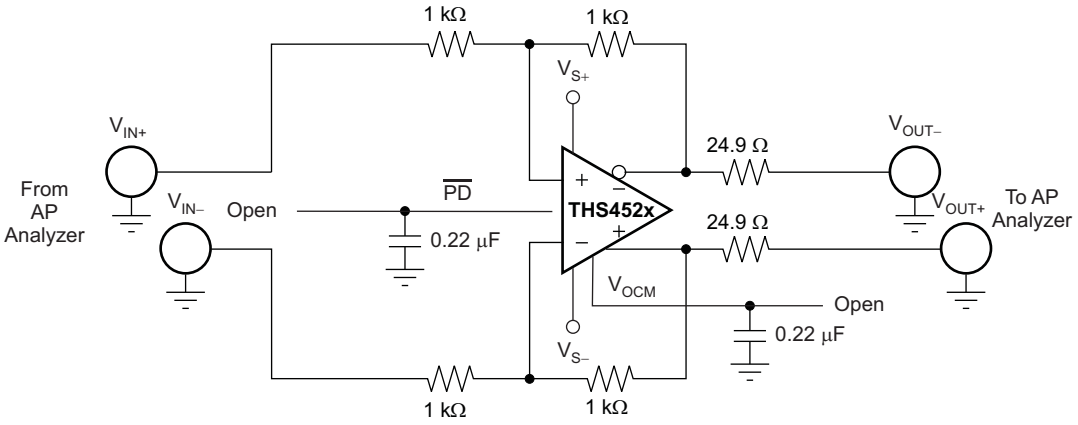


Figure 4. Example Circuit From the THS4521 Data Sheet

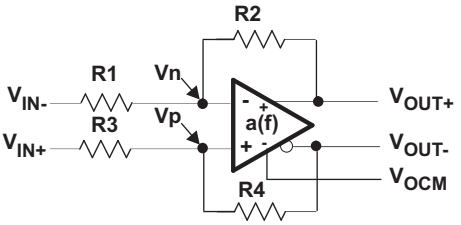
Taking the DC parameters from the device data sheet (+25°C, max values) and assuming a worst-case mismatch of the gain resistors (1% tolerance) results in the following parameters in Table 2. As the bottom row of the table shows, the total output offset for the worst-case condition is approximately equal to ±0.4mV.

Table 2. Circuit and Model Parameters for the THS4521 Circuit Shown in Figure 4

Circuit and Device Parameters	Value	Derived Model Parameters
R1 (lower left)	990 Ω	β_2 = 0.495 R_{EQ1} = 499.95
R2 (lower right)	1010	
R3 (upper left)	1010	β_1 = 0.505 R_{EQ2} = 499.95
R4 (upper right)	990	
V_{IO}	±2 mV	
I_{IB}	±0.85 µA	
I_{IO}	±50 pA	
a	116 dB	
CMRR	100 dB	b_1,b_2 = 1 ± 5×10^{-6}
PSRR	100 dB	
Vs+	5 V	
VCM	2.5 V	
Vin	1 V	
V_{ICM}	2.5 V	
Total Output Error	**±0.4mV**	

4.3 Summary

The desired output voltage as well as the error sources and their contribution to the output error are summarized in the table below for the following circuit:



Quantity	Symbol	General Expression	Asymptotic Form
Feedback factors	β_1,β_2	β_1 = R3/(R3 + R4), β_2 = R1/(R1 + R2)	
Coefficients	b_1,b_2	$b_1 = \left(1+\frac{1}{2CMRR}\right) \quad b_2=\left(1-\frac{1}{2CMRR}\right)$	
Equivalent resistances	R_{EQ1},R_{EQ2}	R_{EQ1} = R1 || R2, R_{EQ2} = R3 || R4	
Applied input common-mode	V_{ICM}	$V_{ICM} = \frac{(V_{IN-} + V_{IN+})}{2}$	
Desired output	$V_{OD,\ Desired}$	$V_{id}\frac{2 - (\beta_1+\beta_2)-\frac{1}{2CMRR}(\beta_1 - \beta_2)}{(\beta_1 + \beta_2) + \frac{1}{2CMRR}(\beta_1 - \beta_2) + 2/a}$	$V_{id}\left(\frac{1-\beta}{\beta}\right)$
Output error due to input offset voltage	$\Delta V_{OD}(V_{IO})$	$\frac{2V_{IO}}{(\beta_1 + \beta_2) + \frac{1}{2CMRR}(\beta_1 - \beta_2) + \frac{2}{a}}$	$V_{IO}\frac{R1 + R2}{R1}$
Output error due to input bias currents	$\Delta V_{OD}(I_{IB})$	$2I_{IB}\frac{(R_{EQ1} - R_{EQ2})+\frac{1}{2CMRR}(R_{EQ1} + R_{EQ2})}{(\beta_1 + \beta_2) + \frac{1}{2CMRR}(\beta_1 - \beta_2)+\frac{2}{a}}$	$I_{IB}\frac{R2}{CMRR}$
Output error due to input offset current I_{IO}	$\Delta V_{OD}(I_{IO})$	$I_{IO}\frac{(R_{EQ1} + R_{EQ2}) + \frac{1}{2CMRR}(R_{EQ1} - R_{EQ2})}{(\beta_1 + \beta_2) + \frac{1}{2CMRR}(\beta_1 - \beta_2)+\frac{2}{a}}$	$I_{IO}R2$
Output error due to common-mode mismatch $V_{OCM} - V_{ICM}$	$\Delta V_{OD}(V_{OCM} - V_{ICM})$	$\frac{2(V_{OCM} - V_{ICM})(b_1\beta_1 - b_2\beta_2)}{(\beta_1 + \beta_2) + \frac{1}{2CMRR}(\beta_1 - \beta_2)+\frac{2}{a}}$	$\frac{(V_{OCM} - V_{ICM})}{CMRR}$
Output error due to input common-mode V_{ICM}	$\Delta V_{OD}(V_{ICM})$	$\frac{2V_{ICM}/CMRR}{(\beta_1 + \beta_2) + \frac{1}{2CMRR}(\beta_1 - \beta_2)+\frac{2}{a}}$	$\frac{1}{\beta}\frac{V_{ICM}}{CMRR}$
Output error due to power supply variations	$\Delta V_{OD}(\Delta V_S)$	$\frac{2\Delta V_S/PSRR}{(\beta_1 + \beta_2) + \frac{1}{2CMRR}(\beta_1 - \beta_2)+\frac{2}{a}}$	$\frac{1}{\beta}\frac{\Delta V_S}{PSRR}$

5 References

1. Sergio Franco, *Design with Linear Operational Amplifiers and Analog Integrated Circuits*, Third Edition, McGraw-Hill, New York, NY, 2002
2. *Fully-Differential Amplifiers*, author: James Karki, Texas Instruments (SLOA054D)

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