

Highly Integrated PMIC for Powering the SiRFatlasIV™

PMP-DC Power Mgmt Units

ABSTRACT

This design was created to help those needing to power the SiRFatlasIV and doing so by implementing a highly integrated and efficient design using the TPS65072 power management unit.

1 Introduction

This reference design is for powering one SiRFatlasIV™ and accounts for voltage and current; requirements are presented in [Table 1](#). The TPS65072 is a power management integrated circuit (PMIC), suitable for applications that require multiple power rails. The TPS65072 provides three highly efficient, step-down converters targeted at providing the core voltage, peripheral, I/O, and memory rails in the system. The SiRFatlasIV requires 1.2-V, 1.8-V, and 3.3-V input.

2 Power Requirements

The power requirements for each SiRFatlasIV are listed in the following table.

For more information and other reference designs, visit www.ti.com/processorpower.

Table 1. SiRFatlasIV Power Requirements

| Core, I/O | Pin Name | Voltage | I _{max} (mA) | Tolerance |
|-----------|-----------|---------|-----------------------|-----------|
| I/O | VDDIO_MEM | 1.8 | 600 | ±5% |
| | VDDIO | 3.3 | 600 | ±5% |
| | VDD_PDN | 1.2 | 600 | ±5% |
| | VDD_PRE | 1.2 | 200 | ±5% |
| | VDDPLL | 1.2 | 200 | ±5% |

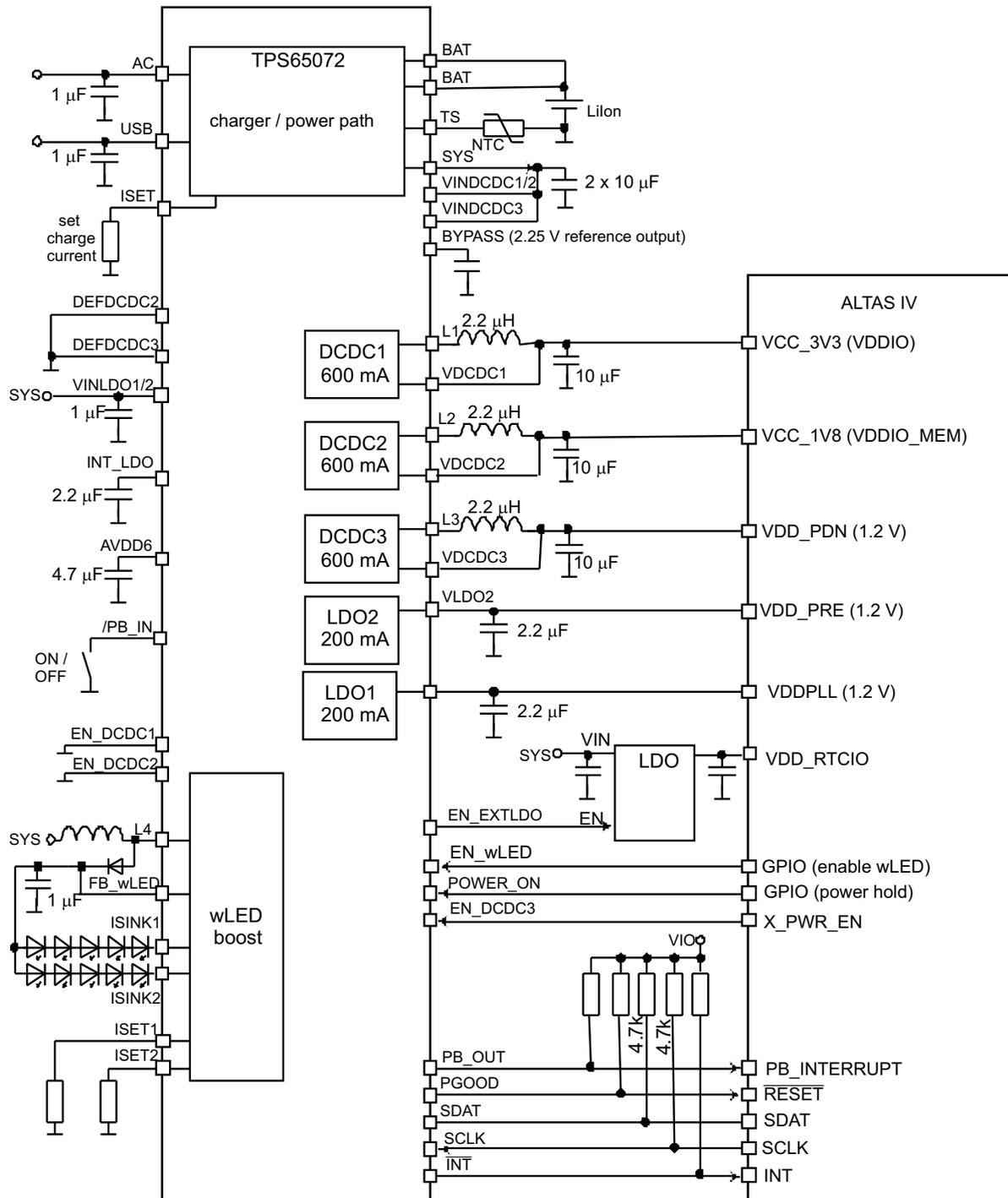
2.1 Device Features

TPS65072

- Charger/Power Path Management
 - 2-A Output Current on the Power Path
 - Linear Charger; 1.5-A Maximum Charge Current
 - 100-mA/500-mA/ 800-mA/1300-mA Current Limit From USB Input
 - Thermal Regulation, Safety Timers
 - Temperature Sense Input
- Three Step-Down Converters:
 - 2.25-MHz, Fixed-Frequency Operation
 - Up to 1.5 A of Output Current
 - Adjustable or Fixed Output Voltage
 - VIN Range From 2.8 V to 6.3 V
 - Power Save Mode at Light-Load Current
 - Output Voltage Accuracy in PWM Mode ±1.5%
 - Typical 19-µA Quiescent Current per Converter
 - 100% Duty Cycle for Lowest Dropout

SiRFatlasIV is a trademark of SiRF Technology, Inc.

- LDOs
 - Fixed Output Voltage
 - Dynamic Voltage Scaling on LDO2
 - 20- μ A Quiescent Current
 - 200-mA Maximum Output Current



Note: /Reset to Atlas 4 may need to be a RC delay from VDDIO

Figure 1. Typical Configuration for Powering the SiRFatlasIV Processor

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