Application Report
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bq20z80 Printed Circuit Board Layout Guide

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ABSTRACT

Attention to layout is critical to the success of any battery management circuit board. The mixture of high current paths with an ultra low current microcontroller creates the potential for design issues that are not always trivial to solve. Guidelines are presented to insure a stable and well performing project.

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1 Introduction

Attention to layout is critical to the success of any battery management circuit board. The mixture of high current paths with an ultra low current microcontroller creates the potential for design issues that are not always trivial to solve. Careful placement and routing with regard to the principles described below will insure success.

2 Component Placement

2.1 Power Supply Decoupling Capacitors

Power supply decoupling is very important for optimal operation of the bq20z80 advanced gas gauge. To keep the loop area small, place these capacitors right next to the IC. Use the shortest possible traces to the IC. Ideally, the traces on each side of the capacitor should be the same length and run in the same direction to avoid differential noise during ESD. If possible, place a via near the VSSD pin to the digital ground plane and another from near the VSSA pin to the analog ground plane.

Figure 1 is an example of what **NOT** to do. The VDDA and VDDD decoupling caps are close to the IC, but the loop area is huge, rendering the capacitor useless and forming a nice little loop antenna for noise pickup.

2.2 AFE Decoupling and LDO Compensatio Capacitor

Power supply decoupling for the bq29312A can best be achieved by placing a 1 µF/25 V capacitor mid way between pin 1 and pin 12.

The LDO voltage regulator within the bq29312A requires a 4.7 µF capacitor to be placed fairly close to the REG pin. This cap is for amplifier loop stabilization as well as an energy well for the load.

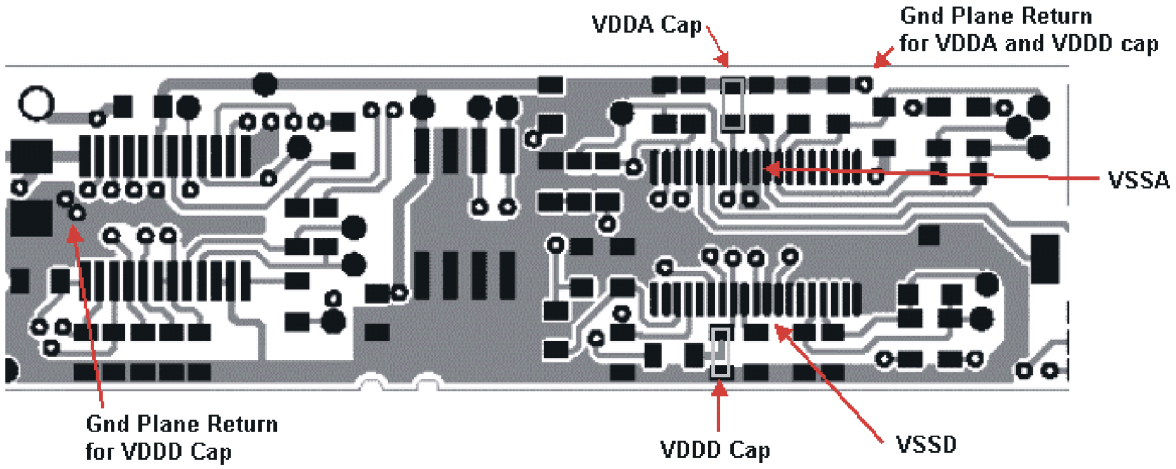

Figure 1. Bad Example of Decoupling Capacitor Placement and Routing

2.3 PLL, Oscillator and Master Reset Components

The VCO in the phase locked loop (PLL) requires a low pass filter. Since this is a sensitive circuit, care should be used to place these components relatively close to pin 32 of the IC.

The 100K oscillator resistor, if used instead of a crystal, is perhaps the most critical component surrounding the bq20z80. Because the clock circuit is based on an extremely low level current source, any ground noise can introduce unwanted jitter into the 32 kHz clock. Place the resistor close to the IC, connecting to pins 33 and 34. Pin 34 is of special concern since it must be connected to analog ground when an oscillator resistor is used. Use a separate trace to connect pin 34 to analog ground at pins 29/30. This will prevent any unwanted ground current from interfering with the clock.

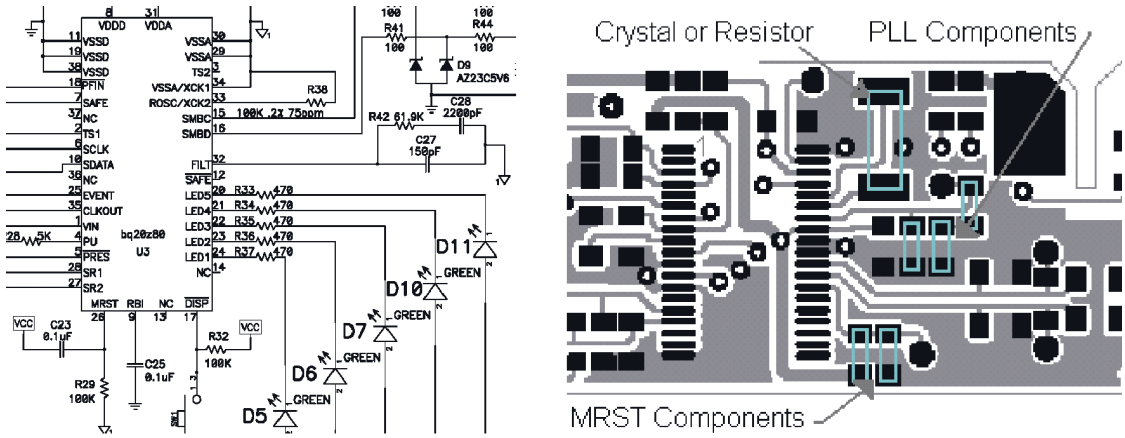

Figure 2. Minimize Length and Loop Area for These Critical Components to Reduce Noise Pickup

2.4 Communication Line Protection Components

The 5.6V zener diodes, used to protect the communication pins of the bq20z80 from ESD should be located as close to the pack connector as possible. The grounded end of these zeners should be returned to the Pack(–) node, rather than to the low current digital ground system. This way, ESD will be diverted away from the sensitive electronics as much as possible.

2.5 Protector FET Bypass and Pack Terminal Bypass Capacitors

The general principle is to use wide copper traces to lower the inductance of the bypass capacitor circuit. In Figure 3, an example layout demonstrates this technique.

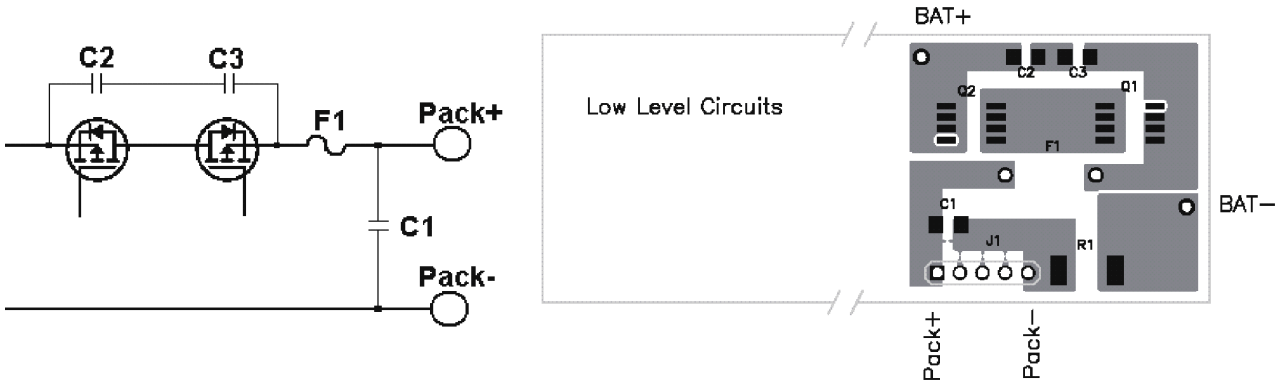

Figure 3. Use Wide Copper Traces to Lower the Inductance of Bypass Capacitors C1, C2, C3

2.6 Ground Systems

The bq20z80 will perform optimally when two separate low current ground systems are defined – analog and digital ground. In addition, ESD ground is defined along the high current path from the Pack(–) terminal to the sense resistor. Refer to the ground symbols in the bq20z80 reference design, and provide separate low current ground systems accordingly. It is important that these two ground systems only connect together at the sense resistor Kelvin pick-off point as shown in Figure 4. Use inner layer ground planes, if possible, for each low current ground system.

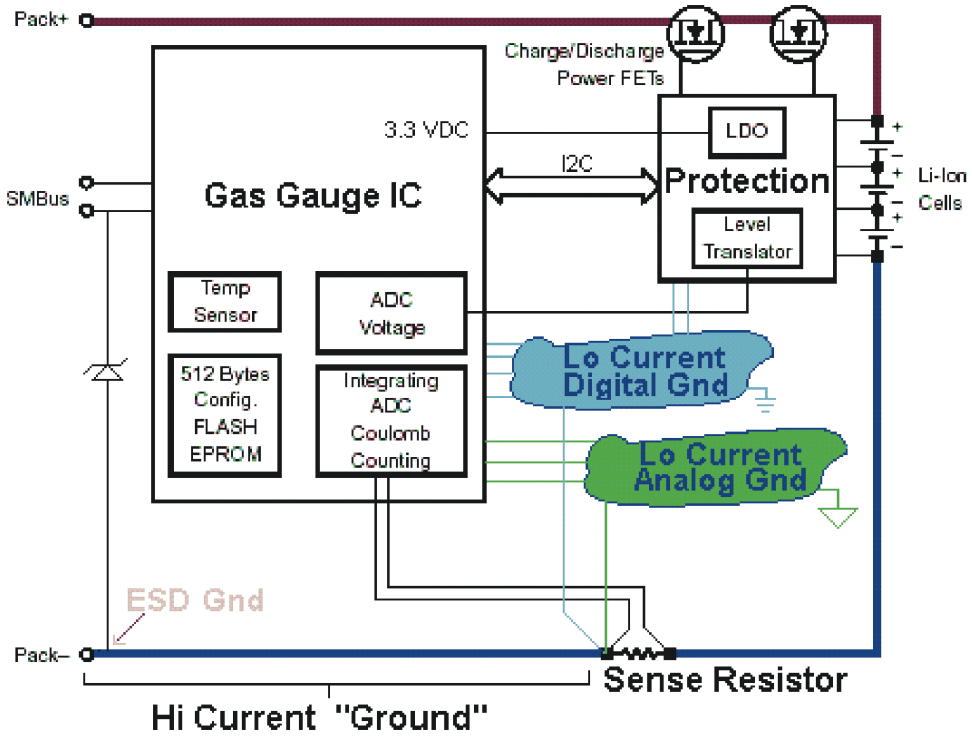

Figure 4. Use Separate Analog and Digital Low-Current Ground Systems

3 Kelvin Connections

Kelvin voltage sensing is extremely important in order to accurately measure current, and top and bottom cell voltages. Figure 5 and Figure 6 demonstrate *right* and *wrong* techniques.

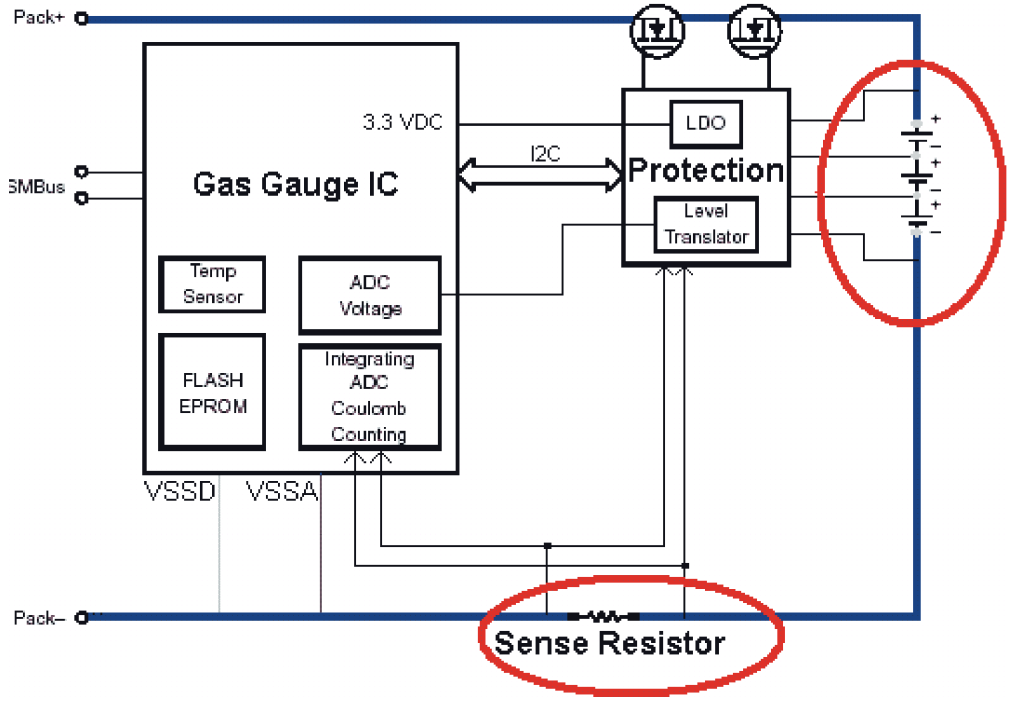

Figure 5. WRONG! Sensing through high current copper traces produces measurement errors.

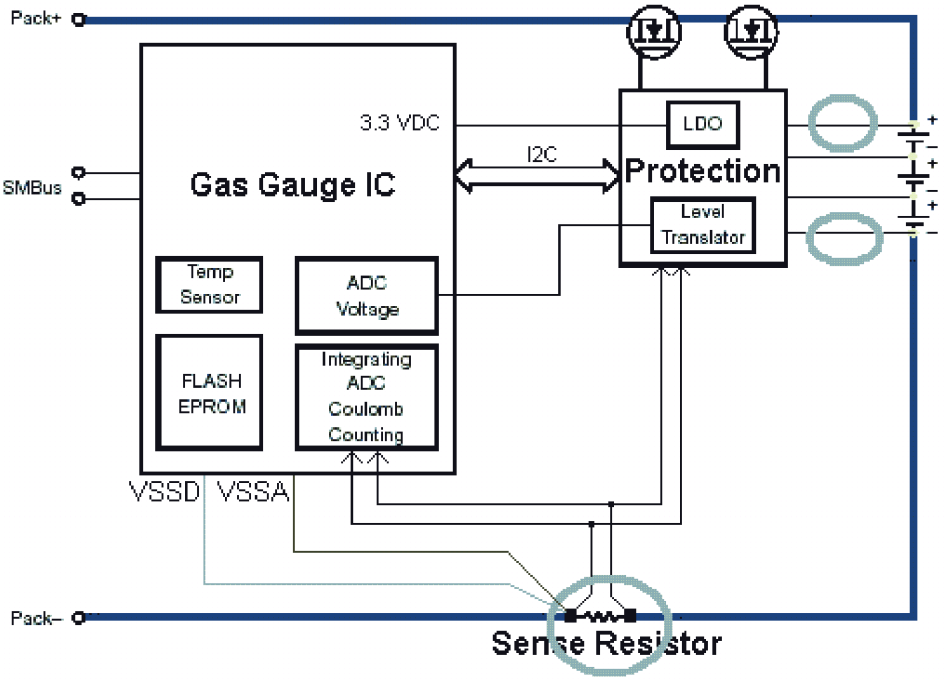

Figure 6. RIGHT! In some cases, top and bottom cell voltage sensing may be extended out to the cells.

4 Board Offset Considerations

While the most important component for board offset reduction is the decoupling capacitor for VDDA, additional benefit is possible by using this recommended pattern for the Coulomb Counter differential low pass filter network. Maintain the symmetrical placement pattern shown for optimum current offset performance. Use symmetrical shielded differential traces, if possible, from the sense resistor to the 100 Ω resistors.

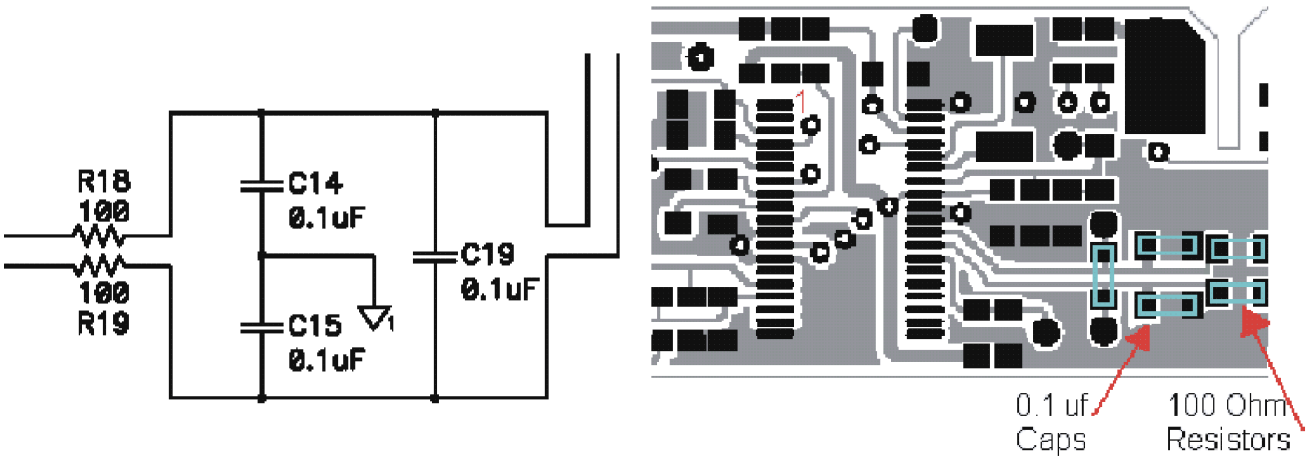

Figure 7. Differential Filter Components With Symmetrical Layout

5 ESD Spark Gap

Protect SMBus Clock, Data, and other communication lines from ESD with a spark gap at the connector. The pattern in Figure 8 is recommended, with 0.2 mm spacing between the points.

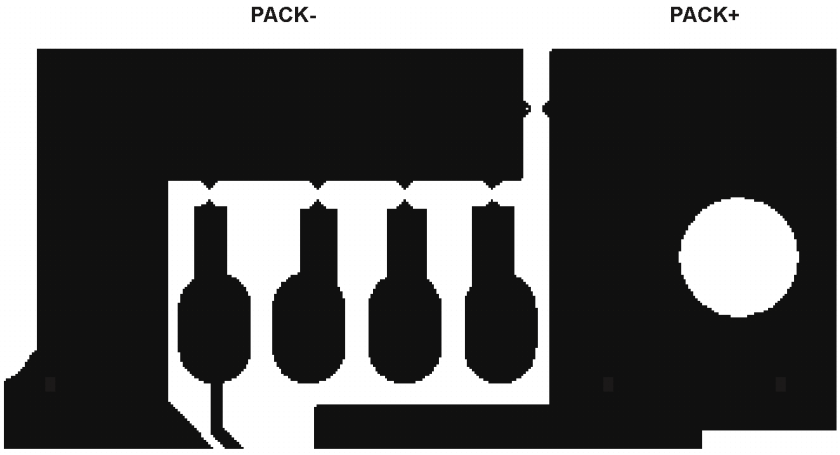

Figure 8. Recommended Spark Gap Pattern Helps Protect Communication Lines From ESD

5.1 Unwanted Magnetic Coupling

A battery fuel gauge circuit board is a challenging environment due to the fundamental incompatibility of high current traces and ultra-low current semiconductor devices. The best way to protect against unwanted trace-to-trace coupling is with a component placement such as that shown in Figure 3, where the high current section is on the right and electronics devices on the left. Clearly this is not possible in many situations due to mechanical constraints. Still, every attempt should be made to route high current traces away from signal traces, which enter the bq20z80 directly. ICs can be damaged due to magnetic and capacitive coupling from the high current path. Note that during high current and ESD events, the high current traces appear inductive due to the fast current rise time, as illustrated in Figure 8.

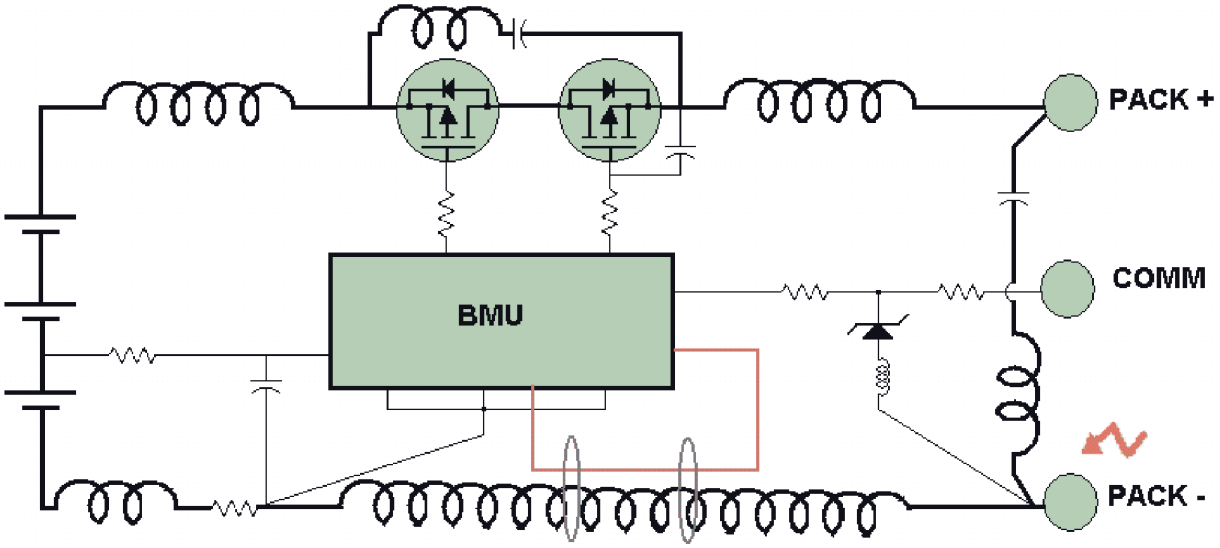

Figure 9. Avoid Close Spacing Between High Current and Low Level Signal Lines

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