Minimizing Buck-Boost (Inverting) Converter High-Frequency Switching Noise

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ABSTRACT

This application report explains how to use proper board layout and bypass capacitors to reduce high-frequency switching noise generated by a buck-boost (inverting) switching converter.

1 Description of the Problem

Various nodes of a switching converter can generate high amplitude switching noise in the 100-MHz+ range. Figure 1 shows an a-coupled voltage measurement taken at the input (CH1-**top**, brown) and output (CH2-**bottom**, blue) of a TPS63700 configured to provide V_{OUT} = –12 V at 150 mA from V_{IN} = 5 V. The time scale is 80 ns/div. The ground loop on each voltage probe was minimized.

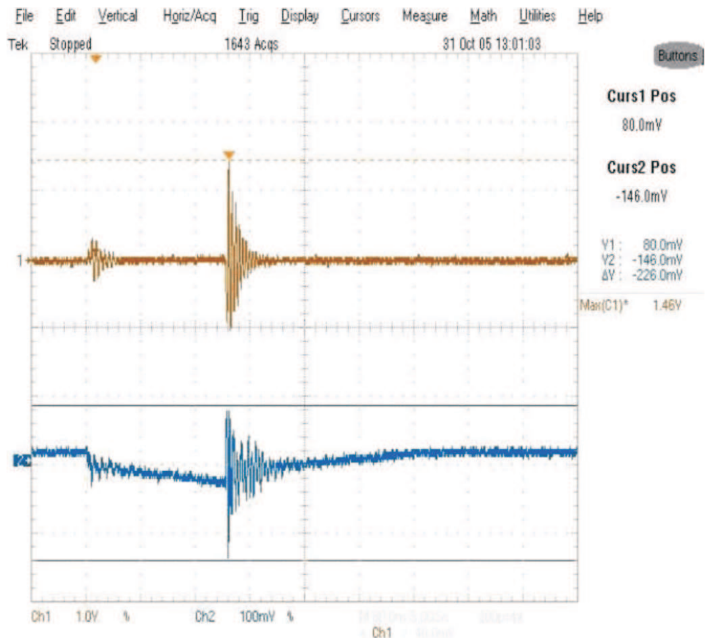

Figure 1. High-Frequency Switching Noise Measurement Using Bad Board Layout

Switching noise over 200 MHz and 220 mV_{pk-pk} on the output and over 2 V_{pk-pk} on the input is present. Figure 2 shows the board layout. Multiple 25-V ceramic output capacitors (C7–C10) are used in parallel due to the unavailability of a single 22-µF, 25-V-rated output capacitor. Notice that the output capacitors (C7–C10) and diode D1 are far from the IC and that the input capacitor (C1) and output capacitors (C7–C10) share a common ground plane.

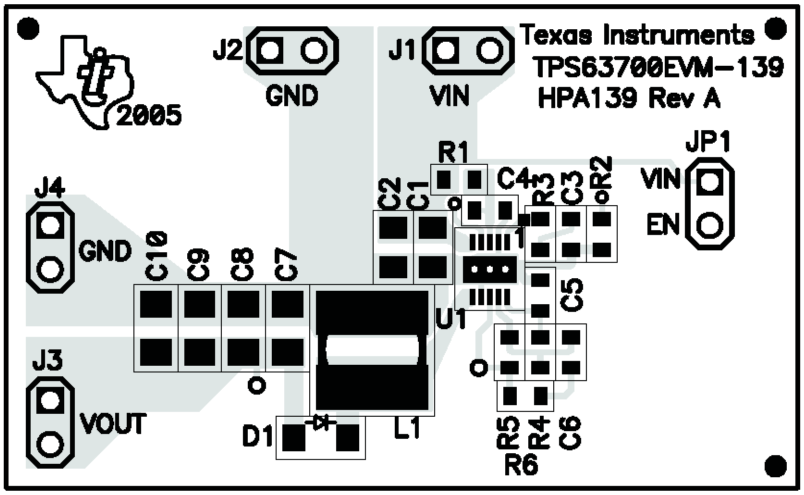

Figure 2. Inverter Bad Board Layout

The *critical loop*, shown in blue in Figure 3, is created by the parasitic inductances and capacitances, shown in red, in the inverter power stage. These parasitic capacitances and inductances interact at each switching cycle to produce the switching noise seen at V_{IN} and V_{OUT} in Figure 1. Where possible, the designer must select FETs and diodes with minimal parasitic capacitances. Through proper board layout, the designer must minimize the parasitic inductances, $L_{PAR\#}$, by placing the bulk input capacitor as close as possible between the power switch, Q1, and a single power ground point, close to the converter IC's power ground pin. The bulk output and the bulk output capacitance also must be placed as close as possible between the diode, D1, and the same power ground point. Additional high-frequency bypass capacitors, $C_{IN\text{-}BYP}$ and $C_{OUT\text{-}BYP}$, in the range of 0.01 µF to 0.47 µF, are best at reducing the ringing seen between V_{IN} and ground and V_{OUT} and ground.

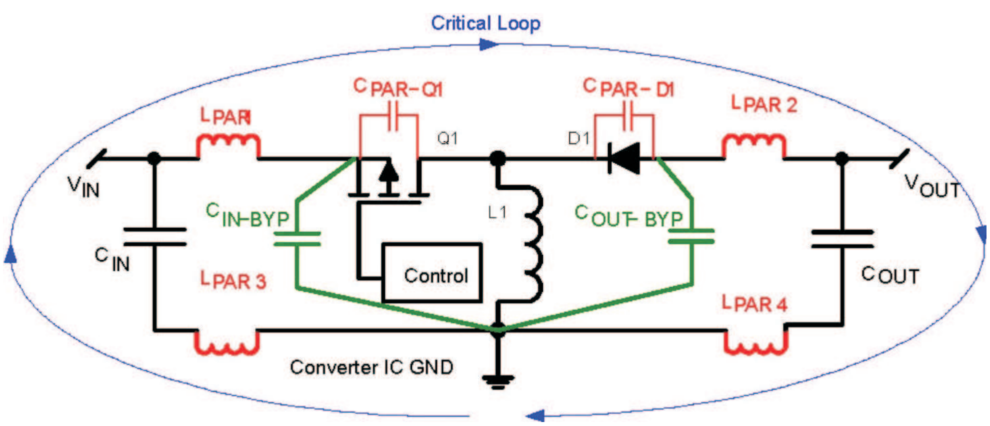

Figure 3. Buck-Boost (Inverting) Converter Schematic

2 Implementation of Solution

Figure 4 shows the layout for the TPS63700 after implementing the previously mentioned recommendations. High-frequency bypass capacitors C2 on the input voltage and C7 on the output voltage were added and placed as close between VIN and power ground and V_{OUT} and power ground as possible. Also, note that the input and output grounds do not share a ground plane except at a point close to the IC.

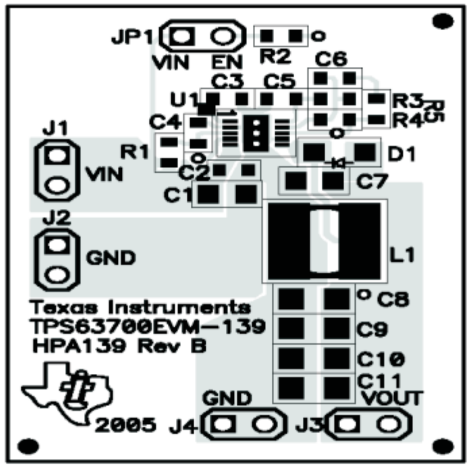

Figure 4. Inverter Improved Board Layout

Figure 5 shows switching noise measured under the same conditions used in Figure 1 but with the improved board layout. The time scale is 40 ns/div. Switching noise has been reduced to about 170 mV on the output and under 500 mV_{pk-pk} on the input.

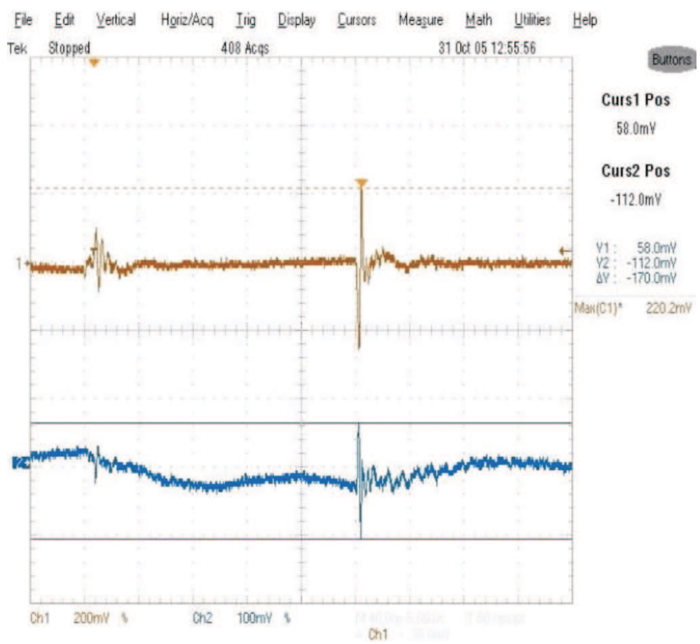

Figure 5. High-Frequency Switching Noise on Output of Inverter Using Improved Board Layout and Bypass Capacitors

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