

Customizing Your TPS6510x/TPS6514x

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ABSTRACT

This application report shows how to use external circuitry to boost the output voltage capability of the positive and negative charge pumps of the TPS6510x and TPS6514x triple output power supplies. In addition, the report shows how to use external circuitry to modify the internally controlled sequencing, implement sequencing delay, and short circuit protection.

Introduction

When using LCDs with lower liquid crystal cell voltage, the required source voltage from the main boost converter V_{OUT1} is typically 7 V to 8 V. However, the required TFT gate voltage (VGH) may need to be in the range of 23 V to 24 V. The simplest method to produce VGH is to quadruple V_{OUT1} . In addition, applications like portable DVD players or small-size LCD displays require a negative voltage, VGL, down to $-2 \times V_{OUT1}$. By adding a discrete charge pump composed of two small external capacitors and a small, SOT-23 or smaller packaged dual Schottky diode to the charge pump tripled V_{OUT3} and inverted V_{OUT2} voltages of the TPS6510x/4x family, the voltages necessary for these applications can easily be realized. The efficiency of the charge pumps is still acceptable. The approximate efficiency excluding switching and quiescent current losses of such a charge pump is calculated as shown in Equation 1.

$$\eta = \frac{Vo3}{Vo1 * M} = \frac{23V}{7.5V * 4} = 76\% \text{ with } M = \text{Charge pump gain (2, 3, or 4)} \quad (1)$$

The HPA031EVM for the TPS65140 was modified to implement the circuits described in the following paragraphs (see Figure 1).

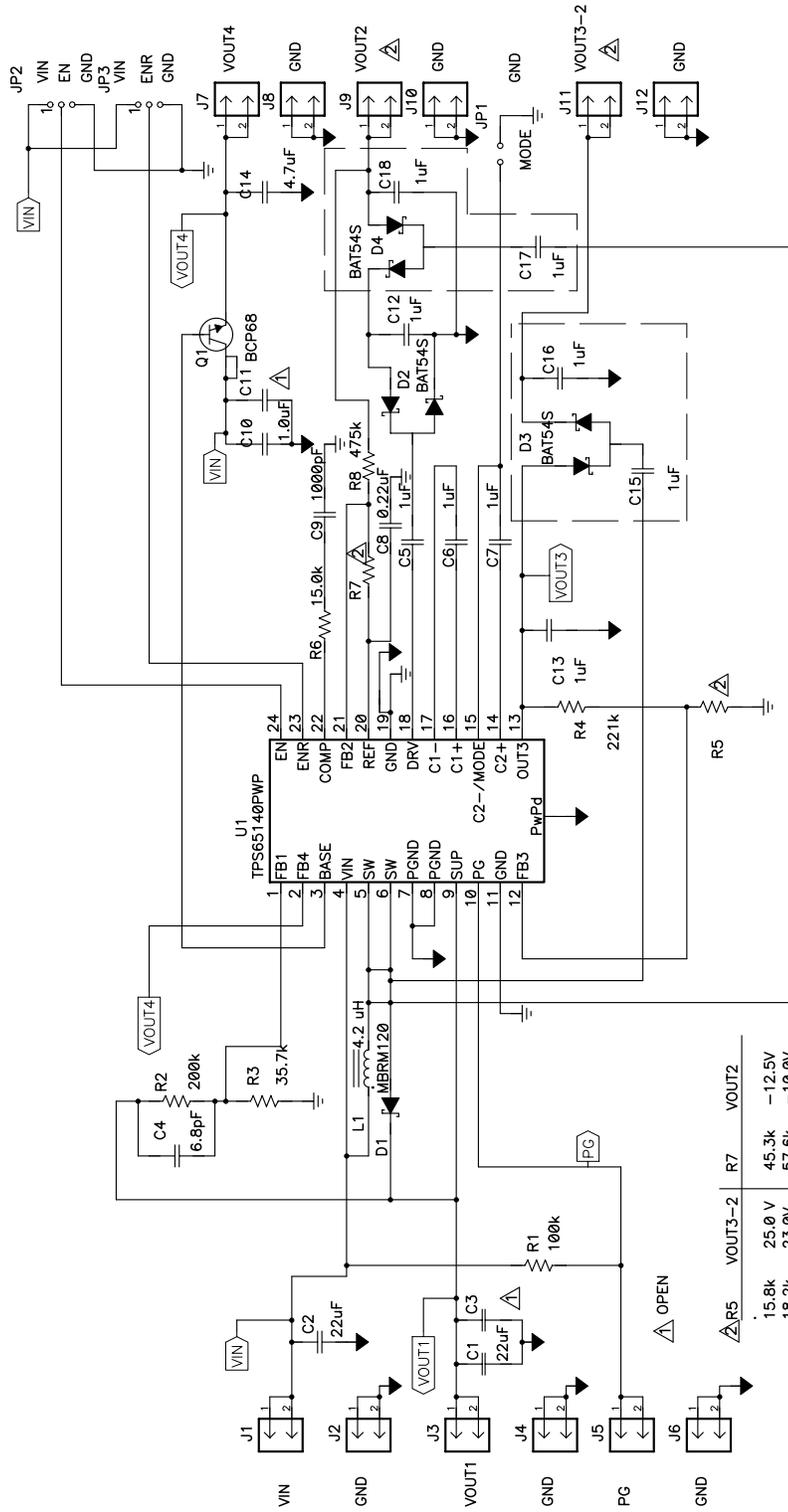


Figure 1. TPS65140EVM-031 Modified

	R5	VOUT3-2	R7	VOUT2
V	15.8k	25.0 V	45.3k	-12.5V
I	18.2k	23.0V	57.6k	-10.0V

Boosting the Positive Charge Pump ($V_{OUT3} > 3 * V_{OUT1}$)

In order to produce a quadrupled V_{OUT1} voltage (V_{OUT3-2}), an external charge pump stage is required to add the output voltage of the main boost converter (V_{OUT1}) on top of the output of positive charge pump (V_{OUT3}) configured as a tripler. As seen in Figure 1, the external charge pump is composed of two external capacitors, C15 and C16, and a small, dual Schottky diode, D3. Equation 2 computes the feedback resistors for the positive charge pump in tripler mode.

$$V_{OUT3-2} = V_{OUT3} + V_{OUT1} - V_{SCHOTTKY} = 1.214 * (1+R4/R5) + V_{OUT1} - V_{SCHOTTKY} \quad (2)$$

where $V_{SCHOTTKY} \sim 0.5 \text{ V}$.

C15, C16, and V_{OUT3} output capacitor C13 have all been sized at $1 \mu\text{F}$ in order to maximize the output current and minimize the output voltage ripple. Capacitance values as low as 220 nF can be used if lower output currents and higher output voltage ripple are acceptable. Figure 2 shows the load regulation for $V_{OUT3-2} = 25 \text{ V}$ and 23 V , given $V_{IN} = 3.3 \text{ V}$, $V_{OUT1} = 7.5 \text{ V}$ and $I_{OUT1} = 150 \text{ mA}$. Even though the external charge pump must be placed outside of the V_{OUT3} feedback loop for stability reasons, the measured load regulation for V_{OUT3-2} is still within 3% at $T_A = 25^\circ\text{C}$ for output currents well above 30 mA on each rail.

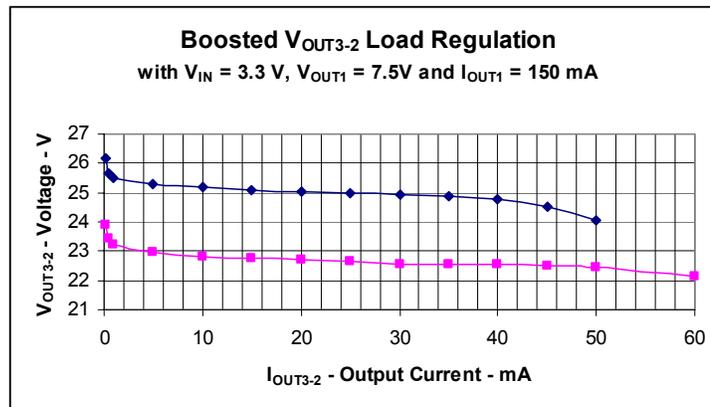


Figure 2. Load Regulation for V_{OUT3-2}

Lowering the Negative Charge Pump ($|V_{OUT2}| > V_{OUT1}$)

The TPS6510x and TPS6514x negative charge pump can only invert the output voltage of the main boost converter V_{OUT1} . An output voltage of $-2 * V_{OUT1} + V_{LOSSES}$ can be realized by adding an additional charge pump stage, composed of D4, C17, and C18 in Figure 1, inside the V_{OUT2} feedback loop. V_{LOSSES} includes the Schottky diode forward voltage drop plus internal charge pump driver R_{DSon} losses and is approximately 2.5 V . Because the additional charge pump stage is within the V_{OUT2} feedback loop, the same equations setting the negative charge pump output voltage (V_{OUT2}) as outlined in the TPS6510x/4x data sheet can be used. Capacitors C17, C18, and C12 have been sized at $1 \mu\text{F}$ in order to maximize the output current and minimize the output voltage ripple. Capacitance values as low as 220 nF can be used if lower output currents and higher output voltage ripple are acceptable. Figure 3 shows the load regulation for $V_{OUT2} = -10 \text{ V}$ and -12.5 V , given $V_{IN} = 3.3 \text{ V}$, $V_{OUT1} = 7.5 \text{ V}$, and $I_{OUT1} = 150 \text{ mA}$.

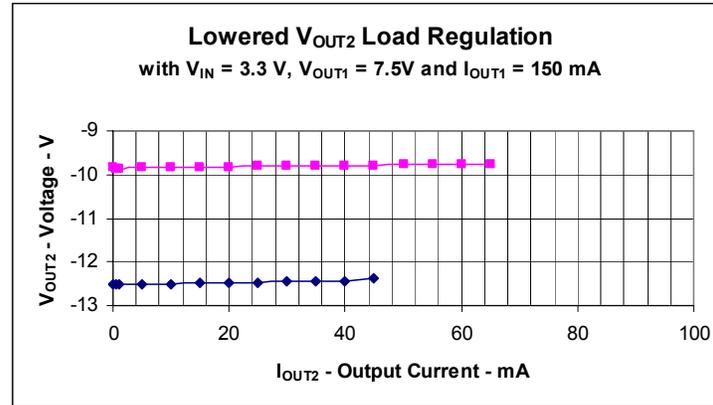


Figure 3. Load Regulation for Lowered V_{OUT2}

Modifying the Power-Up Sequencing

Pulling EN high on the TPS6510x and TPS6514x starts the internal power-up sequencing with the main boost converter coming up first, followed by the negative positive charge pump, and the positive charge pump. Adding the circuit in Figure 4 to V_{OUT1} of Figure 5, not only changes the order of the sequencing but also provides an adjustable sequencing delay. In addition, because the MOSFET Q3 is driven by the power-good signal, this circuit provides short circuit protection and input-to-output disconnect for the V_{OUT1} rail. When all of the output rails of the TPS65140 are within regulation, the power-good signal (PG), pulled high to $V_{IN} = 3.3\text{ V}$ through a 100-k Ω resistor, goes high and turns on Q2. This starts the RC delay circuit that eventually turns on Q3. The voltage divider formed by resistors R9 and R10 is configured so that Q3 turns on (but not with enough voltage to exceed Q3's maximum source to gate voltage rating). Recommended components include FDN360P or SI2343 for Q3 and MMBT3904 for Q2. The turnon delay for Q3 is implemented by C25 and R9. R10 is used to hold the gate of Q3 off during device shutdown. Equation 3 shows the approximate delay before Q3 turns on.

$$t_{dly} \sim -R9 \times C19 \times \ln(1 - |V_{TH}|/V_{OUT1}) \quad (3)$$

Where V_{TH} is the threshold voltage of Q3.

In this example, using $|V_{TH}| = 0.95\text{ V}$, $t_{dly} = 3\text{ ms}$. Figure 5 shows the circuit in practice.

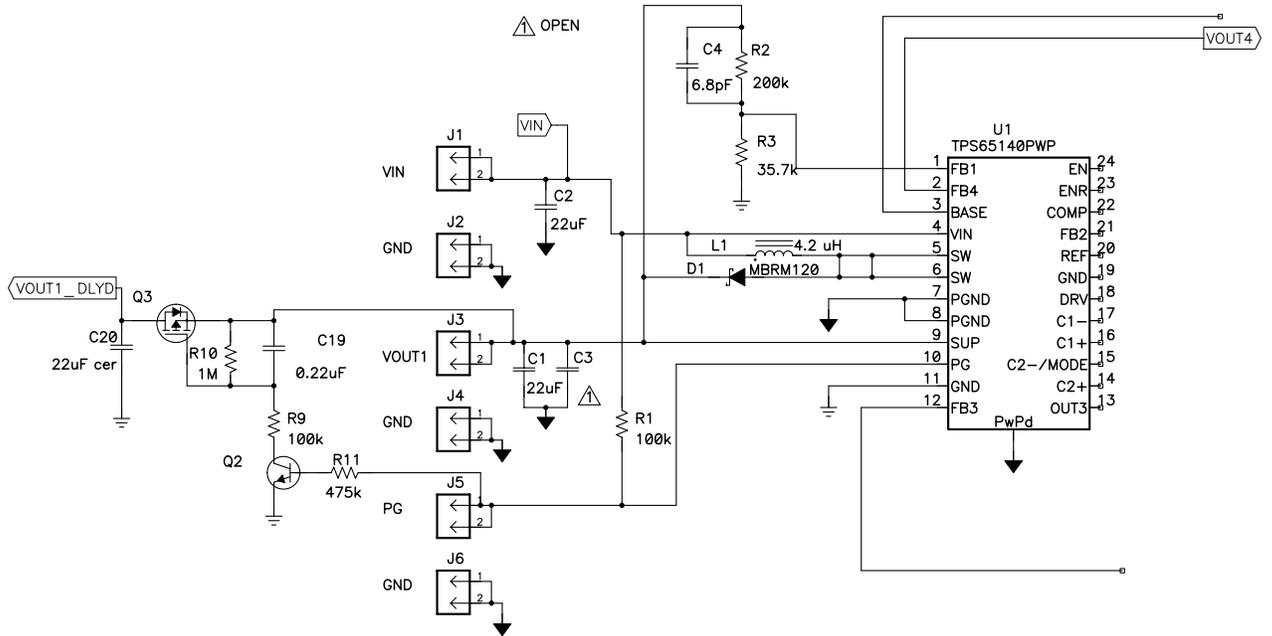


Figure 4. Example Delay Circuit

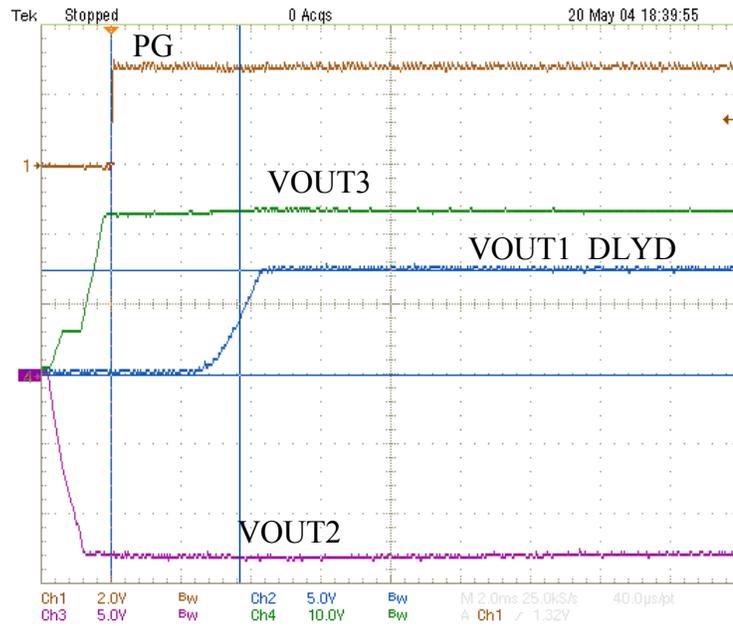


Figure 5. Modified Start-Up Using Delay Circuit

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