TEXAS INSTRUMENTS

TPS6010x/TPS6011x Charge Pump

Application Report

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Contents

List of Figures

List of Tables

TPS6010x/TPS6011x Charge Pump

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ABSTRACT

Charge pumps are dc/dc converters that use a capacitor instead of an inductor or transformer for energy storage. They are able to generate positive or negative voltages from the input voltage. The input voltage can be multiplied by some factor such as 0.5, 2, 3, and so on, to generate the output voltage desired. Often, charge pumps and all related parts (including those used for energy storage) are integrated in some other circuits, such as some PLL devices where a negative voltage is required. Integrated charge pumps can only supply a small amount of current due to the limitation in the size of integrated capacitors. If more current is needed, a dc/dc converter is required with sufficient energy storage capacity to handle this higher current. This requires the use of some external components.

Most charge pumps have had the disadvantage of having an unregulated output voltage that was simply the input voltage multiplied by some factor. The first TI™ charge pump family, the TPS6010x/TPS6011x, is a family of regulated charge pumps with different output voltages and different output current versions up to 300 mA. Only four external components are necessary to generate this high current. The TPS6010x parts have a regulated output voltage of 3.3V, and the TPS6011x devices provide 5 V. The output voltage is very precise due to special circuit design and shows only a very small ripple.

This application report is a detailed description of the use of TI's TPS6010x and TPS6011x charge pump devices. It includes the basic operation of the charge pumps, a detailed description of the features of the TPS6010x/TPS6011x devices, the requirements and best choice of external components, the recommended layout, and some design examples.

1 Basic Operation of the Architecture Used

The charge pumps used in TI's family of TPS6010x/TPS6011x double the input voltage but, because the input voltage can have a wide range of variation, the output voltage is regulated. This section first describes the basic function of a charge pump doubling the input voltage; it then shows the specific integrated charge pumps and their regulation circuits.

1.1 Charge Pump as Voltage Doubler

Figure 1 shows the principle of a charge pump doubling the input voltage.

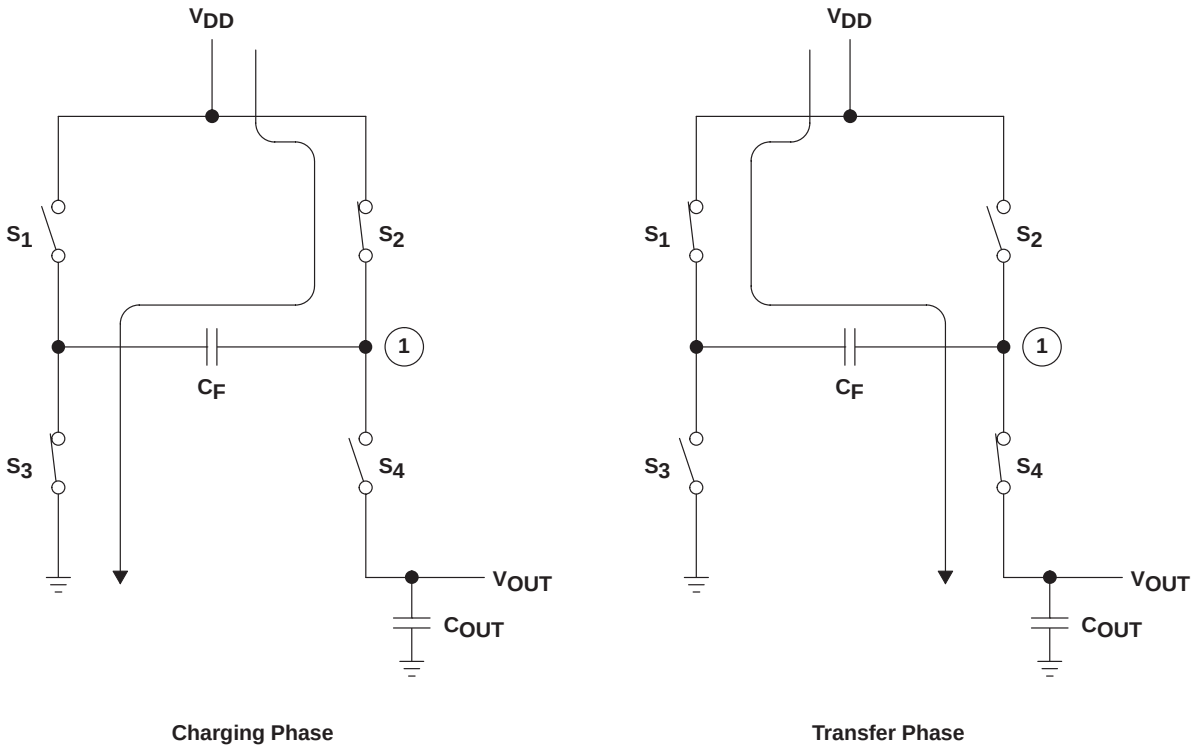

Figure 1. Basic Charge Pump Configured as a Voltage Doubler

The oscillator runs at a 50% duty cycle and regulates the turning on and off of the four switches. During the first half of the oscillator frequency period (charging phase), switches S_2 and S_3 are closed, and switches S_1 and S_4 are opened. The flying capacitor (C_F) is charged (ideally up to V_{DD}). During the second half (transfer phase) switches S_2 and S_3 are opened, and switches S_1 and S_4 are closed. Capacitor C_F is discharged and charges the output capacitor (C_{OUT}). The voltage at this moment at node 1 is ideally:

$$V_1 = V_{DD} + V_{CF} \approx 2 \times V_{DD}.$$

Therefore, the output capacitor (C_{OUT}) will ideally be charged up to $2 \times V_{DD}$ after reaching the steady state. The real voltage at C_{OUT} will be a little less than $2 \times V_{DD}$ because of losses in the switches and charging losses in capacitor C_F. So the output voltage for this configuration only depends on the input voltage and on the losses in the switches and in the capacitor C_F.

1.2 Regulated Charge Pumps in the TPS6010x/TPS6011x Family

The two charge pumps in the TPS6010x/TPS6011x family are basically working as voltage doublers with a regulated output voltage. The TPS6010x devices have an output voltage of 3.3 V ±4% over the whole input-voltage range, and the TPS6011x devices have an output voltage of 5V ±4% over the whole input-voltage range. Figure 2 shows the functional block diagram of the TPS6010x/TPS6011x family. Two separate charge pumps are integrated to get a very small ripple at the output. All the other blocks are required to control the different modes and to regulate the output voltage. The different modes are shown in Sections 1.2.1 through 1.2.6. Refer to the data sheets for a more detailed description.

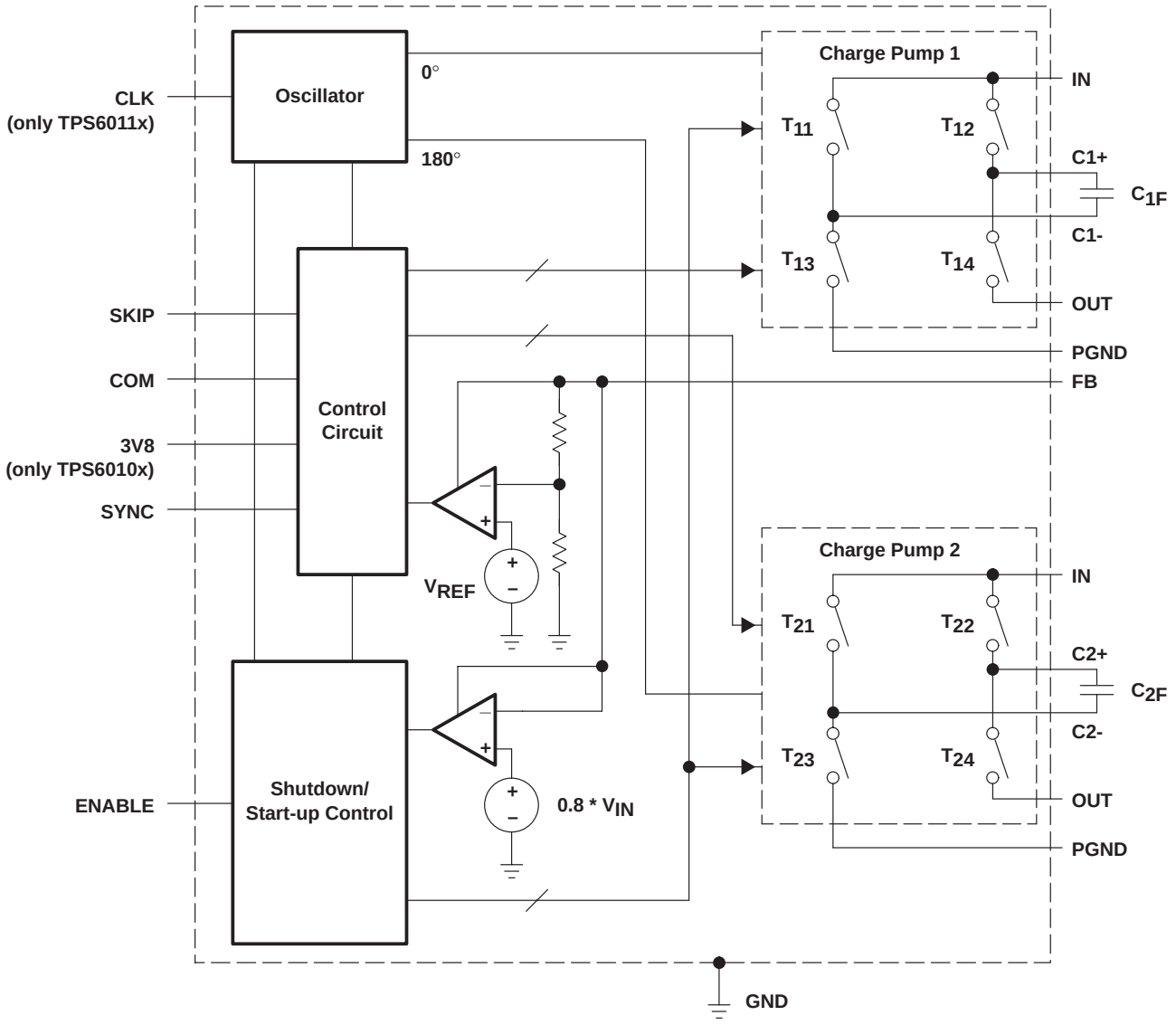

Figure 2. Functional Block Diagram, TPS6010x/TPS6011x Charge Pumps

At start-up, when all capacitors are discharged, the shutdown/start-up control circuit starts charging the output capacitor (C_{OUT}) up to $0.8 \times V_{IN}$ to reduce the start-up time and to eliminate the need for a Schottky diode between IN and OUT. Therefore, during shutdown the input and output are disconnected. The advantage with very light loads like the MSP430 is that the charge pump can be disabled and the load can be supplied by the output capacitor during this time. The quiescent current can be reduced with this operation mode. The control circuit controls the different modes of the device. All the possible modes and their use under different requirements are described in the following sections.

1.2.1 Push-Pull Mode (GND at pin COM)

The two charge pumps work in push-pull mode for minimum ripple, that is, in each half of an oscillator cycle one of the charge pumps is charging the respective flying capacitor (C_{Fx}), and the other one is charging the output capacitor (C_{OUT}). Therefore, the two charge pumps operate with a phase shift of 180°.

1.2.2 Single-Ended Mode (V_{IN} at pin COM)

If output ripple is not too critical, the device can work without phase shift between the two charge pumps, and the number of external components can be reduced by one flying capacitor.

1.2.3 Constant-Frequency Mode (GND at pin SKIP)

In constant-frequency mode, the ripple at the output is minimized because the output capacitor (C_{OUT}) is charged during each oscillator cycle. The unwanted output power has to be dissipated in the device. This decreases the efficiency for light loads in comparison to pulse-skip mode. The advantage is the defined spectrum.

1.2.4 Pulse-Skip Mode (V_{IN} at pin SKIP)

The device can also run in pulse-skip mode for optimized efficiency at light loads. In this mode, the charging of the output capacitor takes place only if the output voltage drops below a defined threshold. The efficiency for light loads increases, but the output ripple is higher than in push-pull mode.

1.2.5 3.3-V Mode (GND at pin 3V8) and 3.8-V Mode (V_{IN} at pin 3V8)

In comparison with the TPS6011x, the TPS6010x provides one additional mode: the 3.8-V mode. Although it is possible to minimize the output ripple with the combination of push-pull and constant-frequency modes, the reduction might not be enough. Additionally, the output of the TPS6010x may be too far from where the power is needed, and this long distance can cause EMI problems on the power pin of the supplied device. To improve the described behavior, the additional 3.8-V mode is implemented. In this mode, the regulated output voltage is increased to 3.8 V. A linear voltage regulator can then be connected with the output of the charge pump to smooth the output voltage. The efficiency of this solution is nearly the same as with the charge pump alone because the TPS6010x is doubling the input voltage and dissipating the unwanted power.

1.2.6 Synchronization (V_{IN} at pin SYNC)

It is also possible to synchronize the device externally with a frequency below 800 kHz. The input at the SYNC pin has to be a high signal, and the frequency signal has to be connected to pin 3V8 in the TPS6010x, or to CLK in the TPS6011x. The charge pumps operate now at half the external frequency. The only requirements on the external signal source are a duty cycle between 20% and 80%, and the proper signal levels.

2 TPS6010x/TPS6011x Operation Modes

The TPS6010x/TPS6011x family of charge pumps from Texas Instruments includes different modes to optimize the device for specific applications. This section describes the functionality of the devices at start-up and normal operation.

The behavior of the output is dependent on the layout, and on the external capacitors. The measurements in this section are taken on the layout recommended in the data sheet. Table 1 shows the values of the capacitors used during the measurements. For different capacitors please refer to Section 3.

All measurements in this section are made at room temperature.

Table 1. Capacitors Used for the Different Devices

LOCATION	TPS60100	TPS60101	TPS60110	TPS60111
Input (IN) capacitors	Sprague 10 µF/10 V, Taiyo Yuden 1 µF/16 V	Sprague 10 µF/10 V, Taiyo Yuden 1 µF/16 V	Sprague 15 µF/10 V, Taiyo Yuden 1 µF/16 V	Sprague 15 µF/10 V, Taiyo Yuden 1 µF/16 V
Output (OUT) capacitors	Sprague 22 µF/20 V, Taiyo Yuden 1 µF/16 V	Sprague 22 µF/20 V, Taiyo Yuden 1 µF/16 V	Sprague 33 µF/20 V, Taiyo Yuden 1 µF/16 V	Sprague 33 µF/20 V, Taiyo Yuden 1 µF/16 V
Flying capacitors (C_{xF})	Taiyo Yuden 2.2 µF/16 V	Taiyo Yuden 2.2 µF/16 V	Taiyo Yuden 2.2 µF/16 V	Taiyo Yuden 2.2 µF/16 V

2.1 Start-Up Behavior of the Devices With Full and Light Resistive Loads

The most important part of the start-up behavior is the charging of the output capacitors (C_{OUT}), which is nearly independent of the different modes. Only the start-up behavior for push-pull, constant-frequency modes operating with the internal oscillator is shown.

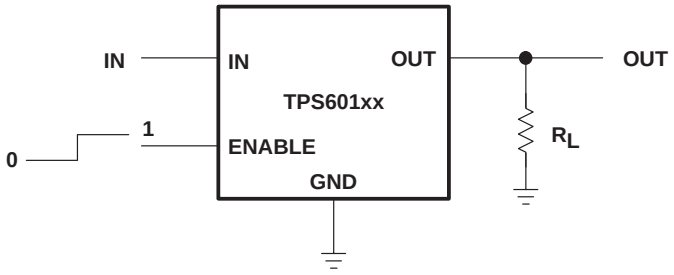

Figure 3. Evaluation Circuit for Start-Up Behavior

During the measurements, the supply voltage (V_{IN}) is constantly applied (2.4 V for TPS6010x, and 3 V for TPS6011x). The device is enabled and driven into start-up by applying the supply voltage to the ENABLE pin. The output capacitors (C_{OUT}) are discharged. The diagrams also show the minimum duration for the ENABLE signal to get a stable output voltage. All measurements in this section use a resistive load. The start-up behavior with capacitive and/or inductive loads is discussed in Section 2.2.

2.1.1 TPS60100 Start-Up Behavior

For the TPS60100, a 16.5-Ω resistor is used for full load, and a 330-Ω resistor is used for light load. After start-up, these resistive loads handle a 200-mA current for full load, and 10 mA for light load.

Figures 4 through 7 show that the output voltage is stable after the latest 500 µs under these conditions.

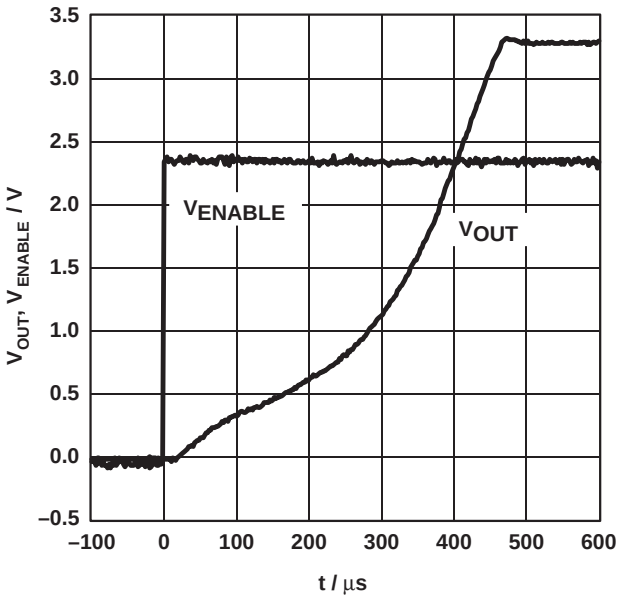

Figure 4. TPS60100: Start-Up With Full Load to 3.3 V

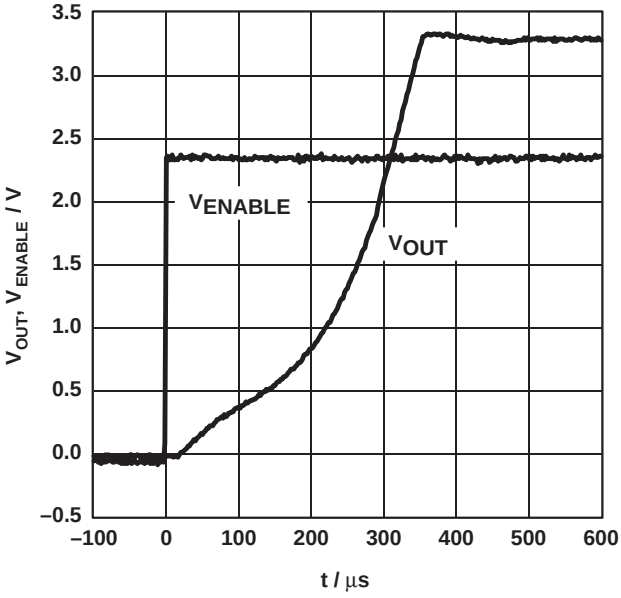

Figure 5. TPS60100: Start-Up With Light Load to 3.3 V

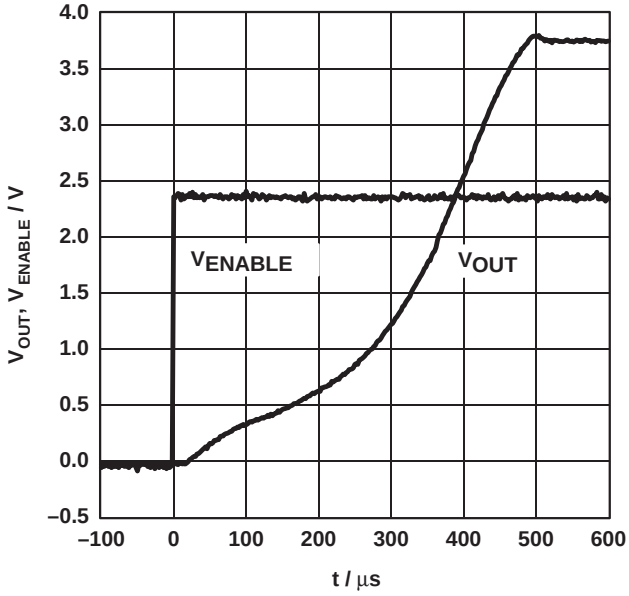

Figure 6. TPS60100: Start-Up With Full Load to 3.8 V

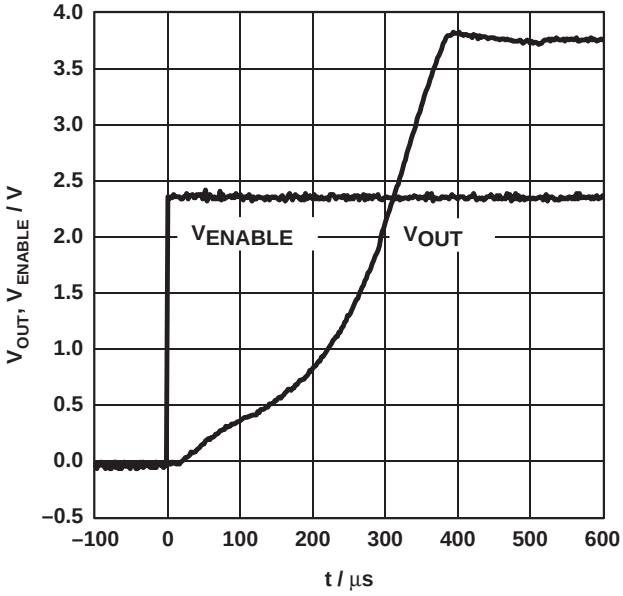

Figure 7. TPS60100: Start-Up With Light Load to 3.8 V

2.1.2 TPS60101 Start-Up Behavior

For the TPS60101, a 33-Ω resistor is used for full load, and 330 Ω for light load. After start-up, these resistive loads handle a current of 100 mA for full load, and 10 mA for light load.

Figures 8 through 11 show that the output voltage is stable after the latest 450 µs under these conditions.

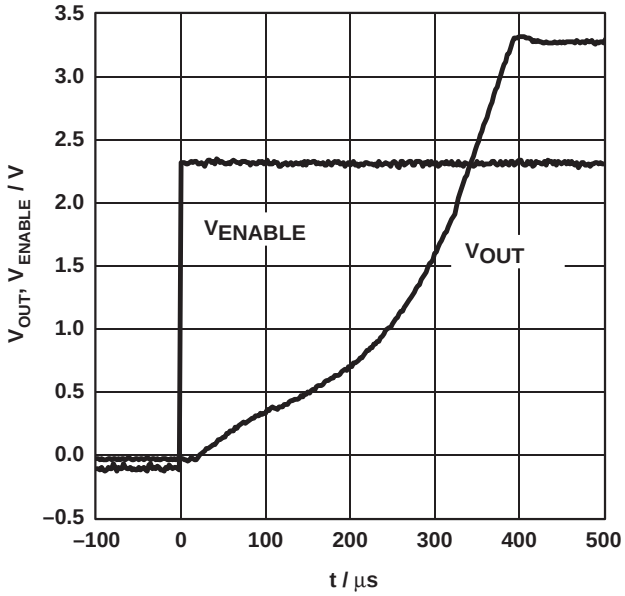

Figure 8. TPS60101: Start-Up With Full Load to 3.3 V

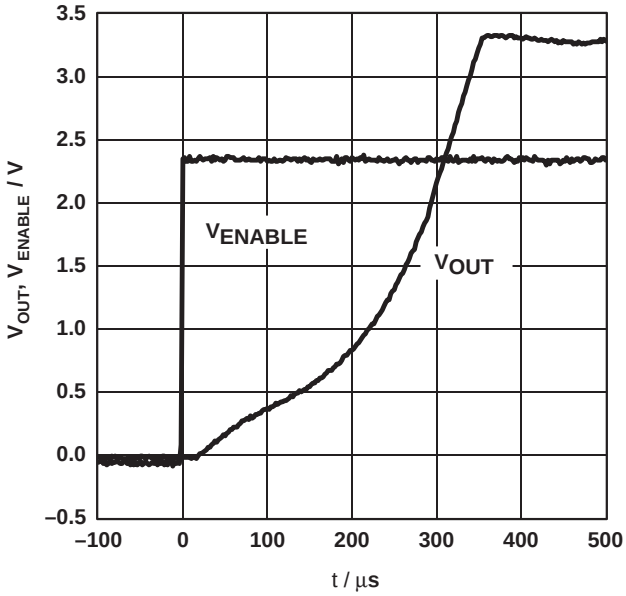

Figure 9. TPS60101: Start-Up With Light Load to 3.3 V

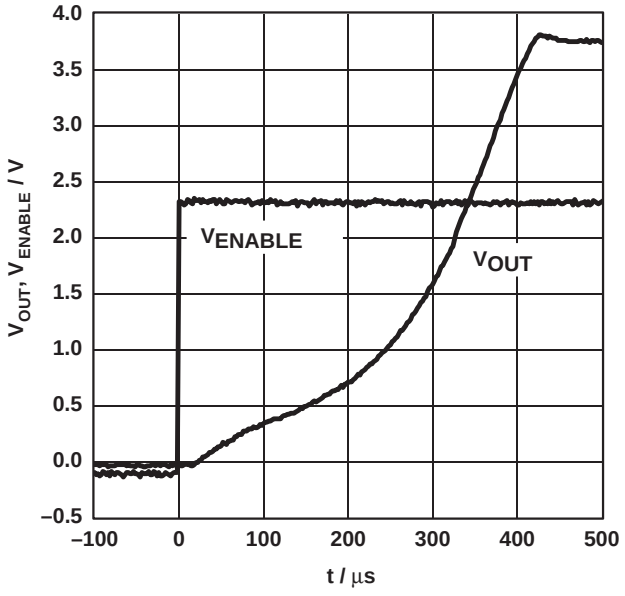

Figure 10. TPS60101: Start-Up With Full Load to 3.8 V

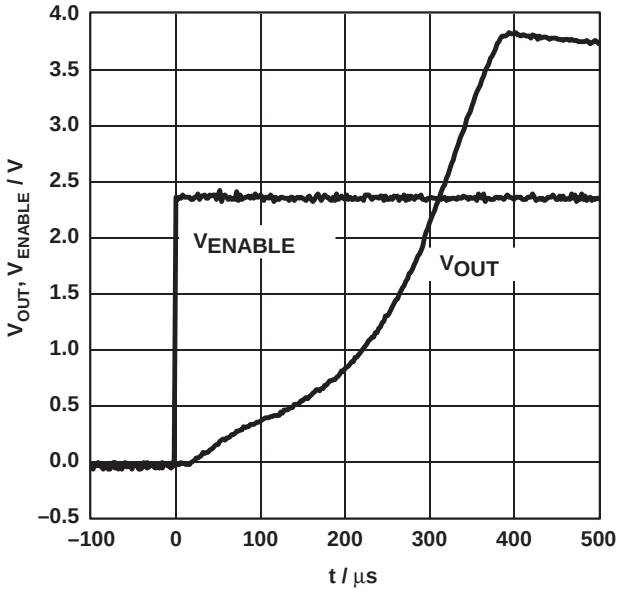

Figure 11. TPS60101: Start-Up With Light Load to 3.8 V

2.1.3 TPS60110 Start-Up Behavior

For the TPS60110, a 16.7-Ω resistor is used for full load, and a 500-Ω resistor for light load. After start-up, these resistive loads handle a current of 300 mA for full load, and 10 mA for light load.

Figure 12 shows that the output voltage is stable after the latest 900 μs with full load, at room temperature, and with an input voltage (V_{IN}) of 3 V.

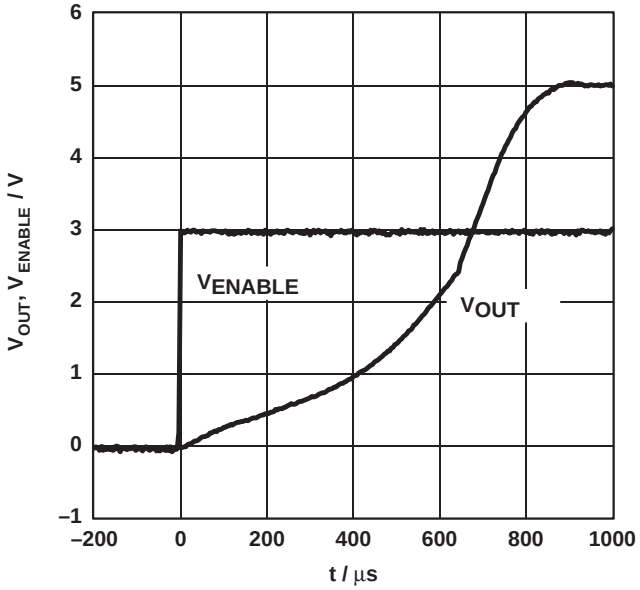

Figure 12. TPS60110: Start-Up With Full Load to 5 V

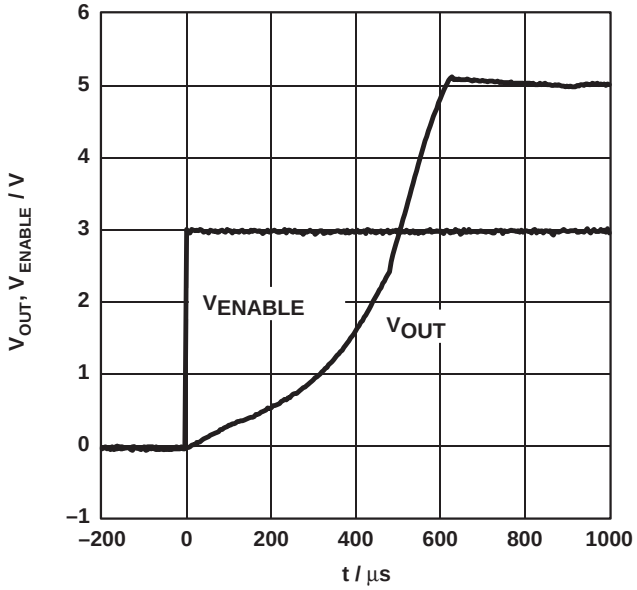

Figure 13. TPS60110: Start-Up With Light Load to 5 V

2.1.4 TPS60111 Start-Up Behavior

For the TPS60111, a 33.3-Ω resistor is used for full load, and a 500-Ω resistor is used for light load. After start-up, these resistive loads handle a current of 150 mA for full load, and 10 mA for light load.

Figure 14 shows that the output voltage is stable after the latest 750 μs.

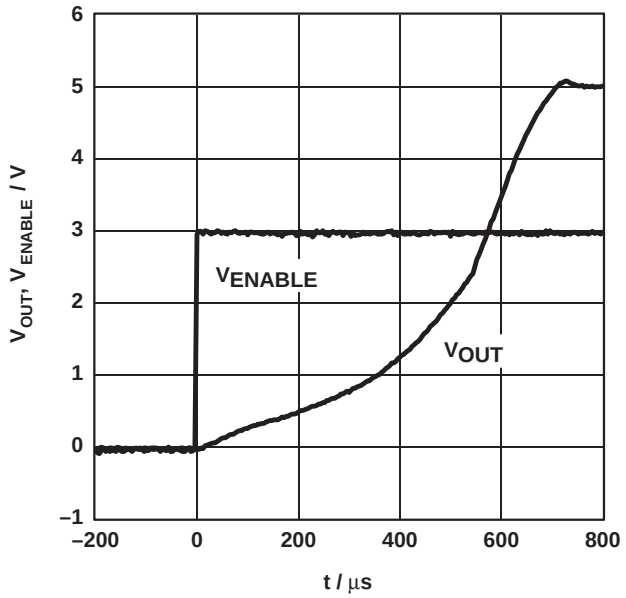

Figure 14. TPS60111: Start-Up With Full Load to 5 V

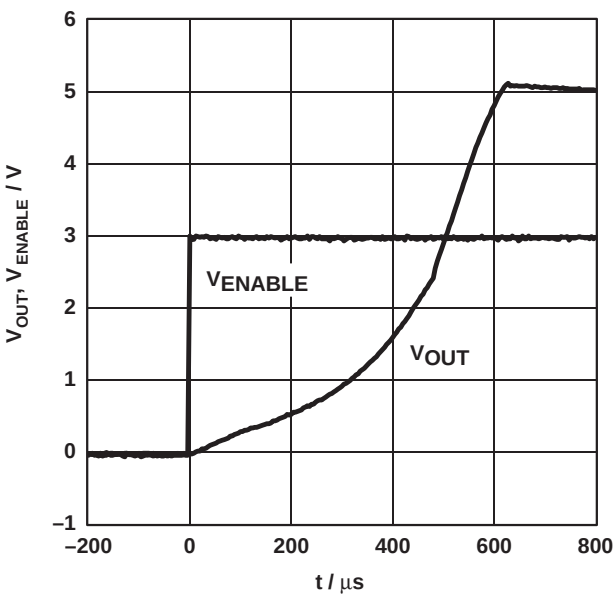

Figure 15. TPS60111: Start-Up With Light Load to 5 V

Figures 4 through 15 show that first the start-up circuit controls the operation until the output voltage (V_{OUT}) reaches $0.8 \times V_{IN}$. During this time period the device limits the supply current to charge the output capacitors. This means that with increasing output voltage the supply current increases nonlinearly. When $V_{OUT} = 0.8 \times V_{IN}$ is exceeded, the device switches to standard operation as defined by the different mode inputs, that is, the flying capacitors charge the output capacitor.

The previous measurements show that a maximum of 1 ms after applying the ENABLE signal, the output voltage becomes stable at room temperature for the given input voltage.

2.2 Start-Up Behavior Under Different Loads

Section 2.1 describes the start-up behavior for resistive loads only. In real applications the loads are generally not simply resistive. Block capacitors, filter inductors, processors, or other load combinations can be found. This section covers the behavior of the TPS6010x/TPS6011x for some combinations of capacitive, resistive, and inductive loads. The input voltage for the TPS6010x is 2.4 V, and 3 V for the TPS6011x.

2.2.1 Capacitive Loads in Parallel With Resistive Loads

Figures 17 and 18 show the start-up behavior of TPS60100 and TPS60110 with full load (resistive, TPS60100: 16.5 Ω, TPS60110: 16.7 Ω) plus an additional capacitor of 100 μF in parallel.

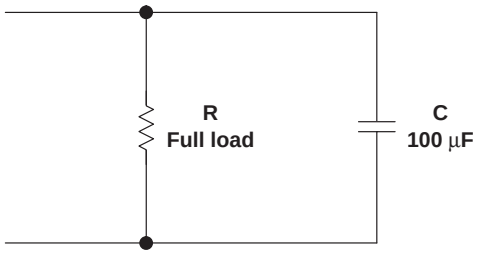

Figure 16. Load Circuit for Capacitive Loads in Parallel

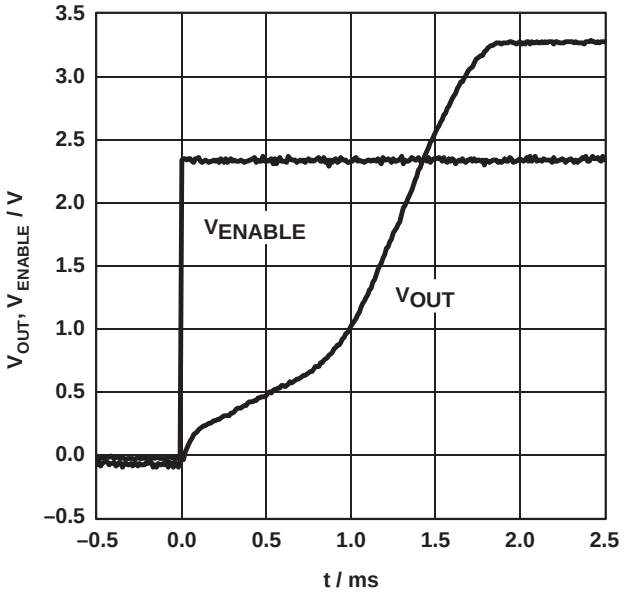

Figure 17. Start-Up of TPS60100 With the RC Network in Figure 16

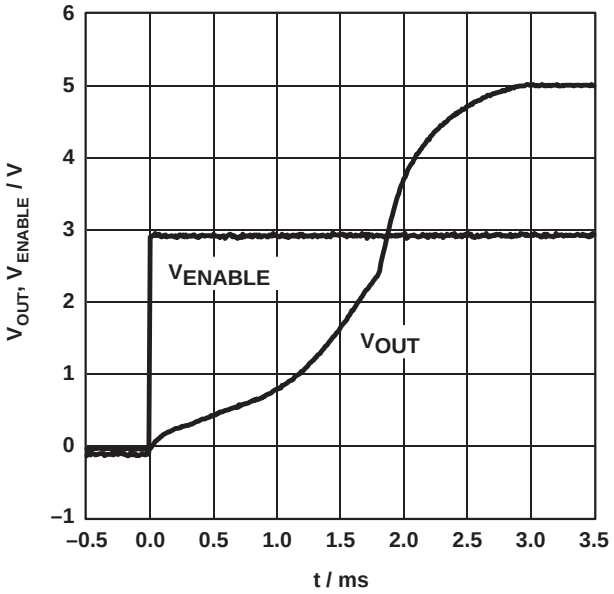

Figure 18. Start-Up of TPS60110 With the RC Network in Figure 16

In the case of resistive plus capacitive loads, the behavior of the device is similar to the pure resistive load. The start-up circuitry of the device controls the operation until $V_{OUT} > 0.8 \times V_{IN}$. Afterwards the device switches to standard functionality and charges the output capacitors with the flying capacitors. Increasing the value of the capacitive load increases the duration until the output voltage is stable.

2.2.2 Additional Inductive and Capacitive Loads

Figures 20 and 21 show the start-up behavior of TPS60100 and TPS60110 with the load circuitry shown in Figure 19. The resistor represents full load for the devices (TPS60100: 16.5 Ω, TPS60110: 16.7 Ω).

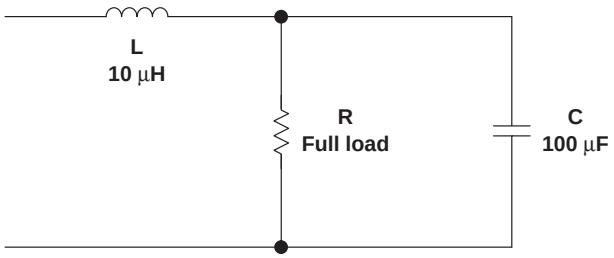

Figure 19. Load Circuit for RLC Loads

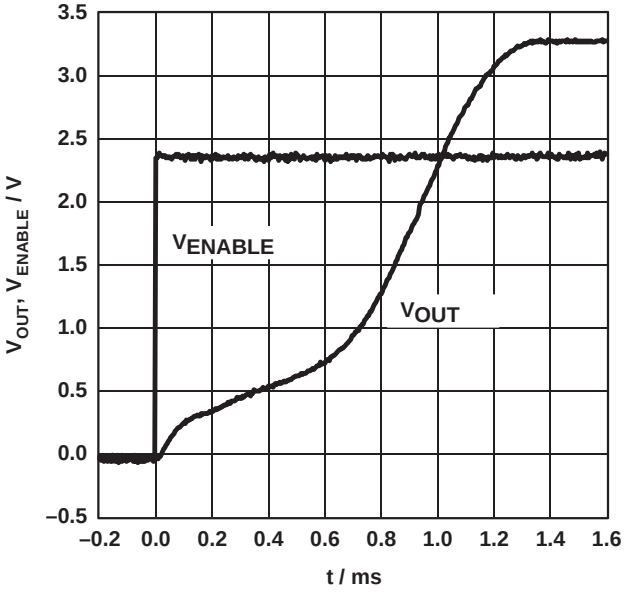

Figure 20. Start-Up of TPS60100 With the RLC Network in Figure 19

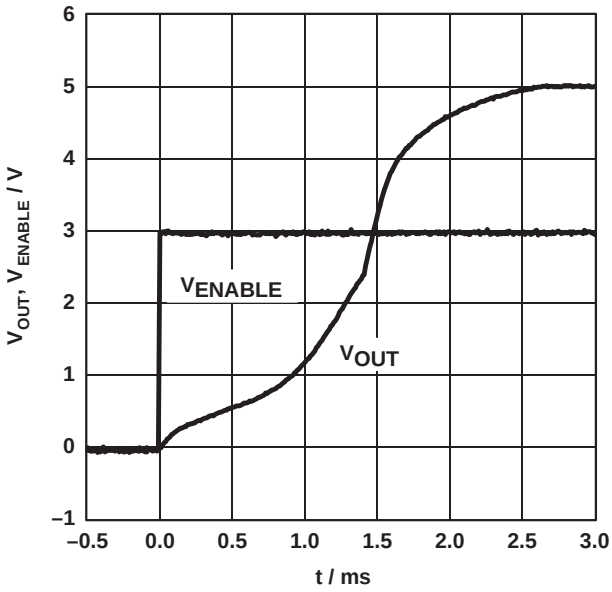

Figure 21. Start-Up of TPS60110 With the RLC Network in Figure 19

For resistive plus capacitive and inductive loads, the device behaves similar to a resistive load. The device is controlled by the start-up circuitry until $V_{OUT} > 0.8 \times V_{IN}$. Afterwards the device charges the output capacitors in standard operation mode.

2.3 Short-Circuit Protection

The devices are short-circuit, but *not overload* protected. The current is limited during a *hard* output short-circuit (V_{OUT} = 0 V). For the TPS6010x, the output short-circuit current is typically 125 mA; this current is typically 150 mA for the TPS6011x. This is due to the structure of the device. During start-up, the device is working like a fold-back circuit; that is, when the output voltage increases, the output current increases faster than linearly. For a hard short-circuit, the output voltage is zero and the device is in the start-up behavior ($V_{OUT} << V_{IN}$); these two factors limit the current to a typical value of 125 mA/150 mA. *With overload, however, the temperature increases and can destroy the device*.

2.4 Spectrum of the Different Modes Under Light and Full Load

The spectrum of the output voltage is dependent on the output current and on the operating mode of the device. This section shows the TPS60100 spectrum for some modes under light and full load. The light load is a 330-Ω resistor, and the full load is 16.5 Ω.

2.4.1 Push-Pull, Constant-Frequency, 3.3 V, and Using the Internal Oscillator

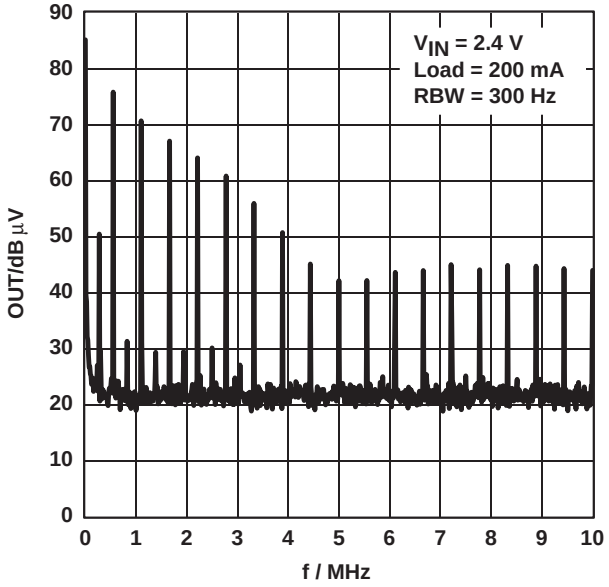

Figure 22. TPS60100: Spectrum for Full Load in Constant-Frequency Mode

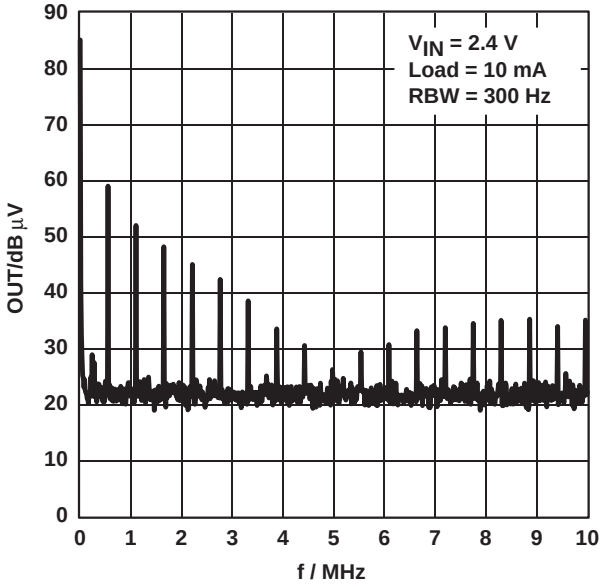

Figure 23. TPS60100: Spectrum for Light Load in Constant-Frequency Mode

2.4.2 Push-Pull, Pulse-Skip, 3.3 V, With Internal Oscillator

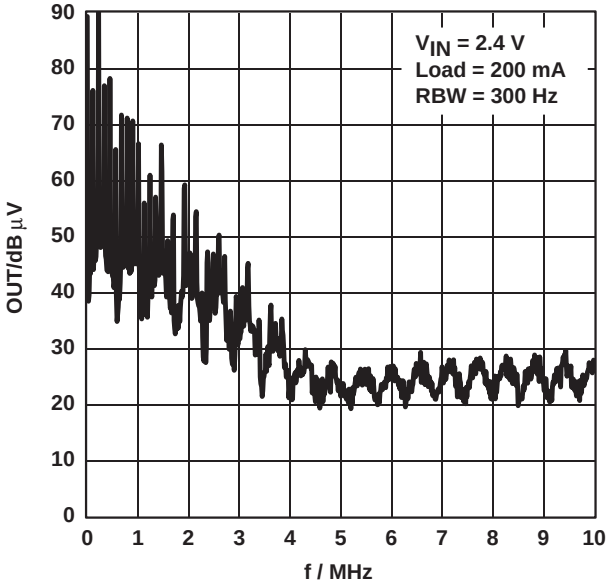

Figure 24. TPS60100: Spectrum for Full Load in Pulse-Skip Mode

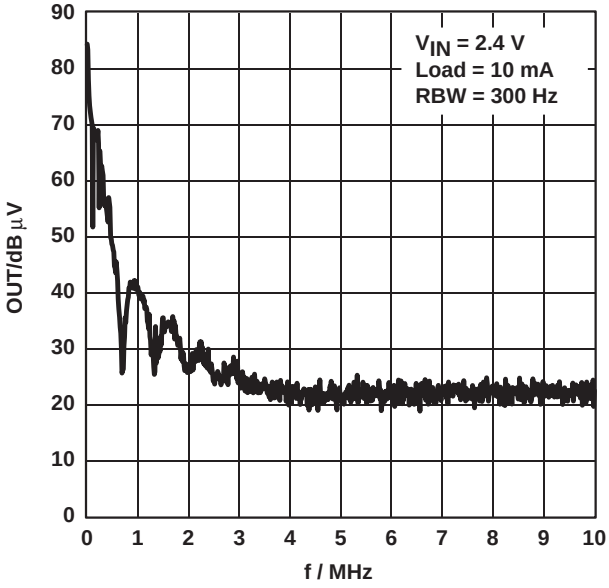

Figure 25. TPS60100: Spectrum for Light Load in Pulse-Skip Mode

2.5 Switching Between Modes

This section shows what happens with the output voltage when the mode is changed during operation (the device is constantly enabled and using the internal oscillator). First, the TPS6010x/TPS6011x is enabled, operates in push-pull mode, and works at a fixed frequency with an output voltage of 3.3 V. The control pins COM, SYNC, SKIP, and 3V8 are pulled to GND and the ENABLE pin is pulled to high level. The maximum resistive load is applied during all the tests. The input voltage of the devices is 2.4 V for TPS60100 and 3 V for TPS60110. To test the possibility of changing the logic signals on the fly, a function generator is connected to one of the pins COM, SKIP, or 3V8 (for TPS60100 only). The two other pins remain connected to GND. The signal is a 1-kHz rectangular wave with either 2.4-V or 3-V amplitude.

Only TPS60100/TPS60110 are shown for all mode changes because the differences between TPS60100 and TPS60101, and TPS60110 and TPS60111 are negligible. The mode change between 3.3 V and 3.8 V is shown only for TPS60100; the TPS6011x has only one output voltage option.

2.5.1 Push-Pull Versus Single-Ended Mode

The push-pull mode minimizes the output ripple. The two charge pumps operate in anti-phase, that is, while one is charging the respective flying capacitor (C_{XF}) (charging phase), the other one is charging the output capacitor (C_{OUT}) (transfer phase). Therefore, the ripple in this mode is less than 20 mV using tantalum capacitors (for the capacitors on the EVMs, see Table 1). In single-ended mode both charge pumps are working in phase. During one half of the period the flying capacitor (C_{XF}) (or with the measurement equipment used, both flying capacitors) is charged (both charge pumps are in the charge phase); in the second half of the period the output capacitor (C_{OUT}) is charged (both charge pumps are in transfer phase). The ripple depends on the capacitance of the output capacitor and on its equivalent series resistance (ESR), because the capacitor provides the output current during one half of a period.

The COM pin is connected to a function generator to switch between the modes on the fly. Figures 26 and 27 show that there is almost no change in the average output voltage, even though the devices are operating only for a short period of time in push-pull or in single-ended mode. For the TPS60100, the average output voltage increases by 40 mV; for the TPS60110, the average output voltage decreases by 20 mV.

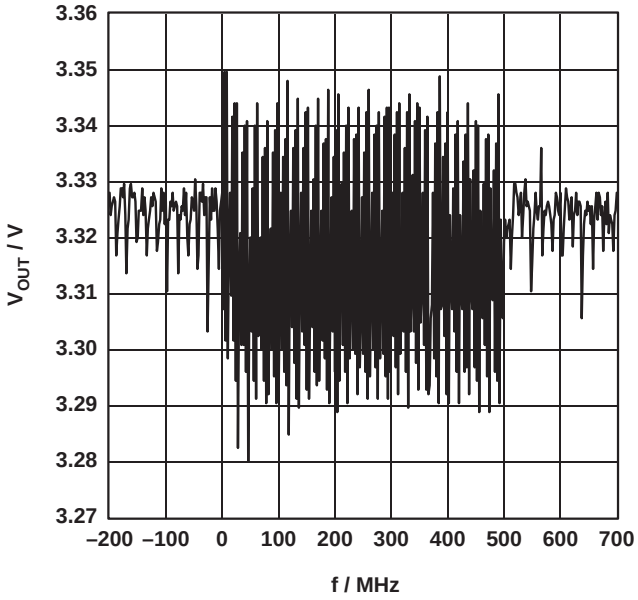

Figure 26. V_{OUT} for TPS60100, Push-Pull to Single-Ended

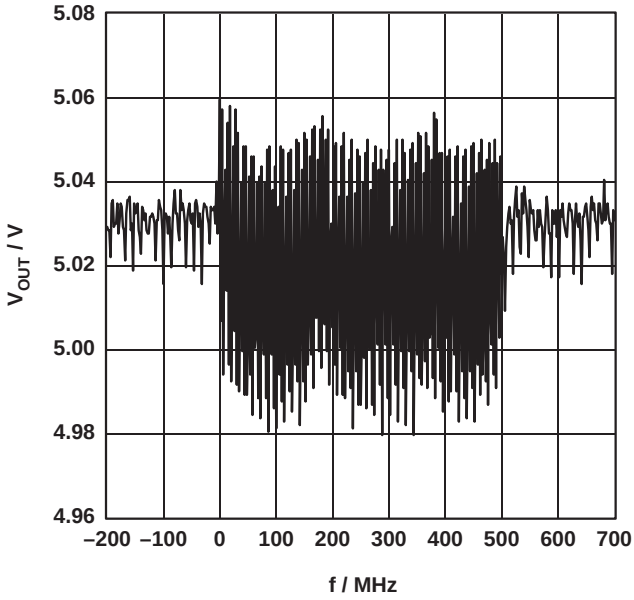

Figure 27. V_{OUT} for TPS60110, Push-Pull to Single-Ended

2.5.2 Constant-Frequency Versus Pulse-Skip Mode

In constant-frequency mode, the output capacitor (C_{OUT}) is charged during each oscillator cycle regardless of the load current. This leads to a lower efficiency for light loads because the unwanted power has to be dissipated in the package. The advantage of this mode is the lower electromagnetic interference (EMI) because the device works with only one specific operating frequency. This simplifies the filtering of the output signal.

In pulse-skip mode, the output capacitor (C_{OUT}) is only charged when needed. The regulation is equivalent to a two-point regulation. If the output voltage is below 3.3 V (TPS6010x), or 5 V (TPS6011x), the charge pump starts operating until the output voltage is above this threshold. The charge pump requires minimal power as long as the output voltage is above the threshold . During this time period, pulses are skipped and the output (OUT) is disconnected from the input (IN). For light loads, the efficiency increases in comparison with the constant-frequency mode. The filtering of the output signal is more complicated than in constant-frequency mode because the frequency is not fixed.

The SKIP pin is connected to the function generator. Figures 28 and 29 show that there is nearly no change in the average output voltage, even though the device is operating only for a short period of time (500 μs) in constant-frequency or in pulse-skip mode. The average output voltage decreases by about 10 mV. The TPS60110 shows an overshot of about 20 mV when the mode changes from pulse-skip to constant-frequency. For this case, the charge in the flying capacitors is higher than it would be in constant-frequency mode (they were charged in pulse-skip mode).

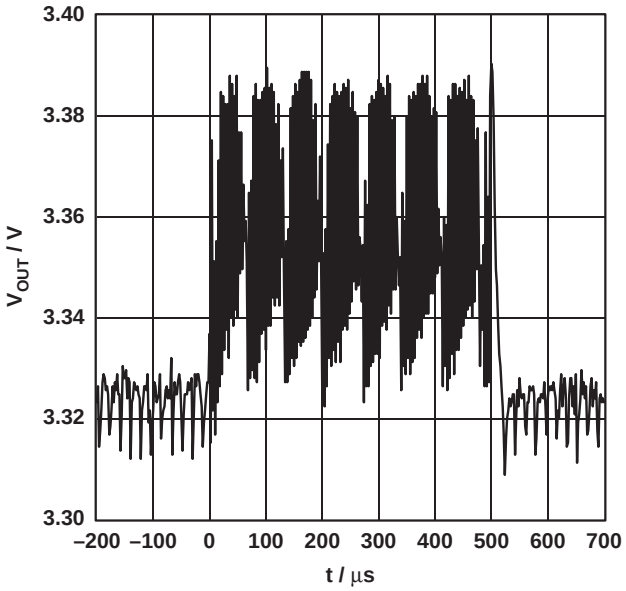

Figure 28. V_{OUT} for TPS60100, Constant-Frequency to Pulse-Skip

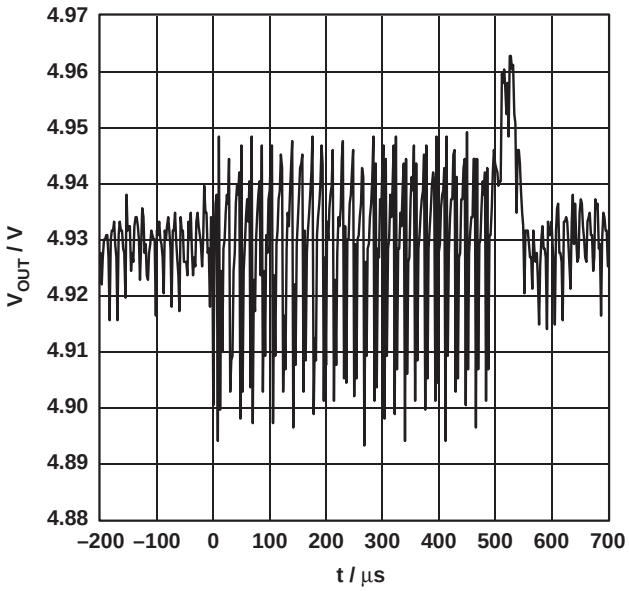

Figure 29. V_{OUT} for TPS60110, Constant-Frequency to Pulse-Skip

2.5.3 Switching Between 3.3 V and 3.8 V Mode

The output voltage of the TPS6010x can be set to either 3.3 V or 3.8 V with pin 3V8 . Although this is not a typical operating condition, it was verified that no problem occurs if these modes are changed on the fly. Starting from 3.3 V, the output voltage needs up to 150 μs to reach 3.8 V. From 3.8 V down to 3.3 V, the rate of decrease is dependent on the load. The rate of increase is nearly independent of the load because the internal regulation is fast enough to load the output capacitor in a few cycles. The ramp-down is faster with high loads, as expected. Figure 30 proves that it is possible to change between modes at 1 kHz without any problems.

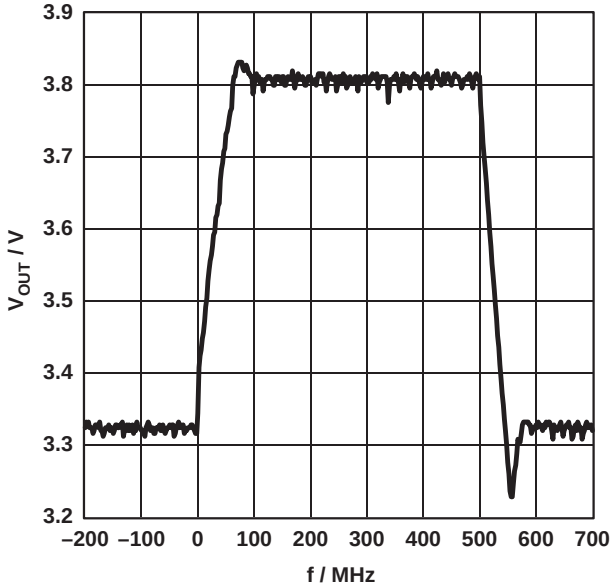

Figure 30. V_{OUT} for TPS60100, 3.3 V to 3.8 V

3 Capacitor Selection

The impact of the different capacitors on the output voltage ripple can be very high. Only ceramic capacitors are recommended for the flying capacitors (C_{xF}). The input and output capacitor can be ceramic, tantalum, or electrolytic. The influence of the different input and output capacitors is discussed in this section.

For push-pull mode, a minimum of four capacitors is needed: one input capacitor, two flying capacitors, and one output capacitor. In single-ended mode, a minimum of three capacitors is required: one input capacitor, one flying capacitor, and one output capacitor. In all modes, the input capacitor (C_{IN}) should have a minimum of half the capacitance value of the output capacitor (C_{OUT}):

$$C_{IN} \approx \frac{C_{OUT}}{2}$$

All measurements are made with the TPS60100EVM-131 (see Section 4) in push-pull mode, operating with the internal oscillator and producing an output voltage of 3.3 V. The flying capacitors for all measurements are 2.2 μF/16 V ceramic capacitors from Taiyo Yuden in a 1206 package. The capacitance value of the input capacitor is 10 μF, and the output capacitor is 22 μF. There are also 1-μF auxiliary capacitors applied to the input and output.

3.1 Capacitor Selection for Constant-Frequency Mode

In constant-frequency mode the value of the output capacitor(s) is important for device regulation. The regulation requires a minimum capacitance of 22 μF for stability because it is compensated with this value. The use of capacitors with higher capacitance is also possible. The ESR of the capacitor is not very critical. A higher ESR only leads to higher ripple.

Table 2. Ripple Dependent on Input and Output Capacitors in Constant-Frequency Mode

C_{IN} (10 μF)				C_{OUT} (22 μF)				RIPPLE V_{P-P} [mV], MAX
MFR.	SORT	PACKAGE	VOLTAGE	MFR.	SORT	PACKAGE	VOLTAGE	
Taiyo Yuden	Ceramic	1210	10 V	Taiyo Yuden	Ceramic	1812	10 V	7
Sprague	Tantalum 595D	A	10 V	Sprague	Tantalum 595D	A	6.3 V	27
Sprague	Tantalum 595D	C	25 V	Sprague	Tantalum 595D	D	25 V	13
Panasonic	Tantalum TE	D	35 V	Panasonic	Tantalum TE	D	25 V	18
AVX	Tantalum TPS	C	25 V	AVX	Tantalum TPS	C	16 V	20
AVX	Tantalum TPS	C	25 V	Panasonic	AI-Elko VS		6.3 V	80

3.2 Capacitor Selection for Pulse-Skip Mode

In pulse-skip mode, neither the capacitor value nor the ESR of the output capacitor are critical for stability. In this mode, both the capacitance and its ESR influence the output ripple. A higher capacitance and a smaller ESR cause a smaller output voltage ripple. The regulation is stable for all capacitance values, because this is a two-point regulation. Problems occur if the ESR is too high, as with aluminum electrolytic capacitors. This is not an issue with ceramic and tantalum capacitors.

Table 3. Ripple Dependent on Input and Output Capacitors in Pulse-Skip Mode

C_{IN}				C_{OUT}				RIPPLE V_{P-P} [mV], MAX
MFR.	SORT	PACKAGE	VOLTAGE	MFR.	SORT	PACKAGE	VOLTAGE	
Taiyo Yuden	Ceramic	1210	10 V	Taiyo Yuden	Ceramic	1812	10 V	75
Sprague	Tantalum 595D	A	10 V	Sprague	Tantalum 595D	A	6.3 V	257
Sprague	Tantalum 595D	C	25 V	Sprague	Tantalum 595D	D	25 V	136
Panasonic	Tantalum TE	D	35 V	Panasonic	Tantalum TE	D	25 V	179
AVX	Tantalum TPS	C	25 V	AVX	Tantalum TPS	C	16 V	181
AVX	Tantalum TPS	C	25 V	Panasonic	Al-Elko VS		6.3 V	1068

4 Description of the Evaluation Module and Layout Rules

This section describes the available evaluation modules for the TPS60100 (TPS60100EVM-131), and for the TPS60110 (TPS60110EVM-132). It discusses layout rules that can be applied to your own layout solutions, and shows the influence of soldering the thermal pad. The minimum number of external capacitors for this charge pump family is very low (only three in single-ended mode, or four in push-pull mode). The layout for a charge pump is as critical as for inductive dc/dc converters. The use of the given board layout is recommended because it has been proven.

4.1 Description of the Evaluation Module (EVM)

This section describes the EVM's schematic diagram, circuit board layout, and setup procedure.

4.1.1 Schematic of the EVM

The schematic (Figure 31) and the layout (Figures 32 and 33) of the TPS60100 evaluation module are shown. The schematic and layout for the TPS60110 are the same, except for the usage of connector 3V8.

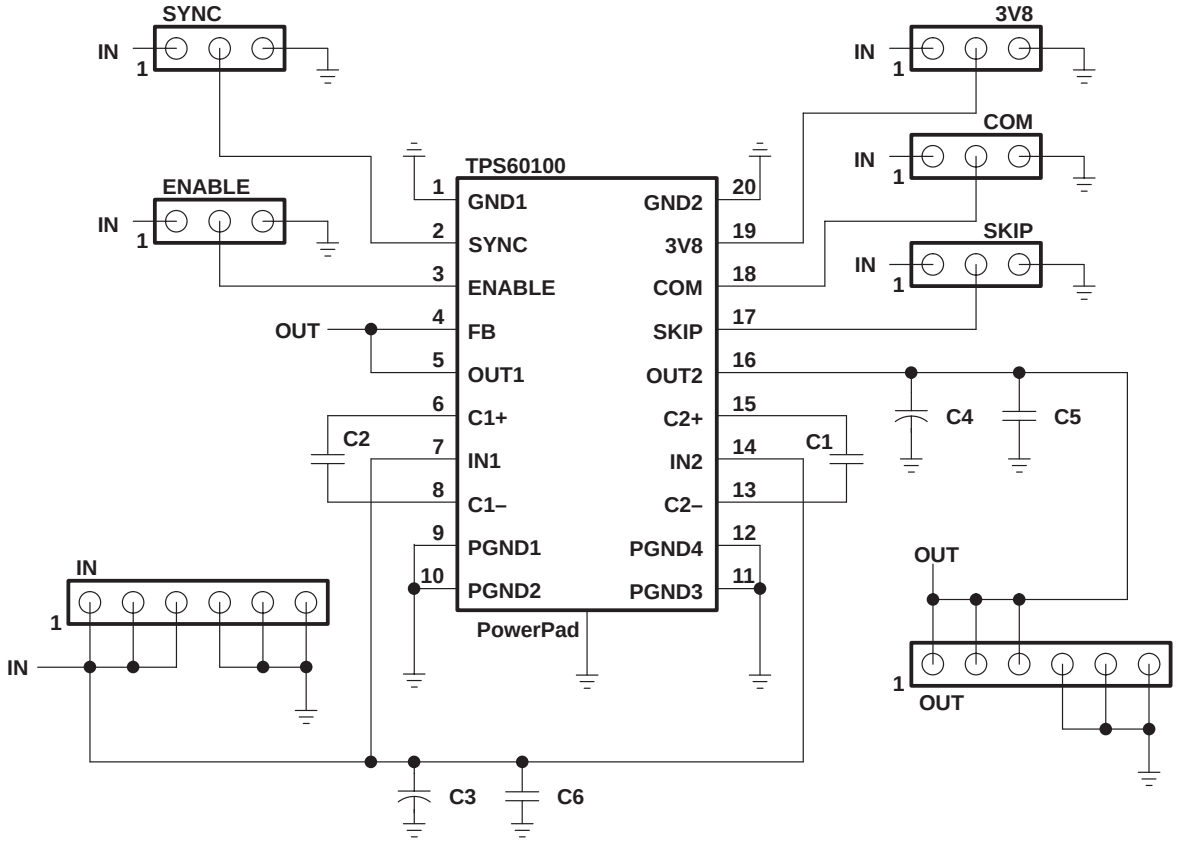

Figure 31. Schematic of the Evaluation Module (EVM)

Section 3 describes the difference in performance using various capacitors. The best performance can be obtained with ceramic capacitors; this is also the most expensive solution. Tantalum capacitors are used on the board for the higher-value capacitors. Reduction of spikes during turnover from the transfer phase of one charge pump to that of the other requires a ceramic capacitor in parallel with the tantalum capacitors at the input and output. Tantalum capacitors are not able to filter these spikes. Their serial resistance is too high to respond as fast as ceramic capacitors. The flying capacitors (C_1 and C_2) must be ceramic for their low series resistance.

Capacitors C_5 and C_6 are two ceramic capacitors used for spike reduction. If spikes are not very critical, it is possible to remove these two capacitors.The input and output are realized with two six-pin connectors on the board. Each uses the first three pins for the supply, and the last three pins for the ground signal.The other five three-pin connectors can be used to connect the five logic pins of the device. These pins are used to adjust the modes of the device (see Table 4). Each connector has the supply (V_{CC}) signal on the first pin, the logic signal on the second pin, and the ground signal on the third pin. It is possible to use jumpers to connect a pin to the input (supply voltage) or to ground. It is also possible to connect any other signal by using an external signal source connected to the second pin.

Do not leave the second pin of these three-pin connectors open; connect it via a jumper to the first or third pin, or use an appropriate external signal source with the appropriate signal level. If the pins are open (floating), the operation mode of the device is undefined. The value of the signal connected to the logic pins can be higher than the supply voltage, but must not exceed the maximum ratings.

Table 4. Selected Modes by Connecting the Jumpers

NAME	CONNECTED WITH GND	CONNECTED WITH IN
3V8	3.3 V at the output (TPS60110: internal clock is used)	3.8 V at the output (TPS60110: Do not connect with IN)
Com	Push-pull mode	Single-ended mode
EN	Device is disabled	Device is enabled
Skip	Fixed-frequency mode	Pulse-skip mode
Sync	Device operates with internal oscillator	Device is synchronized, connect the external clock to the second pin of connector 3V8.

4.1.2 Layout of the EVM

Figures 32 and 33 show the placement of the components and the layout of the EVM. Components are placed only on the top layer of the board. The signal on the bottom is the ground signal (GND). For good performance, the whole bottom layer is one ground plane, interrupted only by some vias.

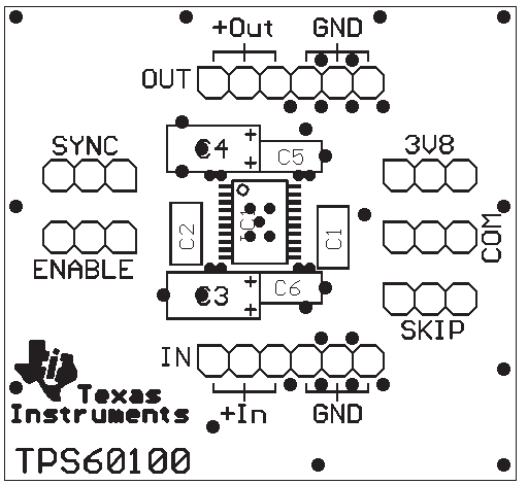

Figure 32. Placement of the Components and Vias (Black Dots)

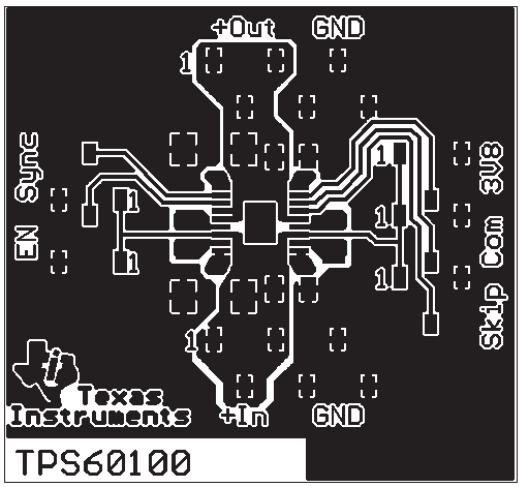

Figure 33. Top Layer of the EVM

Table 5 shows the values, manufacturer, and description of all six capacitors placed on the EVM.

Table 5. Components of the EVM

COMPONENT	VALUE (TPS60100)	VALUE (TPS60110)	MANUFACTURER SERIES	DESCRIPTION
C1, C2	2.2 µF, 16 V	2.2 µF, 16 V	Taiyo Yuden, M	Ceramic flying capacitors
C3	10 µF, 10 V	15 µF, 16 V	Sprague, 595D	Tantalum input capacitor
C4	22 µF, 20 V	33 µF, 16 V	Sprague, 595D	Tantalum output capacitor
C5, C6	1 µF, 16 V	1 µF, 16 V	Taiyo Yuden, M	Ceramic auxiliary capacitors at input and output

The required space for the IC and the capacitors on the EVM is about 15 mm $\times$ 16 mm = 240 mm^2. The capacitors are optimized for performance. For a system that does not require such a good performance, smaller capacitors are sufficient.

4.1.3 Setup of the EVM

Please follow these steps for proper operation of the EVM:

1. Check that all five logic control signals (Enable, Sync, 3V8, Com, and Skip) are properly connected with jumpers, or to an external signal source (for pin function see Table 4).
2. Connect a load to the output (between GND and Out).
3. Connect a signal source (or a battery pack) with the appropriate voltage between input (In) and ground (GND).

4.2 Temperature Differences Between Unsoldered and Soldered PowerPAD™

The devices are mounted in a PowerPAD package. The dimension and the pinning of this package are the same as for a TSSOP 20-pin package. The only difference from a standard TSSOP-package is the so-called PowerPAD on the bottom of the device. This pad is a metal plate with a very good thermal connection to the silicon. It is possible to solder this pad directly to the ground of

PowerPAD is a trademark of Texas Instruments Incorporated.

the printed-circuit board (PCB) to have a better thermal connection. Normally the ground of the PCB is a big copper plate that can dissipate a lot more heat than the device itself.

This section shows the thermal differences on the board and on the device for a soldered and an unsoldered PowerPAD for the TPS60100 and TPS60110. The tests were conducted using the EVMs for TPS60100 and TPS60110 under the following conditions: low airflow, operation in push-pull mode, maximum input voltage supplied, and maximum load current.

Tables 6 through 9 give the values measured for the different temperatures. The ambient temperature was measured less than 1 meter away from the board, the device temperature was measured on top of the device, and the board temperature was measured on the bottom of the board below the device. The junction temperature was measured based on a special voltage measurement.

4.2.1 Test Results for Unsoldered PowerPAD

Table 6 shows the test results for the temperature measurements taken on TPS60100EVM-131 with the PowerPAD unsoldered. The input voltage is 3.6 V, and the load is 200 mA. With these values, the power dissipation in the TPS60100 reaches its maximum in constant-frequency mode. The device doubles the input voltage and dissipates the unwanted power. The second part of the power dissipation is the power required by the device itself. The following formula gives the power dissipation for constant-frequency mode:

$$P_D = \left(2 \times V_{IN} - V_{OUT}\right) \times I_{OUT} + V_{IN} \times I_Q$$

$$P_D\,(TPS60100) \approx \underline{785\ mW},\ V_{IN} = 3.6\ V \text{ and } I_{OUT} = 200\ mA$$

Table 6. Temperature Test With TPS60100 With Unsoldered PowerPAD

VALUE	T/°C (Constant-frequency Mode)	T/°C (Pulse-skip Mode)
Ambient temperature, T_A	22.2	22.3
Package temperature (top), T_P	45	42.5
Board temperature (bottom), T_B	35.1	35.3
Junction temperature, T_J	~66	~62

Table 7 shows the temperature measurements taken on the TPS60110EVM-132. The input voltage is 5.4 V and the load is 300 mA. Therefore, the power dissipation for the TPS60110 in constant-frequency mode can be calculated using the previous formula to the following value:

$$P_D\,(TPS60110) \approx \underline{1754\ mW},\ V_{IN} = 5.4\ V \text{ and } I_{OUT} = 300\ mA$$

Table 7. Temperature Test for TPS60110 With Unsoldered PowerPAD

VALUE	T/°C (Constant-frequency Mode)	T/°C (Pulse-skip Mode)
Ambient temperature, T_A	22.3	22.5
Package temperature (top), T_P	79	77
Board temperature (bottom), T_B	52.5	50
Junction temperature, T_J	~125	~123

4.2.2 Test Results for Soldered PowerPAD

Table 8 shows the test results of the temperature measurements with soldered PowerPAD. The input voltage is 3.6 V and the load 200 mA. The following value gives the power dissipation for constant-frequency mode:

$$P_D\,(TPS60100) \approx \underline{785\ mW},\ V_{IN} = 3.6\ V \text{ and } I_{OUT} = 200\ mA$$

Table 8. Temperature Test for TPS60100 With Soldered PowerPAD

VALUE	T/°C (Constant-frequency Mode)	T/°C (Pulse-skip Mode)
Ambient temperature, T_A	22.5	22.6
Package temperature (top), T_P	43.6	39.5
Board temperature (bottom), T_B	37.1	35.4
Junction temperature, T_J	~55	~54

Table 9 shows the temperature measurements with the TPS60110 EVM-132 with soldered PowerPAD. The input voltage is 5.4 V and the load is 300 mA. Therefore, the power dissipation for TPS60110 in constant-frequency mode can be calculated to the following value:

$$P_D\,(TPS60110) \approx \underline{1754\ mW},\ V_{IN} = 5.4\ V \text{ and } I_{OUT} = 300\ mA$$

Table 9. Temperature Test for TPS60110 With Unsoldered PowerPAD

VALUE	T/°C (Constant-frequency Mode)	T/°C (Pulse-skip Mode)
Ambient temperature, T_A	21.8	21.7
Package temperature (top), T_P	61.5	61
Board temperature (bottom), T_B	59	60
Junction temperature, T_J	~92	~94

4.2.3 Difference in Thermal Resistance With Unsoldered and Soldered PowerPAD

With the former values given, the thermal resistance of the devices with a soldered and an unsoldered PowerPAD can be calculated for constant-frequency mode. The thermal resistance in pulse-skip mode cannot be calculated because there is not an easy correlation between input and output power as in the constant-frequency mode. The formula for the thermal resistance is as follows:

$$R_\vartheta = \frac{\Delta T}{P_D}$$

Three different thermal resistances are interesting in a system. These three are calculated for the TPS60100 and the TPS60110 in constant-frequency mode.

The three thermal resistances calculated are:

- $R_{\varphi JA}$: Thermal resistance between junction and ambient
- $R_{\varphi JC}$: Thermal resistance between junction and case
- $R_{\varphi JB}$: Thermal resistance between junction and board

The following are the formulas for thermal resistance:

$$R_{\vartheta JA} = \frac{T_J - T_A}{P_D}$$

$$R_{\vartheta JC} = \frac{T_J - T_C}{P_D}$$

$$R_{\vartheta JB} = \frac{T_J - T_B}{P_D}$$

Table 10. Thermal Resistances for TPS60100 and TPS60110 in Constant-Frequency Mode

THERMAL RESISTANCE	TPS60100: UNSOLDERED PowerPAD	TPS60100: SOLDERED PowerPAD	TPS60110: UNSOLDERED PowerPAD	TPS60110: SOLDERED PowerPAD
$R_{\varphi JA}$	56°C/W	41°C/W	59°C/W	40°C/W
$R_{\varphi JC}$	27°C/W	15°C/W	27°C/W	17°C/W
$R_{\varphi JB}$	39°C/W	23°C/W	43°C/W	19°C/W

You can see that the thermal resistance with a soldered PowerPAD is between 10°C/W and 24°C/W lower than with an unsoldered PowerPAD.

Although the device will not be destroyed with an unsoldered PowerPAD, the best solution is to solder the PowerPAD to reduce the stress on the device.

You can also see that there is only a small difference between the thermal resistances of the TPS60100 and the TPS60110. The thermal resistance is mainly dependent on the package. Therefore, the values are also usable on TPS60101 and TPS60111, and also in pulse-skip mode.

All the values in Table 10 are typical values.

4.3 Layout Rules for Design

The layout of the EVM may not be feasible on a new system. This section establishes some general rules for the realization of a customized layout. The layout of a charge pump is as critical as that of any other dc/dc-converter. Please keep the following design rules in mind when designing a new layout.

- For dc/dc-converters the layout of the ground potential is very important. The devices have six different ground pins, and these pins should be at the same potential. Therefore, the impedance of the ground connections should be as low as possible. This can be achieved with a *ground layer,* or at least a *ground plane*.
- The devices consist of two independent charge pumps located on each side of the package. For proper and low noise operation *the whole layout has to be as symmetrical to the middle (length) of the device as possible* (look at the layout of the evaluation module).
- The placement of the capacitors is also very important. *All capacitors should be as near to the device as possible*. The capacitors must be charged and discharged very fast, or must react very fast to transients; therefore, the lead resistance has to be reduced with shorter lead lengths to the capacitors. The highest priority is the output capacitor, followed by the input capacitor. The placement of the flying capacitors is not that important as long as they are symmetrical to the device.

5 Application Examples

5.1 Reduction of Spikes With an LC-Filter at the Output

In every switch mode power supply, spikes appear during turnover from one phase to the other. For example, in a single-ended charge pump, these spikes happen during turnover from charge to transfer phase. In the push-pull configuration of the TPS6010x or TPS6011x, these spikes appear during turnover of the transfer phase of one internal charge pump to the other. On many applications these spikes are not critical, and filtering with the output capacitor is satisfactory. For applications where these spikes are critical, a simple solution is shown to reduce, or even to eliminate, these spikes.

All measurements are made on the evaluation modules for TPS60100 and TPS60110 (see the last section) with maximum input voltage and maximum output current. In this case the spikes reach their maximum value. They increase with input voltage and output current. The device is operating in push-pull, linear mode, with the internal oscillator, and a 3.3 V (TPS60100)/5 V (TPS60110) output voltage.

5.1.1 Output Behavior Without Filter

Figures 34 through 37 show the spikes during turnover from one transfer phase to the other, and the spectrum of the output voltage for TPS60100 and TPS60110.

TPS60100

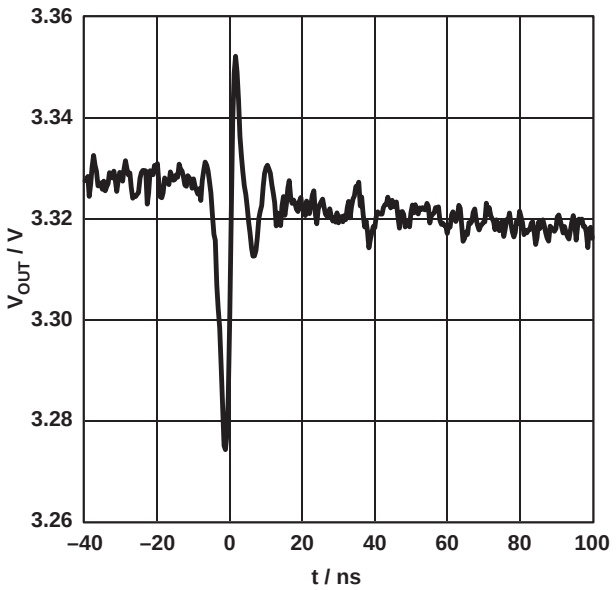

Figure 34. TPS60100: Spikes on the Output Voltage Without LC Filter

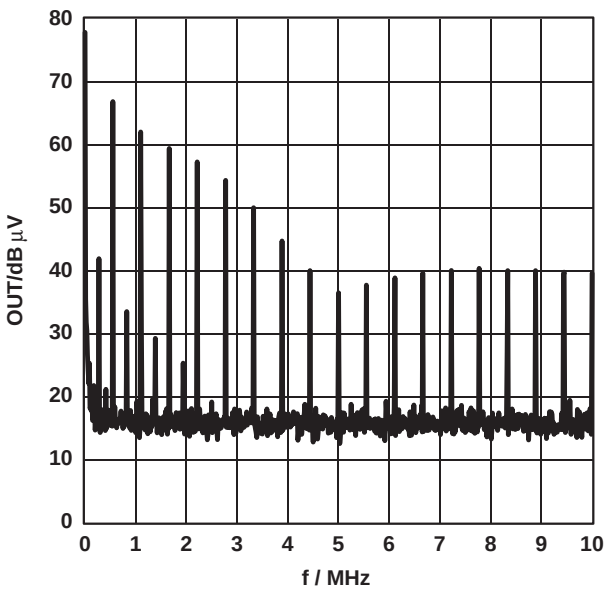

Figure 35. TPS60100: Spectrum of the Output Voltage Without LC Filter

TPS60110

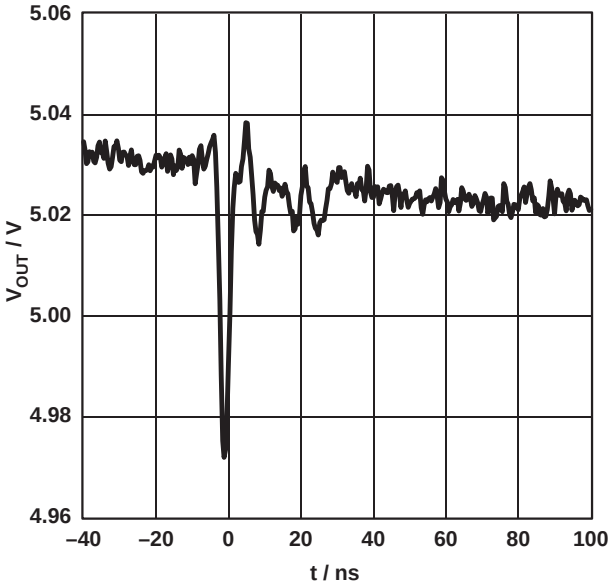

Figure 36. TPS60110: Spikes on the Output Voltage Without LC Filter

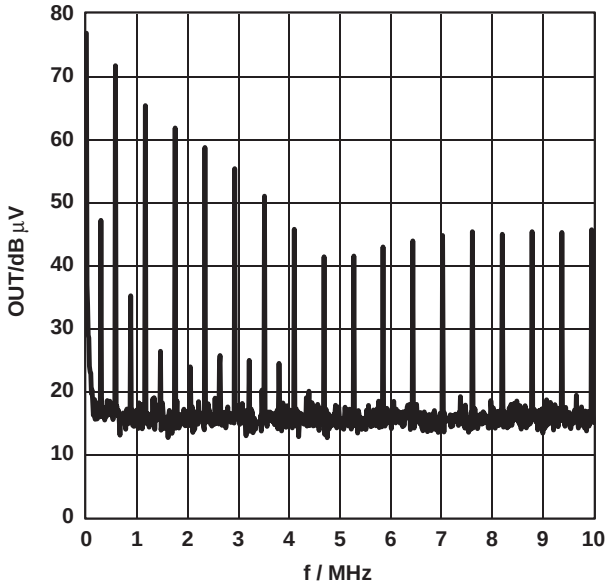

Figure 37. TPS60110: Spectrum of the Output Voltage Without LC Filter

Figures 34 and 36 show that the frequency of the spike is around 100 MHz. Therefore, a filter with a cut-off frequency clearly below 100 MHz is required to get a good filter characteristic at and above 100 MHz. Figure 38 shows the filter configuration used, and Table 11 gives the values of the evaluated filters. The cut-off frequency for the first filter is around 2.3 MHz, and around 0.5 MHz for the second filter. Both cut-off frequencies are in a good range to filter the output spikes. Two filters were evaluated to get results on the influence of the dc resistance of the inductor.

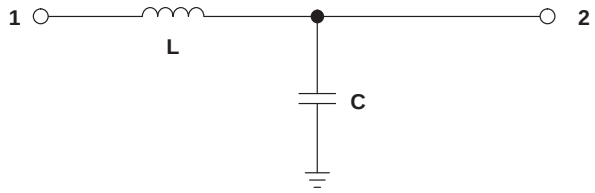

Figure 38. LC-Filter Used

Table 11. Filter Values for the Two Test Filters (see Figure 38)

COMPONENT	VALUE/DC RESISTANCE	MANUFACTURER	ORDER CODE
L1 (Filter 1)	47 nH/0.16 Ω	Coilcraft	1008CS-680XKBC
C1 (Filter 1)	100 nF		
L2 (Filter 2)	100 nH/0.8 Ω	Taiyo Yuden	LEM2520BR10K
C2 (Filter 2)	1 µF	Taiyo Yuden	LMK212BJ105KG-T

5.1.2 Spike Behavior With Additional LC Filter at the Output

The easiest way to implement this filter is to add it at the output of the device. Figures 39 through 44 show the behavior of the output voltage behind the LC filter 1. The LC filter is added without changing the rest of the board. The feedback of the output voltage is connected to point 1 in Figure 38.

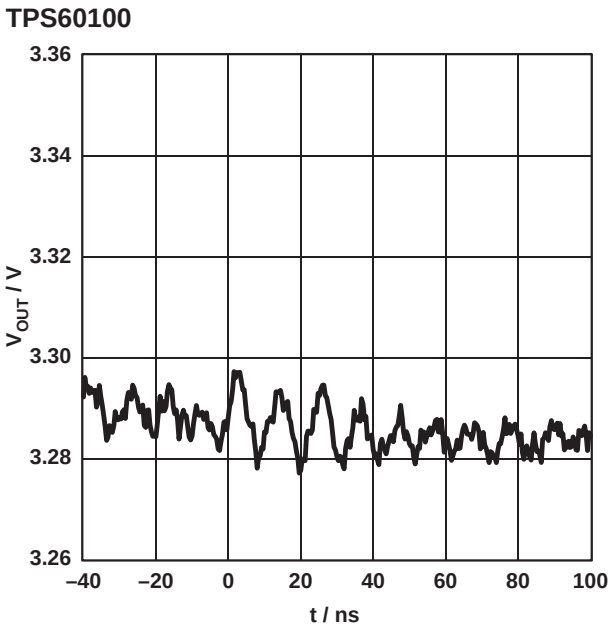

Figure 39. TPS60100: Spikes at the Output Voltage With Filter 1

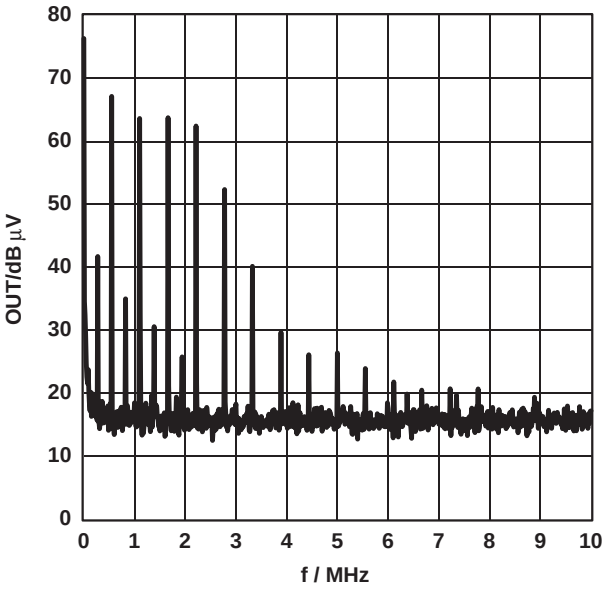

Figure 40. TPS60100: Spectrum of the Output Voltage With Filter 1

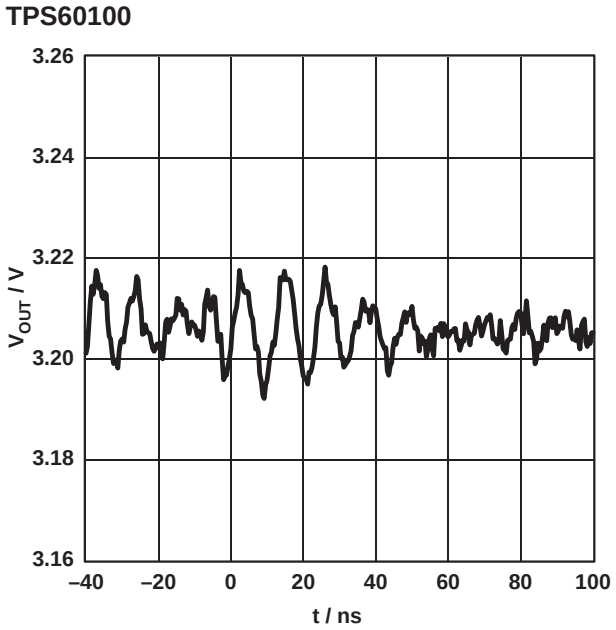

Figure 41. TPS60100: Spikes at the Output Voltage With Filter 2

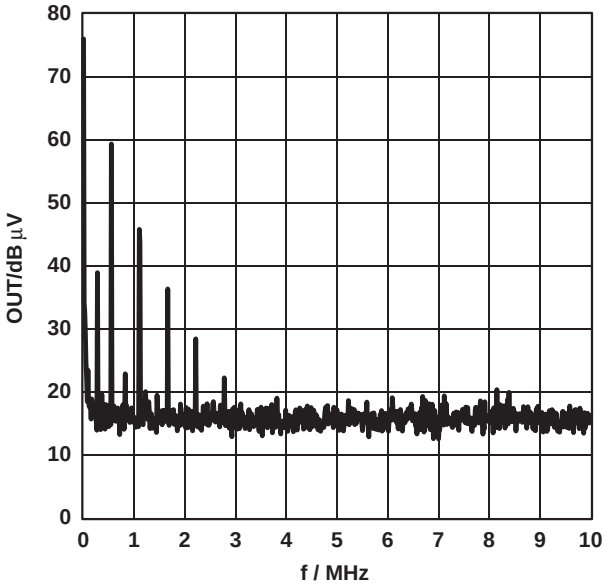

Figure 42. TPS60100: Spectrum of the Output Voltage With Filter 2

TPS60110

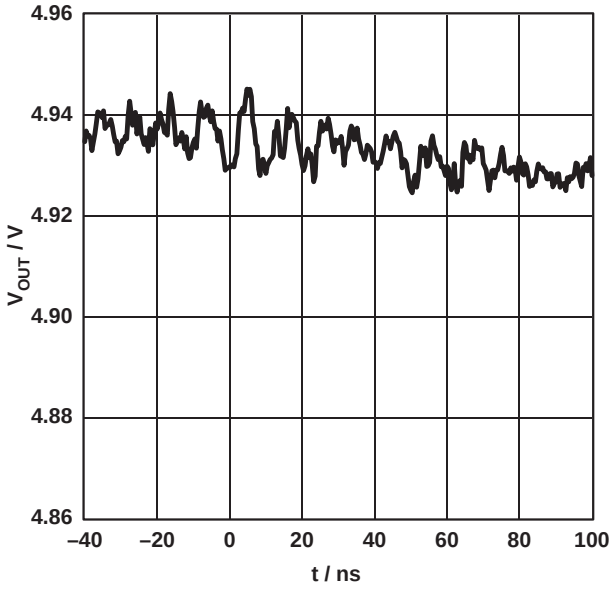

Figure 43. TPS60110: Spikes at the Output Voltage With Filter 1

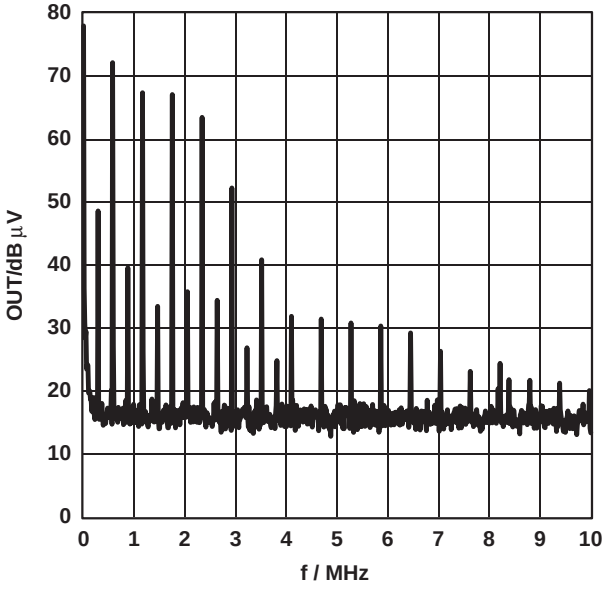

Figure 44. TPS60110: Spikes at the Output Voltage With Filter 1

TPS60100

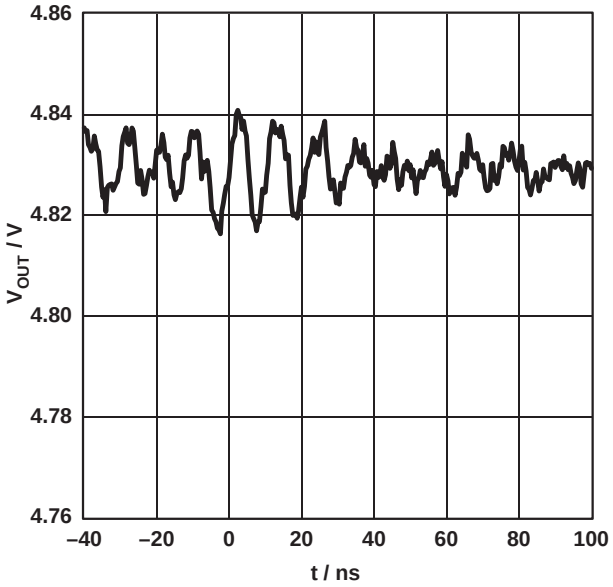

Figure 45. TPS60110: Spikes at the Output Voltage With Filter 2

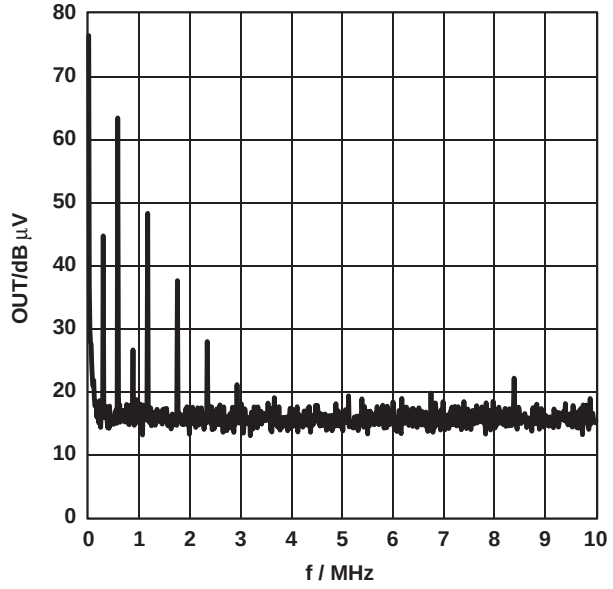

Figure 46. TPS60110: Spikes at the Output Voltage With Filter 2

Comparing Figures 39 through 44 with Figures 34 through 37, it can be observed that the spikes are clearly reduced and the operating frequency harmonics in the output voltage are suppressed.

There is only one disadvantage with this configuration: the voltage in front of the LC filter is regulated, and therefore the voltage behind the LC filter is dependent on the dc resistance of the inductor. The figures show that the output voltage is reduced by less than 100 mV for the maximum output current with Filter 1. The dc resistance of the inductor L1 is low, and therefore the voltage drop is not very critical.

Figures 47 and 48 show the output voltage of the TPS60100 behind the two LC filters. At the time 0 μs a load jump occurs from 0 mA to 200 mA. After the glitch, the output voltage reaches the regulated value. The regulation happens before the inductor and therefore the series resistance of the inductor influences the output voltage behind the LC filter. Figure 47 shows that the low resistance of L1 (0.16 Ω) causes a difference in the output voltage of less than 20 mV, whereas L2 (0.8 Ω) (see Figure 48) causes a difference of about 120 mV.

TPS60100

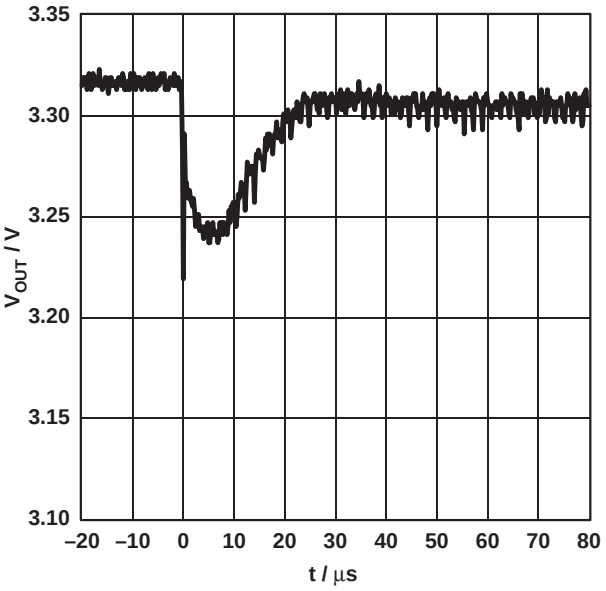

Figure 47. TPS60100: Output Voltage After Load Jump With Filter 1

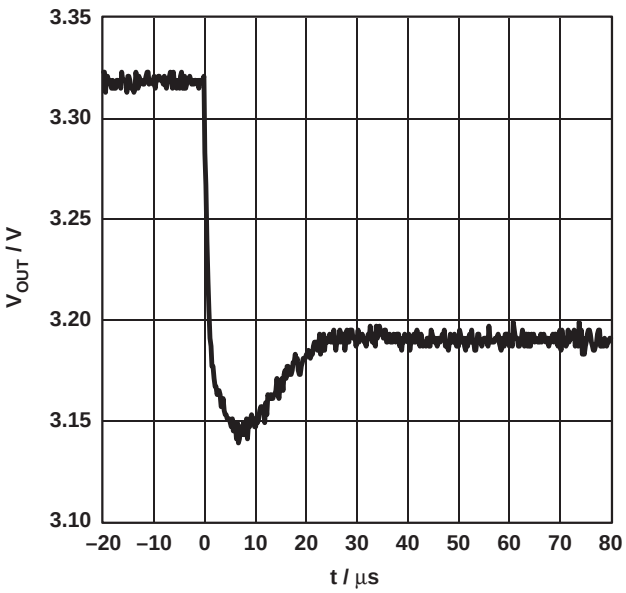

Figure 48. TPS60100: Output Voltage After Load Jump With Filter 2

Figures 49 and 50 show the behavior of the output voltage of the TPS60110 behind two different LC filters after a load jump from 0 mA to 300 mA. As in the TPS60100, the series resistance of the inductor influences the output voltage behind the LC filter.

TPS60110

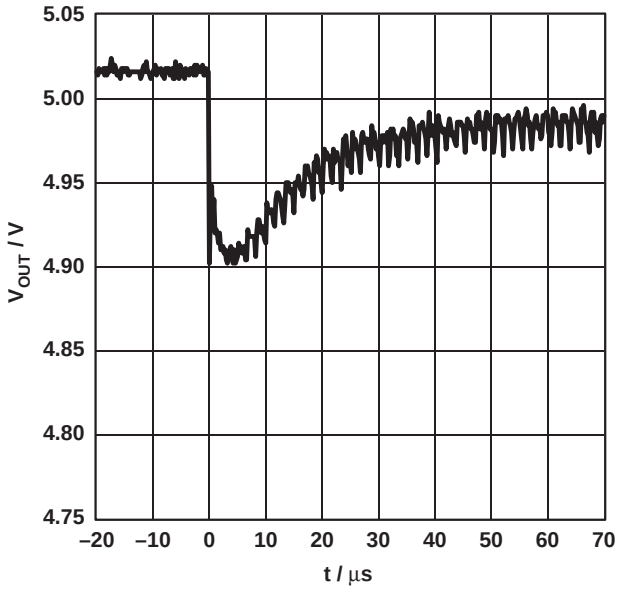

Figure 49. TPS60110: Output Voltage After Load Jump With Filter 1

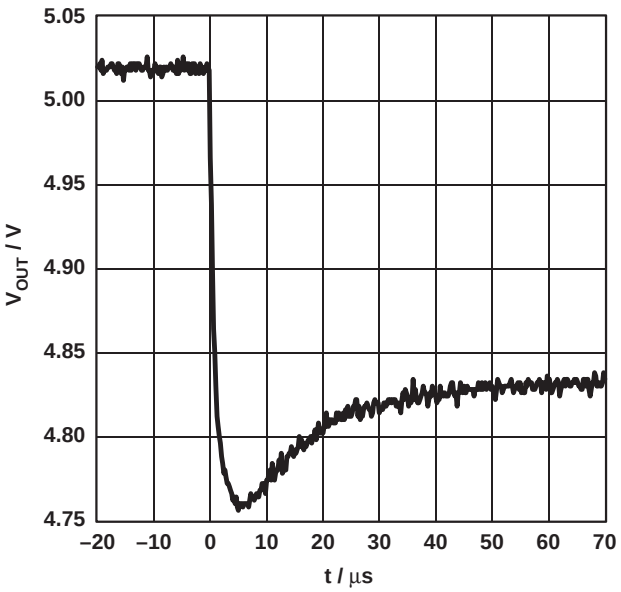

Figure 50. TPS60110: Output Voltage After Load Jump With Filter 2

5.1.3 Add LC Filter and Connect FB-Pin Behind Inductance

The problem with the previous configuration is that the output voltage behind the LC filter is very dependent on the series resistance of the inductor and on the load. This can be eliminated with the feedback pin connected behind the inductor of the LC filter (point 2 in Figure 38). This adds a further pole to the feedback control loop, and it is recommended to use a filter with a cut-off frequency lower than that of Filter 2.

Connecting the FB pin behind the inductor of the filter has almost no influence on spike filtering. The spikes and the spectrum are comparable to the results in Section 5.1.2. Therefore, only the influence on changes in the output load is shown.

Figures 51 through 54 demonstrate that the output voltage behind the inductor is now regulated and no longer dependent on the load. The series resistance only has influence on the glitch during load changes. Nevertheless, the series resistance should not be too high because the loss across this series resistance has to be supplied by the charge pump. The output voltage supplied by the charge pump is higher due to this loss, and therefore the input voltage can not reach the minimum value given in the data sheets.

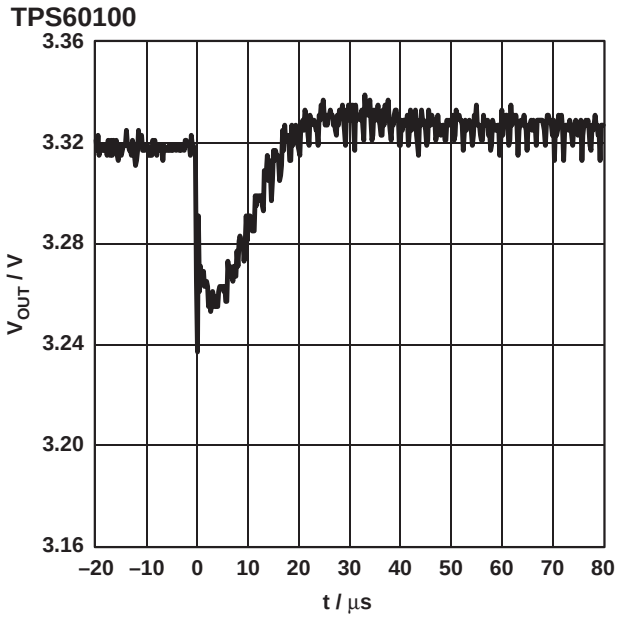

Figure 51. TPS60100: Output Voltage After Load Jump With Filter 1 (FB behind L1)

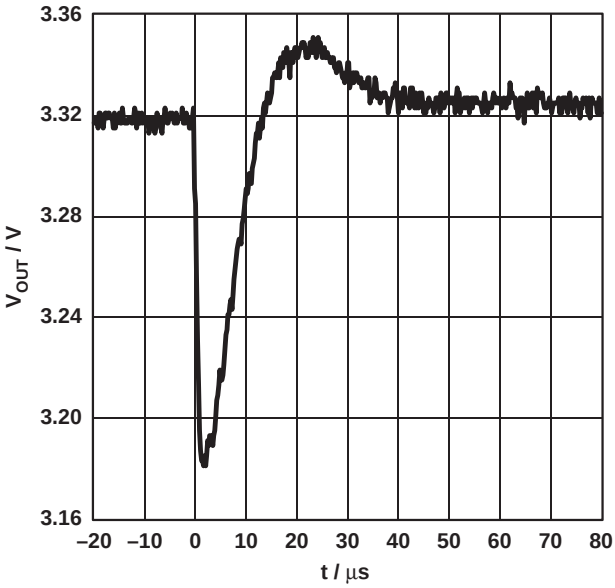

Figure 52. TPS60100: Output Voltage After Load Jump With Filter 2 (FB behind L2)

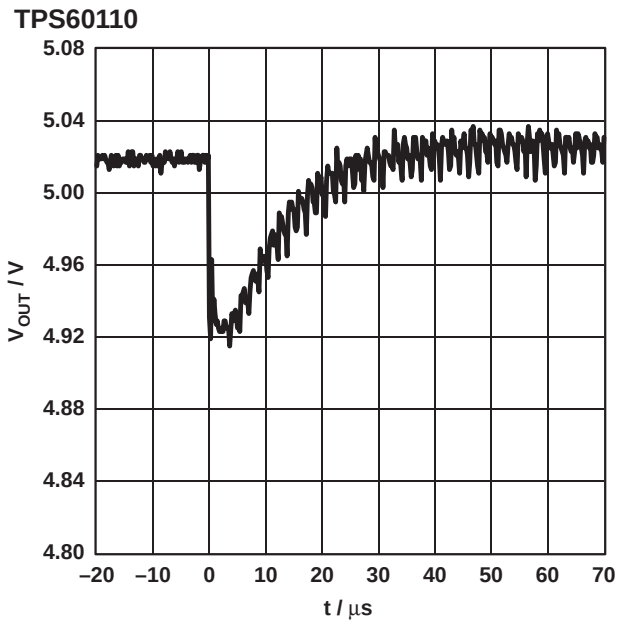

Figure 53. TPS60110: Output Voltage After Load Jump With Filter 1 (FB behind L1)

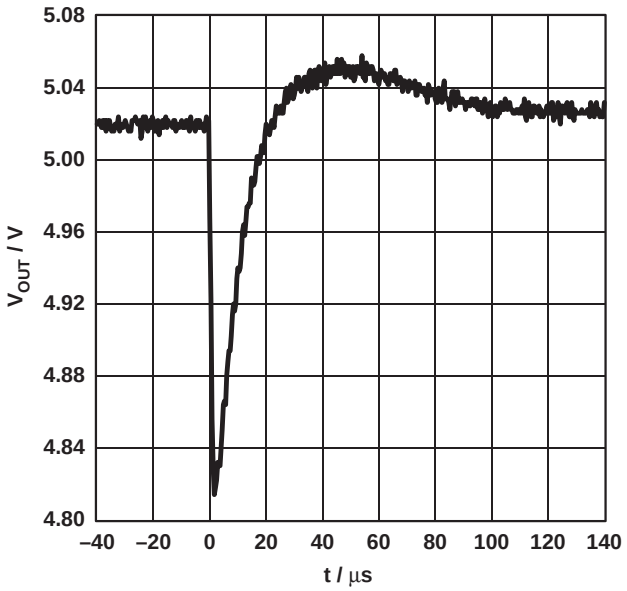

Figure 54. TPS60110: Output Voltage After Load Jump With Filter 2 (FB behind L2)

5.2 Power Supply for a Low Power Digital Signal Processor (DSP)

The generation of the proper two-output voltages for the new low-power TI DSPs of the C5000 series is described in the following sections. The source is a battery pack with two batteries (Alkaline, Nickel-Cadmium, or Nickel-Metal-Hydride). This solution may also be feasible for other low power systems that need two different voltages.

These DSPs need two different supply voltages for operation. The peripheral blocks of the DSP (inputs and outputs) are normally supplied by 3.3 V; the computing function itself (*core*) runs on a voltage of 2.5 V (for example, TMS320VC549, TMS320VC5410) or 1.8 V (for example, TMS320VC5402, TMS320VC5409, TMS320VC5420).

This section will introduce circuits that are cost effective and offer good performance for the price. Other products may certainly offer a higher efficiency; however, their cost can be much higher.

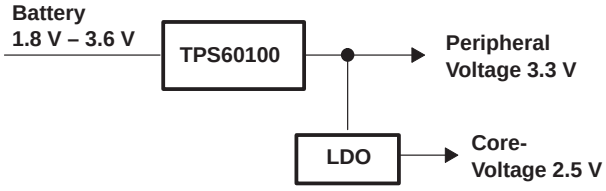

Figure 55. Solution for 2.5-V Core

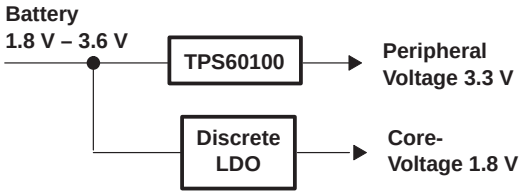

Figure 56. Solution for 1.8-V Core

Power supplies requirements for TI's C5000 DSPs:

- Low frequency of the output voltage, rapid load and input voltage oscillation control

- C549/10: V_{core} = 2.5 V ± 7% V_{per} = 3.3 V ± 10%
- C5402/09/20: V_{core} = 1.8 V ± 7% V_{per} = 3.3 V ± 10%
- Current consumption: *DSP core* between 30 mA and 180 mA typical
- Current consumption: *DSP Peripheral* 40 mA typical; in addition, the current consumption of the other 3.3-V circuits must be taken into account.
- With the C549/10, the *core* voltage must never be allowed to exceed the peripheral voltage by more than 0.5 V.

5.2.1 Generating the 3.3 V Peripheral Voltage With the Charge Pump TPS60100

If ENABLE is set to 1 and all other control signals are set to ground (GND), the device operates in the *constant-frequency* mode with the internal oscillator signal. The two charge pumps work in anti-phase and the following properties can be seen.

The properties of the TPS60100, which can serve as recommended values, are:

Output voltage at ambient temperature of –40°C to 85°C and at a minimum input voltage of 2 V:	3.3 V ± 4%
Ripple of the output voltage at 200-mA load current:	< 20 mV
Overshot of the output voltage with a load change of 10 mA to 200 mA:	±25 mV
Minimum output current at 2-V battery voltage:	200 mA
Current consumption in *constant-frequency* mode:	1.5 mA
Current consumption in *pulse-skip* mode:	50 µA
Efficiency at 2.4-V input voltage and 200-mA load current:	69%

5.2.2 Generation of the Core Voltage for the TI C549/10 DSPs

As the *core* voltage of the C549/10 is only slightly lower than the peripheral voltage, it is a good solution to use a low-dropout linear voltage regulator (LDO) to generate the 2.5-V *core* voltage from the 3.3-V peripheral voltage produced by the charge pump. With a battery voltage of 2.4 V, the total efficiency is around 52% (68% for the charge pump, and 76% efficiency for the LDO). This low value is justifiable because the LDO TPS76325 in the 5-pin SOT-23 case is a simple and cost-effective solution.

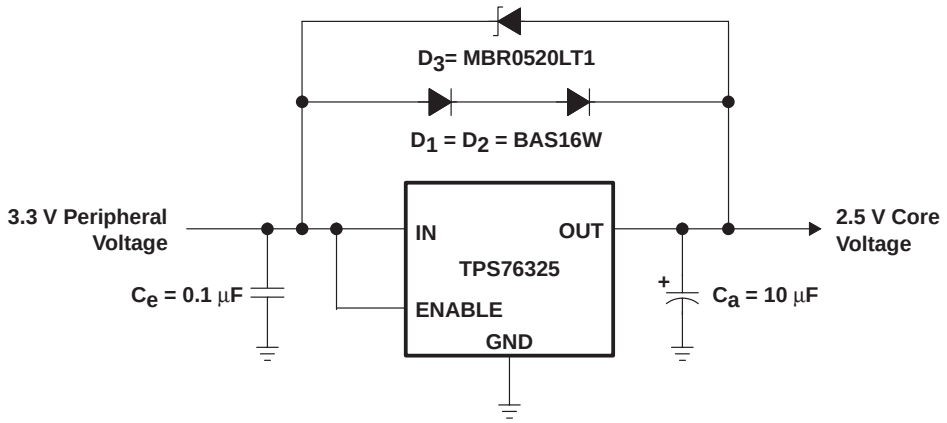

Figure 57. TPS76325 With External Circuitry

According to Section 5.2.1, the charge pump decouples the LDO from the battery; the ENABLE pin in the LDO does not need to be switched, it remains set to 1. The two silicon diodes D1 and D2 (BAS16W) placed in series from the input to the output of the LDO should prevent the peripheral and core voltage from deviating by more than 2 V from each other when switched on. The polarized Schottky diode D3 (MBR0520LT1), connected in the opposite direction, discharges the LDO output capacitor (C_a) so that the peripheral voltage does not exceed the 0.5-V voltage difference between *core* and peripheral. With this arrangement, the charge pump TPS60100 supplies both the current for the *core* as well as for the peripheral sections of the DSP. With a battery voltage of 2 V, the total value of these currents must not exceed 200 mA.

Summary of the important properties of the 2.5-V *core*-voltage supply using TPS76325 in Figure 57:

Output voltage at ambient temperature of –40°C to 85°C:	2.5 V ±3%
Tolerance on the output voltage at a load change from 2 mA to 100 mA:	±50 mV
Maximum output current:	150 mA
Efficiency level at 2.4-V battery voltage and 100-mA load current (LDO connected to TPS60100):	52%

5.2.3 Voltage Regulator for Generation of the 1.8 V Core Voltage for the TI C5402/09/20 DSPs

If a *core* voltage of 1.8 V is generated with the charge pump and a linear regulator, then only 37% efficiency will be attained. It is therefore better to supply the 1.8 V directly from the battery.

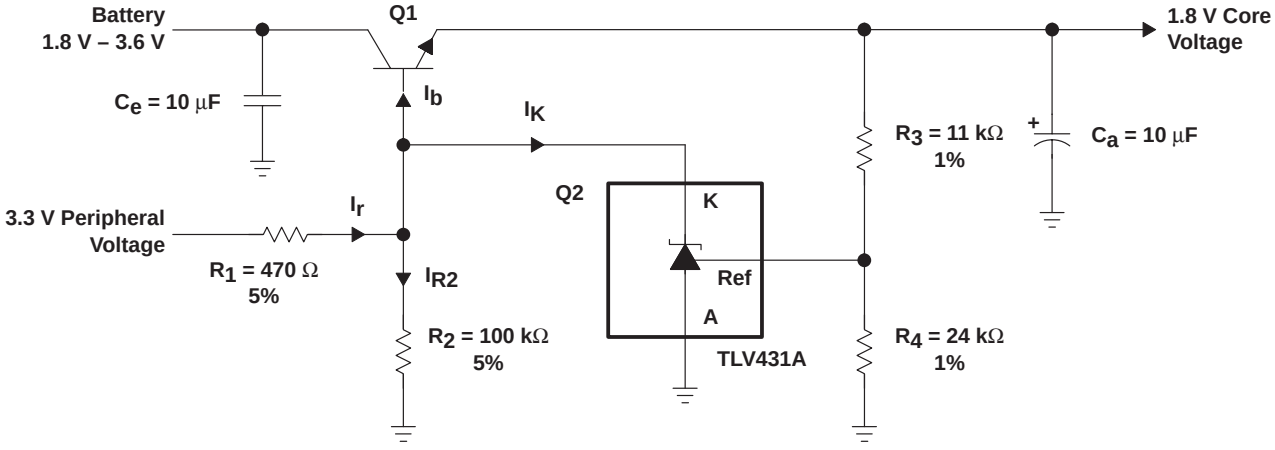

Figure 58. Discrete 1.8-V LDO

An NPN transistor Q1 (BC817-40) functions together with the shunt regulator Q2 (TLV431A) as a *low-dropout* linear regulator. Regulator Q2 drives the base current of Q1 by conducting a larger or smaller part (I_K) of the provided control current (I_r) to ground.

An error amplifier in Q2 regulates I_K in relation to the voltage deviation between the internal voltage reference (1.24 V) and the voltage at pin *Ref*. The latter is divided down from the 1.8-V output by the resistive divider R3/R4.

The regulator current I_r is not provided by the collector voltage of the NPN transistor Q1 as in normal linear regulators, but from the 3.3-V output voltage of the charge pump (V_{per}).

$$I_r \approx I_{b,max} \approx \frac{U_{per} - U_{Core} - U_{beQ1}}{R_1} \approx \frac{0.8\ V}{R_1} \quad when\ I_{R2},\ I_K \ll I_r$$

This provides a number of advantages:

- If needed, Q1 can be operated in saturation since its base current is driven by a higher voltage (3.3 V) that is independent of the collector voltage. In this way, a small dropout voltage of the 1.8-V regulator of about 100 mV at 100 mA load can be achieved. The level of the control current (I_r) which represents the base current when the NPN transistor is operated in saturation, defines the saturation voltage. In the circuit of Figure 58, a control current of about 1.8 mA was chosen. This represents a good compromise between the achievable saturation voltage and the additional current consumption of the 3.3-V charge pump.
- Since the 1.8-V *core* voltage is generated directly from the battery, the efficiency with a battery voltage of 2.4 V is 75%. This value is about twice as high as in the solution described in Section 5.2.2.
- As the base current Q1 is dependent on the 3.3-V peripheral voltage, an automatic connection of *core* and peripheral voltage arises. The *core* voltage is below the peripheral voltage. The value of this deviation is the sum of the base voltage of Q1 and the voltage drop over R1. In practice this is around 1 V. In addition, if the peripheral voltage fails (TPS60100 ENABLE pin on ground potential) the *core* voltage is switched off. Thus the resistance R2 holds the base of the transistor Q1 at ground potential.

The maximum output current of the circuit is limited by the loss in transistor BC817-40 in the SOT23 case. Thus, at an ambient temperature of 85°C, with a soldered PowerPAD, 225 mW of power dissipation is allowed for the transistor. With a maximum input voltage of 3.6 V, a voltage of 1.8 V drops via Q1, and thus a maximum constant current of 125 mA is allowed. For larger output currents, a component with a higher maximum-power dissipation must be chosen, such as the BCP54.

The linear regulator given in Figure 58 for the 1.8-V *core* voltage has the following properties:

Output voltage at ambient temperature of 0°C to 85°C and minimum input voltage of 2 V:	1.8 V ±2.75%
Saturation voltage at 100-mA load:	100 mV
Overshot of the output voltage at a load change from 2 mA to 100 mA:	±30 mV
Maximum output current at 3.6-V input voltage (determined by power dissipation):	125 mA
Current consumption from the 3.3-V peripheral voltage (regulator current I_r):	1.8 mA
Efficiency at 2.4-V input voltage and 100-mA load current:	75%

5.3 Two Devices in Parallel Double the Current

Although the TPS60100/TPS60110 devices are high-current charge pumps, there may be applications where even these output currents are too low. A good solution is to connect two of them in parallel. Two TPS60100 in parallel deliver an output current up to 400 mA, while two TPS60110 in parallel deliver an output current up to 600 mA. Each of the devices in parallel needs its own flying and input capacitors, but the output capacitors should be shared.

Figure 59 shows the connection of two devices in parallel: TPS60100 or TPS60110. Note that the logic pins are not connected in this schematic. Each mode is allowed, but it is recommended to use the same mode for both devices. Table 12 gives the values for the capacitors used on the test in this application. It is also possible to use other capacitor values, like the one given in the data sheets.

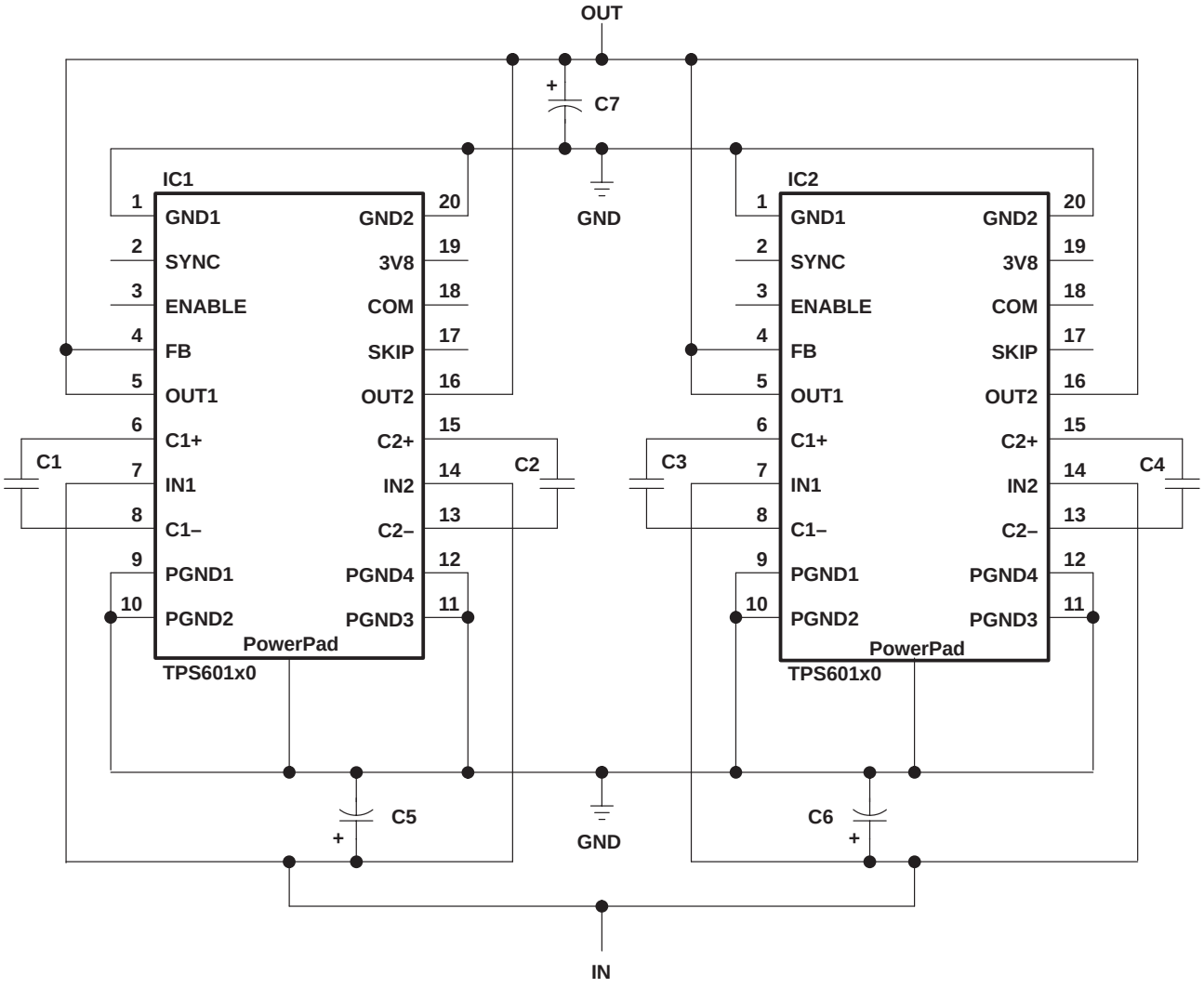

Figure 59. Two Devices in Parallel Double the Current

Table 12. Capacitor Values of Figure 59

CAPACITOR	TPS60100	TPS60110
C1, C2, C3, C4	2.2 µF	2.2 µF
C5, C6	10 µF	15 µF
C7	22 µF	33 µF

For a good performance of this solution some layout rules should be kept in mind:

- Apply the layout rules for a single charge pump. They are still valid.
- Make the layout of the two charge pumps as similar as possible.
- Place the output capacitor equidistant from both charge pumps.

5.4 Changing Output Voltage by Adding a Linear Regulator to the Output

For some applications, the output voltage of TPS6010x/TPS6011x may not be sufficient. The system could require a voltage slightly higher or lower than 3.3 V, or a little bit lower than 5 V. For example, the system could need 3.2 V, 3.4 V, or 4.8 V. In all these cases, the TPS6010x/TPS6011x with a low dropout regulator at the output is the right choice. Figure 60 shows the block diagram of this solution.

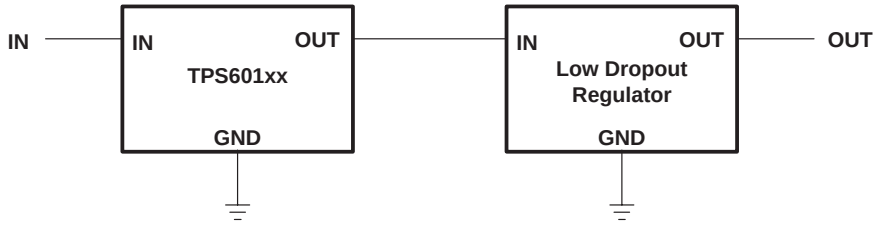

Figure 60. TPS6010x/TPS6011x With Low Dropout Regulator at the Output

The TPS72xx family, or the TPS763xx family of regulators are easy to use low-dropout regulators. Several fixed-voltage versions are available. If the output voltage required is not available, both families also provide adjustable versions.

A positive feature of this solution is that the ripple at the output of the LDO is reduced. The following figures compare the output voltage of the TPS60100 in 3.3-V mode without LDO, and the output voltage behind the LDO with the TPS60100 in 3.8-V mode. In all four measurements the TPS60100 is supplied with an input voltage of 2.2 V and operates in push-pull, constant-frequency mode with the internal oscillator.

Figures 61 and 62 compare the output voltage of the TPS60100 with an output current of 200 mA, with and without TPS7201 (configured for 3.3 V output voltage).

Figures 63 and 64 compare the output voltage of the TPS60100 with an output current of 150 mA with and without TPS76301 (configured for 3.3-V output voltage).

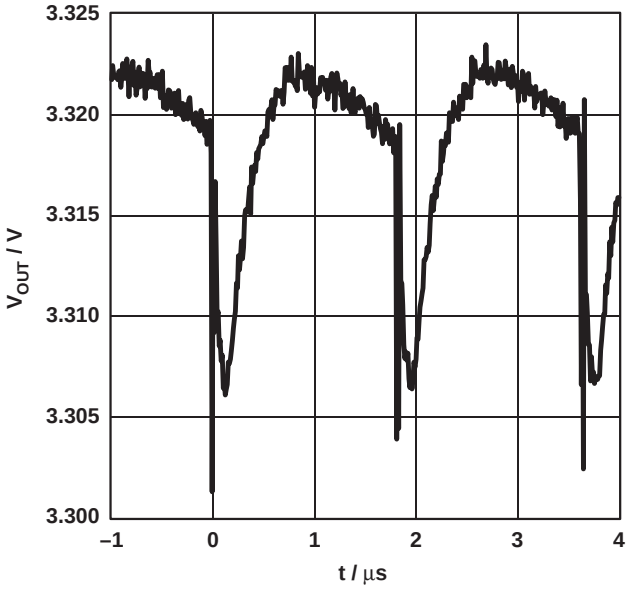

Figure 61. TPS60100: Output Ripple Without LDO

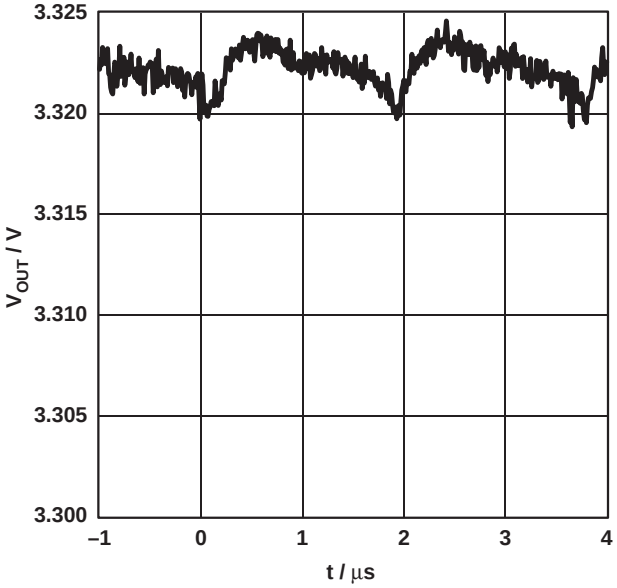

Figure 62. TPS60100: Output Ripple With TPS7201

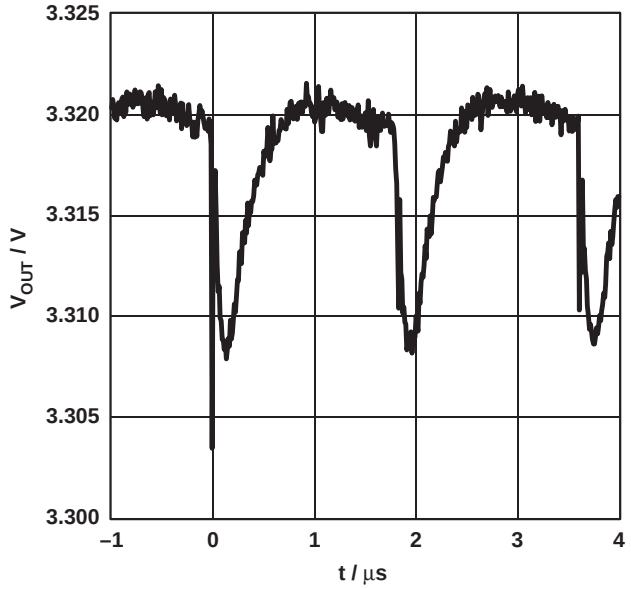

Figure 63. TPS60100: Output Ripple Without LDO

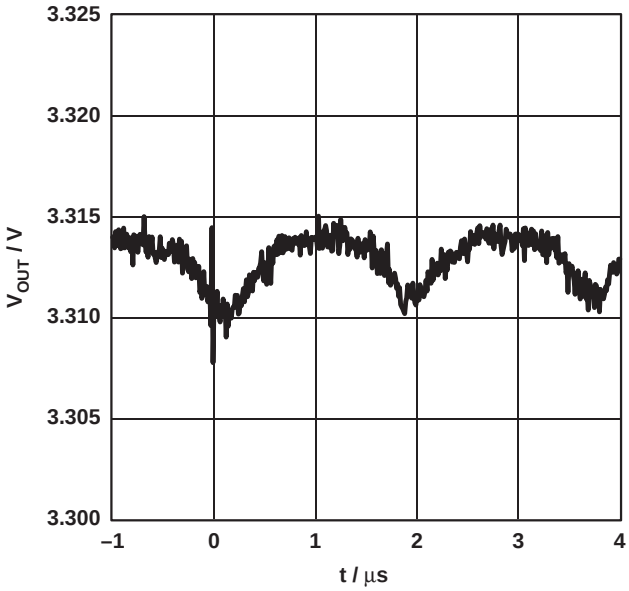

Figure 64. TPS60100: Output Ripple With TPS76301

Another advantage of this solution is that the efficiency is nearly independent of the low-dropout regulator. As long as the input voltage is higher than 2.2 V, and an output voltage of 3.3 V is required, the unwanted power has to be dissipated in the charge pump or in the linear regulator. For example, in a system with the load far away from the charge pump, the solution is to apply the 3.8-V mode and use a linear regulator near the load.

5.5 Regulated Discharging of the Output Capacitor

If the TPS6010x/TPS6011x devices are disabled, the outputs are in the high impedance state. The discharging of the output capacitor depends on the load and leakage current of the capacitor. This may not be acceptable in some applications, and the output capacitor must be regulated during discharge. This section describes simple solutions to regulate the discharge of the output capacitor with the ENABLE signal used to disable the charge pump.

The measurements are taken with evaluation modules TPS60100EVM–131 and TPS60110EVM-132. The devices are operated in push-pull, fixed-frequency mode, using the internal oscillator, and have an output voltage of 3.3 V (TPS60100)/5 V (TPS60110). The ENABLE pin of the device is connected to a function generator that generates a 1-Hz rectangular signal with an amplitude equal to the circuit supply voltage to ground. The discharge current is measured with a series sense resistor in the discharge path. The voltage across this sense resistor is measured with an instrumentation amplifier circuit with two TLE2027 operational amplifiers.

5.5.1 Discharging With an Open-Drain Buffer

Figure 65 shows the diagram of the circuit for regulated discharging of the output capacitor with a buffer. It is built up with an SN74LVC07A with open-drain outputs (it has six separate buffers). The ENABLE signal used to enable and disable the charge pump is also used to switch one of the buffers on the SN74LVC07A. As long as the charge pump is enabled, the input of the buffer is high, and the output is high impedance (open-drain). If the TPS6010x/TPS6011x is disabled, the input of the buffer is low and the output is driven to ground. This discharges the output capacitor (discharge current, I_{dis}). The current-limiting resistor (R_{LIM}) is necessary because the SN74LVC07A can drive a maximum constant current of 24 mA. The absolute maximum ratings for this device show a drive current of ±50 mA. An overdrive of this magnitude is not permitted. Therefore, the current limiting resistors for the two devices are set to 91 Ω for TPS6010x, and 130 Ω for TPS6011x, both from the E24 series. It is possible to use smaller resistors, but it is not recommended to use more than the nominal 40 mA to stay in the safe area of the buffer.

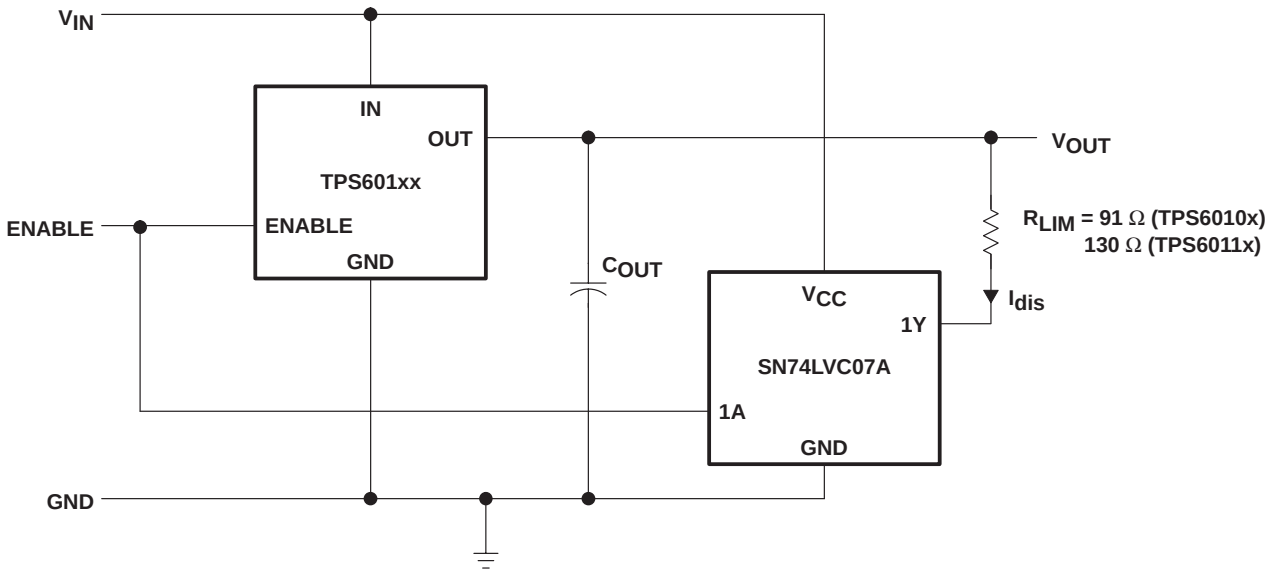

Figure 65. Block Diagram for Regulated Discharging With a Buffer

TPS60100

Figures 66 and 67 show the voltage across, and the discharge current through the buffer. The measurements are taken at 2.4-V input voltage. The worst case is without a load; in this case the capacitor is discharged within 20 ms.

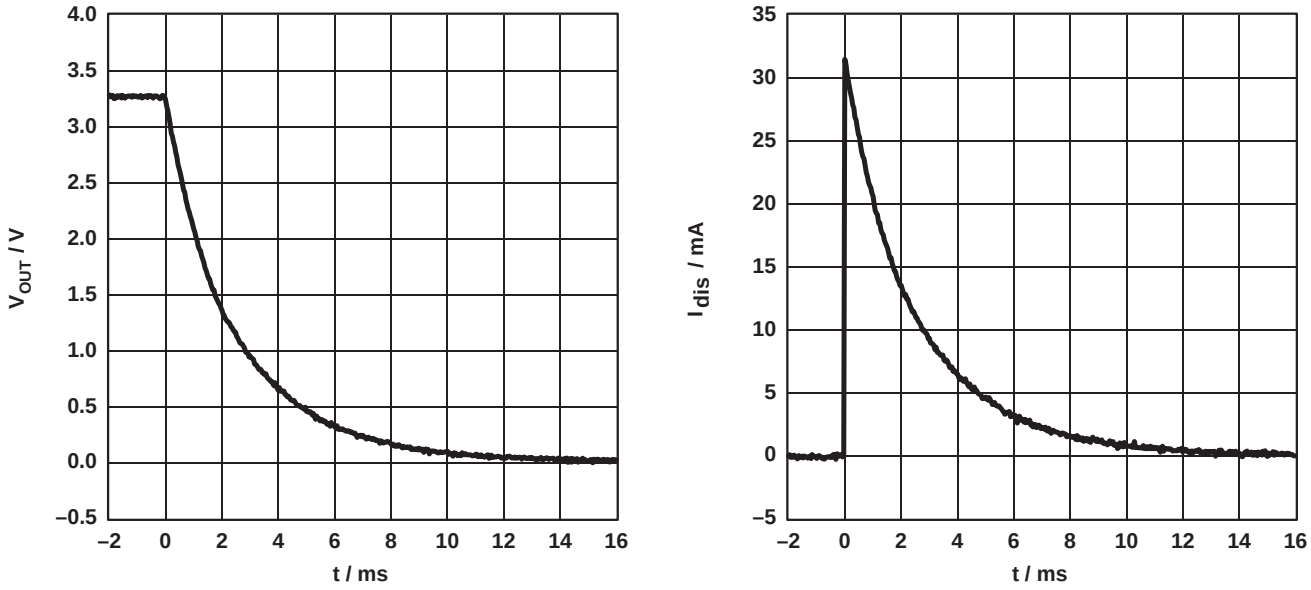

Figure 66. TPS60100: Discharge Current Without Load (buffer)

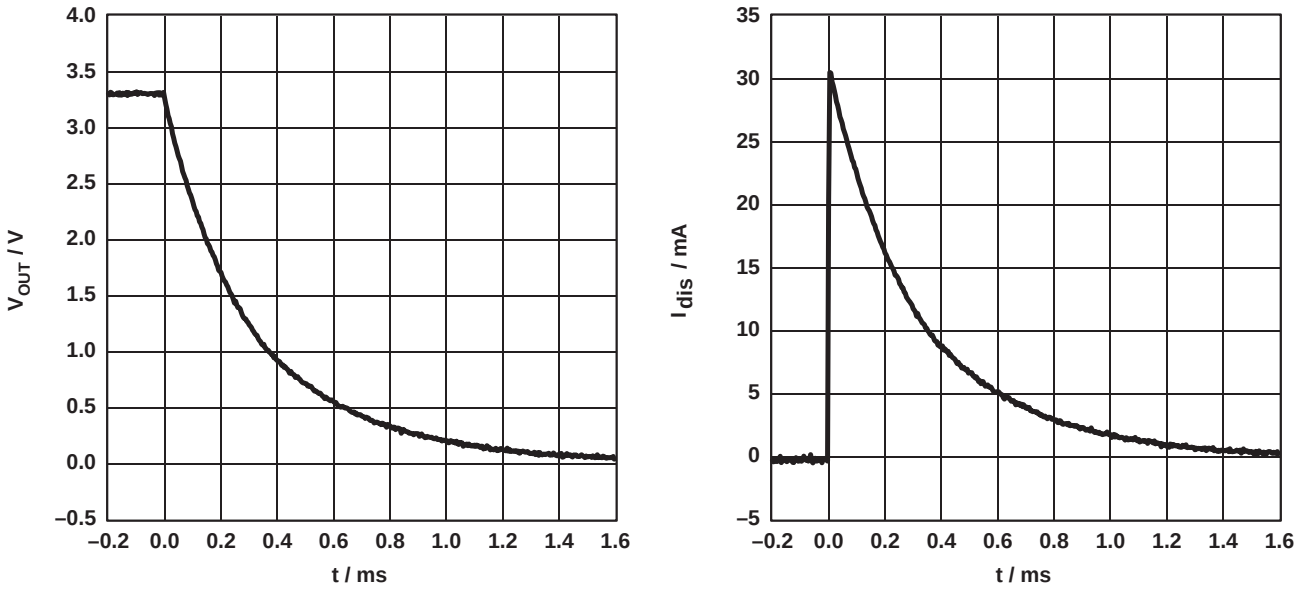

Figure 67. TPS60100: Discharge Current With 200-mA Load (buffer)

TPS60100

Figures 68 and 69 show the discharge current through, and the voltage across the buffer. The measurements are taken with a 3.6-V input voltage. The worst case is without a load; in this case the capacitor is discharged within 40 ms.

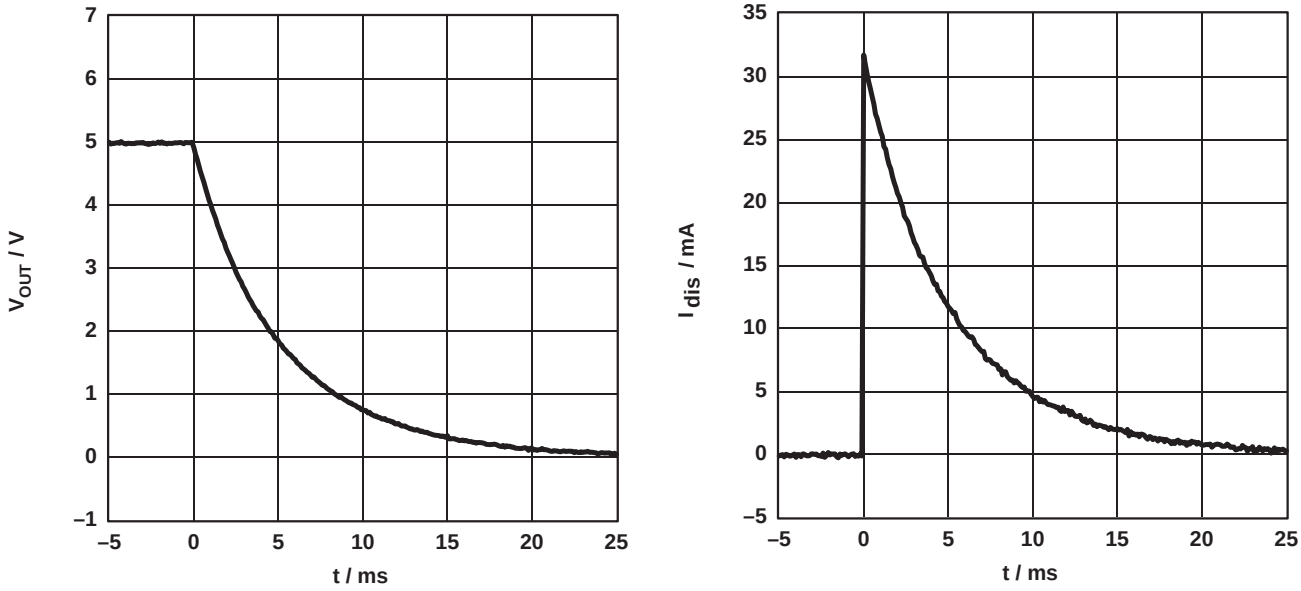

Figure 68. TPS60110: Discharge Current Without Load (buffer)

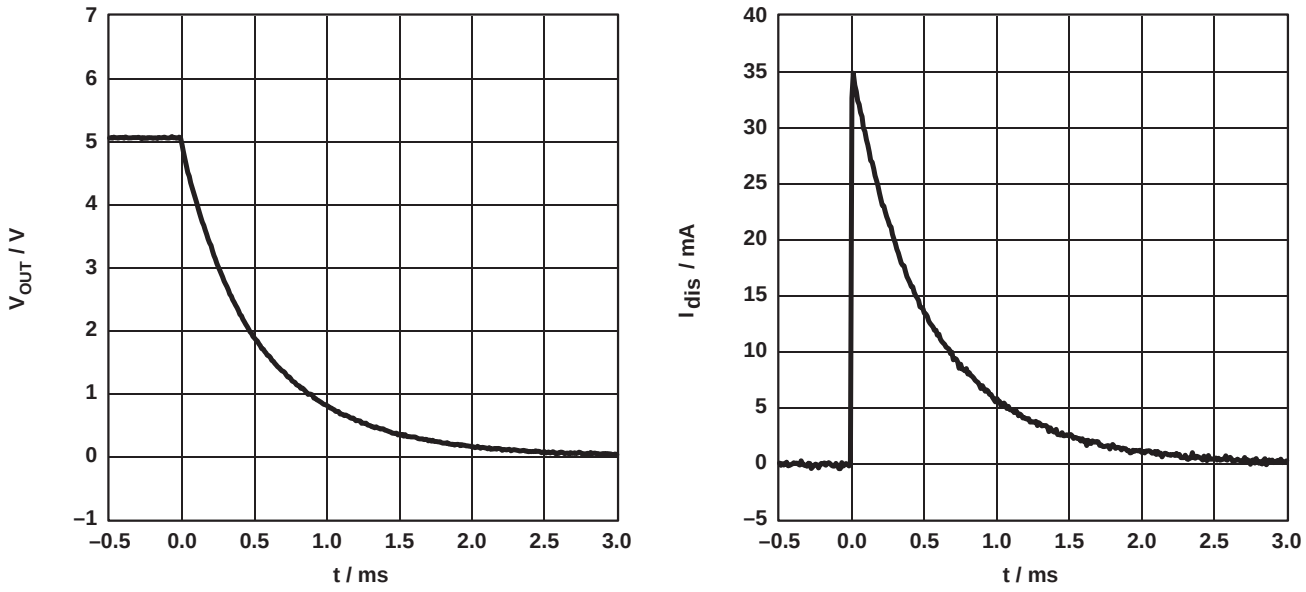

Figure 69. TPS60110: Discharge Current With 300-mA Load (buffer)

The discharge current is nearly independent of the supply voltage of the SN74LVC07A because resistor (R_{LIM}) limits the current.

The discharge time of the output capacitors is highly dependent on the load for all devices. The load current also discharges the output capacitors, and can be higher than the maximum discharge current of the SN74LVC07A. Nevertheless, this is a convenient solution for a system where the discharge time is not very critical.

5.5.2 Discharging of the Output Capacitor(s) With an NMOS Transistor

The disadvantage of the solution in Section 1.1.1 is that the discharge time is highly dependent on the load. The discharge time can vary from a few milliseconds up to tenth of milliseconds. This is not acceptable for some systems, and a solution that allows higher discharge currents is required.

Figure 70 shows the block diagram for this solution. The ENABLE signal of the TPS6010x/TPS6011x is also connected to the input of a single-gate inverter with an open-drain output (SN74AHC1G04). As long as the ENABLE signal is high, the output of the inverter is high impedance. Therefore the NMOS transistor (BSS138) is switched off. If the ENABLE signal disables the TPS6010x/ TPS6011x, the inverter drives the output to ground and the NMOS transistor switches on. The output capacitor is discharged through the transistor.

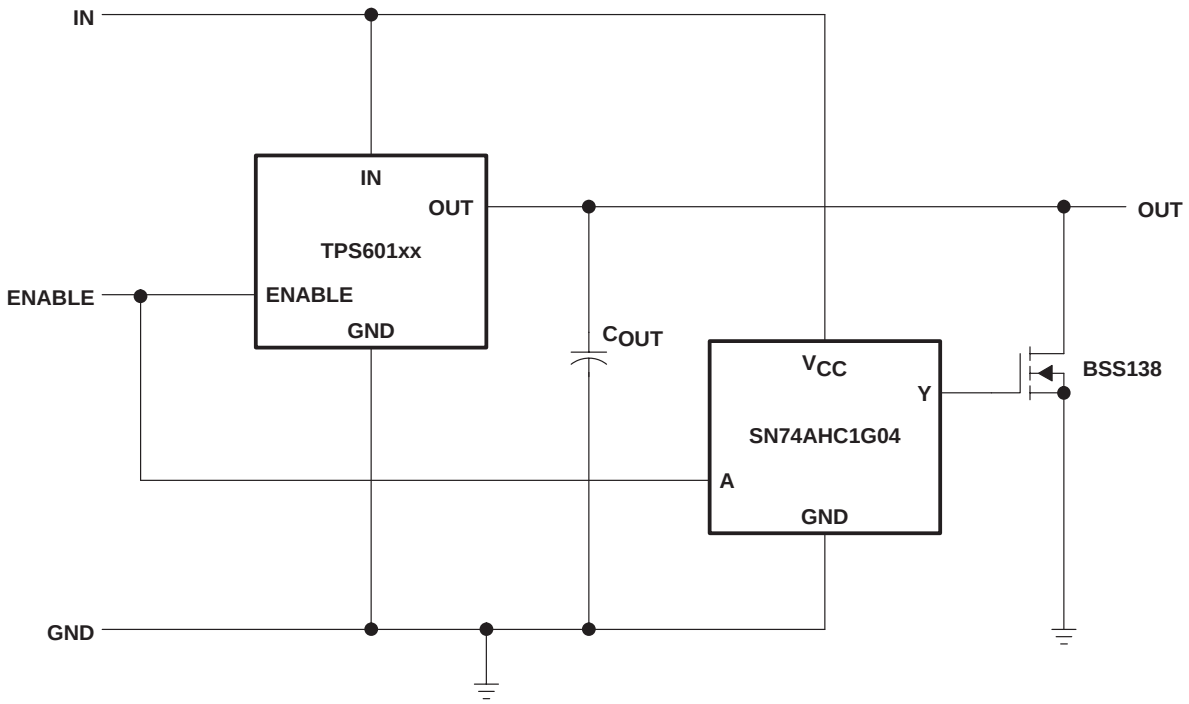

Figure 70. Block Diagram for Regulated Discharging WIth an NMOS Transistor

TPS60100

Figures 71 and 72 show the voltage across, and the discharge current through the buffer. The measurements are taken with a 2.4-V input voltage. The worst case is without a load; in this case the capacitor is discharged within 40 ms.

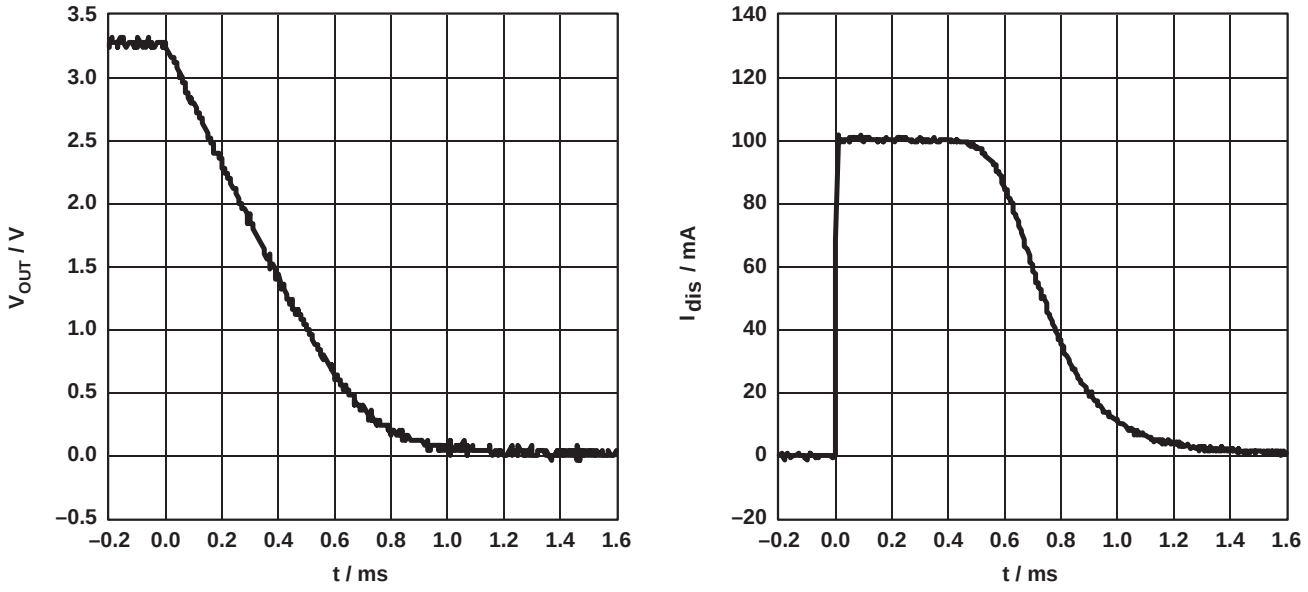

Figure 71. TPS60100: Discharge Current Without Load (NMOS)

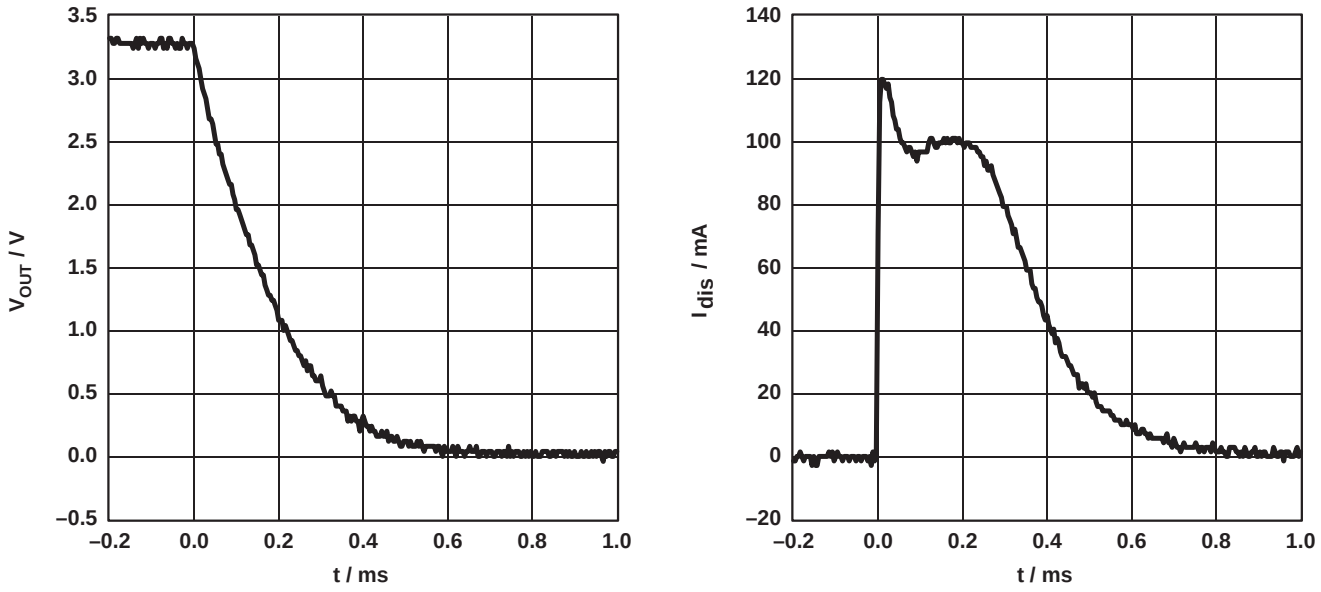

Figure 72. TPS60100: Discharge Current With 200-mA Load (NMOS)

TPS60110

Figures 73 and 74 show the voltage across, and the current through NMOS transistor (BSS138). The measurements are taken with a 3.6-V supply voltage.

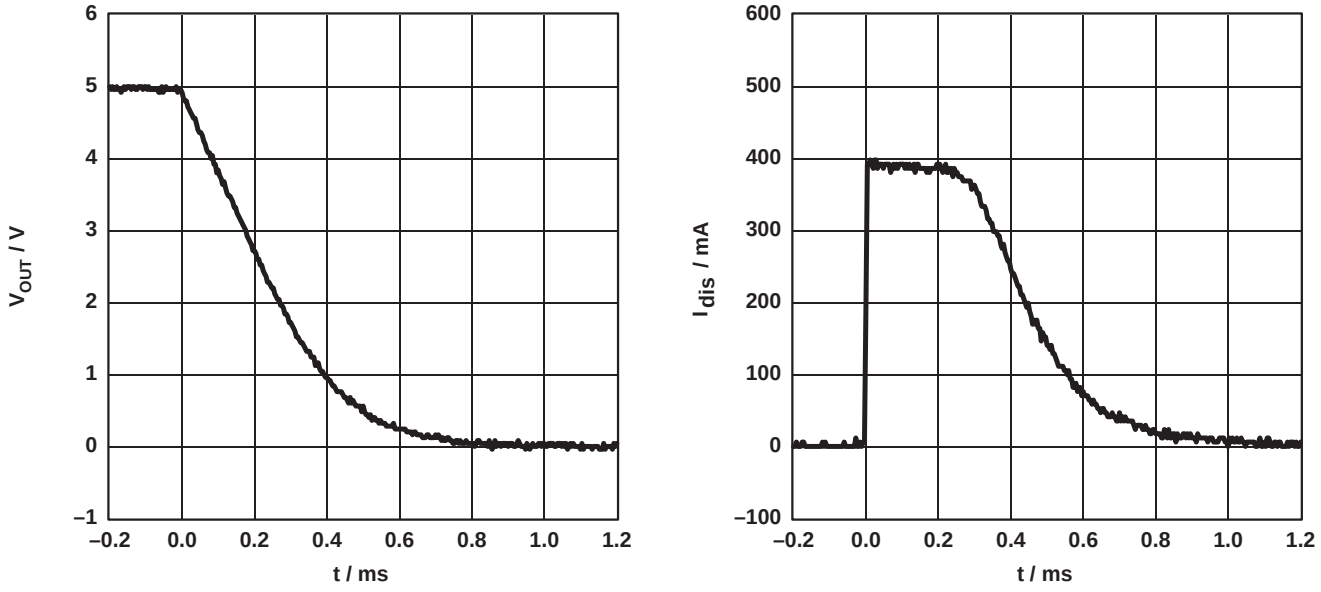

Figure 73. TPS60110: Discharge Current Without Load (NMOS)

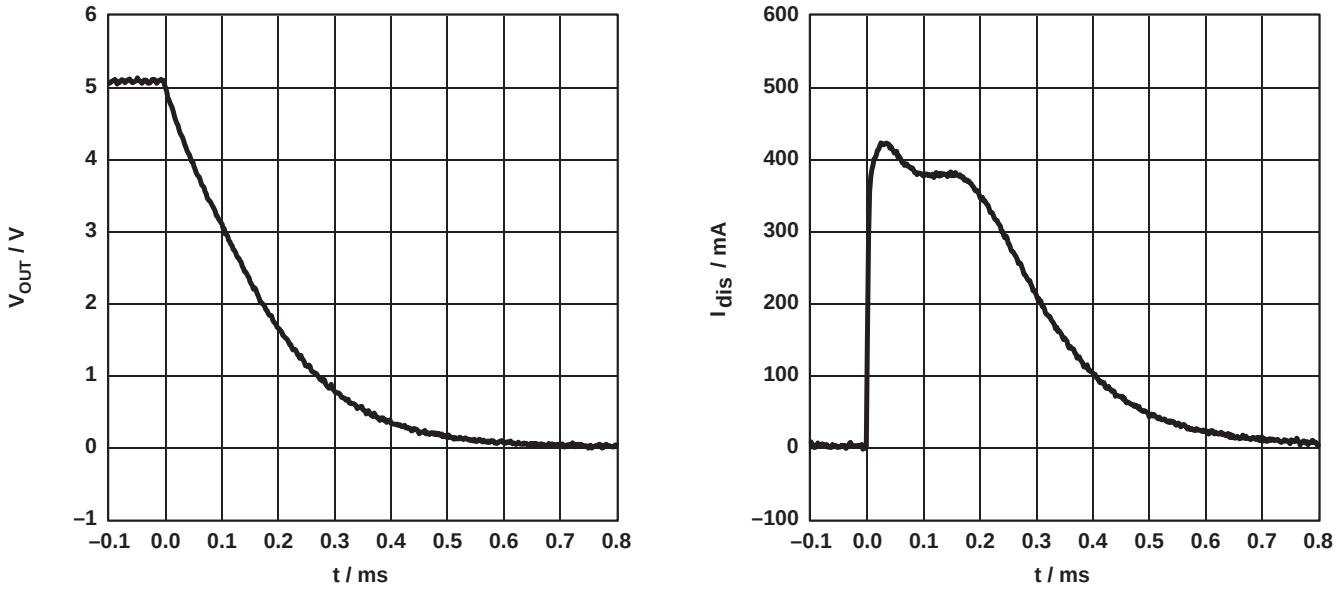

Figure 74. TPS60110: Discharge Current With 300-mA Load (NMOS)

Figures 71 through 74 show that the discharge current is nearly independent of the load. The R_{DSon} of the NMOS transistor limits the current. With a load, the discharge time is not significantly shorter. With a BSS138 NMOS transistor, the discharge time is in the range of 1 ms for both devices (TPS60100/TPS60110), independent of the load. A comparison of Figures 7 and 9, with Figures 8 and 10 shows that the discharge current depends on the supply voltage of the SN74AHC1G04. If EANBLE is low, the higher the supply voltage of the inverter, the higher the voltage between gate and source. This leads to a lower R_{DSon} of the NMOS transistor. Therefore, for this solution the discharge time is nearly independent of the load, but it depends on the supply voltage of the circuit. With the lowest supply voltage (1.8 V for the TPS60100, and 2.7 V for the TPS60110) the discharge time is still less than 7 ms for the TPS60100, or 4ms for the TPS60110. The range of the discharge time for this solution is much smaller than the one for the solution using the buffer. It only ranges between 0.5 ms and 7 ms.

6 Summary

The TPS6010x charge pump devices from Texas Instruments generate regulated 3.3-V output voltage from two-battery cells, and the TPS6011x devices generate regulated 5-V output voltage from three-battery cells. The output ripple is minimized due to the new internal structure. Two single-ended charge pumps are part of these devices and can work in anti-phase to generate this low ripple. Five logic inputs are used to operate the devices in different modes. For example, the devices can be enabled or externally synchronized. Several other modes are available to optimize the devices to the specific application. In this report, the functionality of the devices was described and a proven layout was presented. The devices are packed in a package with PowerPAD, and one section evaluated the influence of soldering this pad. Some application examples also help the designer reduce evaluation time.

7 References

1. Source for Chapter 5.2: Alexander Müller, Erich Bayer: DSP–Spannungs–versorgungen für Batteriebetriebene Geräte, Electronik Industry, Issue 5, May 1999
2. TPS60100 data sheet, Literature Number SLVS213A
3. TPS60101 data sheet, Literature Number SLVS214
4. TPS60110 data sheet, Literature Number SLVS415
5. TPS60111 data sheet, Literature Number SLVS216
6. LT1054 data sheet, Literature Number SLVS033C
7. Internet: http://www.ti.com/sc/docs/products/msp/pwrmgmt/index.htm