*User's Guide*

# *TPS542A50 SWIFT™ Step-Down Converter Evaluation Module User's Guide*


**ABSTRACT**

This user's guide describes the characteristics, operation, and use of the TPS542A50EVM-059 evaluation module (EVM). The user's guide includes test information, descriptions, and results. A complete schematic diagram, printed-circuit board layout, and bill of materials are also included in this document. Throughout this user's guide, the abbreviations *EVM*, *TPS542A50EVM*, and the term *evaluation module* are synonymous with the TPS542A50EVM-059, unless otherwise noted.


## Table of Contents



## List of Figures

## List of Tables



## Trademarks

All trademarks are the property of their respective owners.

# 1 Introduction

The TPS542A50EVM-059 evaluation module (EVM) uses the Texas Instruments TPS542A50 buck converter. The TPS542A50 is a highly integrated high-efficiency synchronous buck converter with differential remote sensing and $I^2C$. It is capable of delivering up to 15 A to a load with output voltages ranging from 0.5 V to 5.5 V. The high-side and low-side switching MOSFETs are integrated in the device package, along with their associated gate drive circuitry.

High efficiency, wide-operating junction temperature, and high output voltage accuracy make the TPS542A50 an excellent choice for applications where high output voltage accuracy across rigorous thermal conditions are required. The rated input voltage, output voltage, and output current range for the TPS542A50 are given in Table 1-1.

**Table 1-1. TPS542A50 Input Voltage and Output Current Summary**

| Converter Part Number | Input Voltage Range | Output Voltage Range | Output Current Range |
|---|---|---|---|
| TPS542A50 | 4 V to 18 V | 0.5 V to 5.5 V | 0 A to 15 A |

## 1.1 Before You Begin

The following warnings and cautions are noted for the safety of anyone using or working close to the TPS542A50EVM-059. Observe all safety precautions.

| | | |
|---|---|---|
|  | **Warning** | The TPS542A50EVM-059 circuit module may become hot during operation due to dissipation of heat. Avoid contact with the board. Follow all applicable safety procedures applicable to your laboratory. |
|  | **Caution** | Do not leave the EVM powered when unattended. |

**WARNING**

The circuit module has signal traces, components, and component leads on the bottom of the board. This may result in exposed voltages, hot surfaces or sharp edges. Do not reach under the board during operation.

**CAUTION**

The circuit module may be damaged by over temperature. To avoid damage, monitor the temperature during evaluation and provide cooling, as needed, for your system environment.

**CAUTION**

Some power supplies can be damaged by application of external voltages. If using more than 1 power supply, check your equipment requirements and use blocking diodes or other isolation techniques as needed to prevent damage to your equipment.

**CAUTION**

The communication interface is not isolated on the EVM. Be sure no ground potential exists between the computer and the EVM.

# 2 Description

The TPS542A50EVM-059 is set up to allow the user to easily measure the performance of the TPS542A50 buck converter under a wide range of input voltages and load currents. The EVM features two fully independent circuits.

The first circuit that will be discussed is the lower half, or bottom circuit, of the EVM as described in Section 3, and is denoted by U1. This circuit maximizes efficiency and performance of the TPS542A50 in applications that are less constrained by layout area. The second circuit that will be discussed is the upper half, or top circuit, of the EVM as described in Section 4, and is denoted by U1_2. This circuit highlights the small layout area (17 mm x 14 mm) that is required by the TPS542A50 converter and all external components while still delivering high performance and efficiency for space-critical applications.

The TPS542A50 features fixed-frequency voltage-mode control with user-configurable internal compensation, switching frequency, current limit, and soft-start. It also features selectable pulse-frequency modulation (PFM) for high light-load efficiency. These features can be configured using external resistors, or their respective pins can be shorted to ground and configured using $I^2C$ to reduce solution size and BOM count. Optionally, a SYNC pin for PWM control can be synchronized to an external clock for low system noise.

Other features include an enable pin, adjustable under-voltage lockout (UVLO), an open-drain power good indicator, and a typical shutdown quiescent current draw of 12 µA.

The output voltage is programmable from 0.5 V to 5.5 V, and is set with a resistive divider between SREF and AGND, with the mid-point of the divider being tapped from the VSET pin.

The low $R_{DS(on)}$ switching MOSFETs allow for high efficiency while maintaining low junction temperatures at high levels of output current. The TPS542A50 is capable of delivering 15 A of current to a load with no air flow at ambient temperatures up to 95°C, and up to 14 A with no external air flow at ambient temperatures of 105°C.

The extended operating junction temperature of -40°C to +150°C makes the TPS542A50 an excellent choice for applications with rigorous thermal requirements. Examples of these applications can be seen in Typical End-User Applications.

The rated input voltage, output voltage, and output current of both circuits featured in the TPS542A50EVM-059 are shown in Table 2-1. The nominal input voltage of the EVM is 12 V, and the default output voltage is 1 V.

**Table 2-1. EVM Input Voltage, Output Voltage, and Output Current Summary**

| TPS542A50EVM-059 | Input Voltage | Output Voltage | Output Current |
|---|---|---|---|
| Bottom circuit | 4 V to 18 V (12 V nominal) | 1 V (default) | 0 A to 15 A |
| Top circuit (small layout area) | 4 V to 18 V (12 V nominal) | 1 V (default) | 0 A to 12 A |

## 2.1 Typical End-User Applications

- Enterprise storage, SSD, NAS
- Wireless and wired communication infrastructure
- Industrial PCs, automation, ATE, PLC, video surveillance
- Enterprise server, switches, routers
- ASIC, SoC, FPGA, DSP core and I/O rails

## 2.2 EVM Features

- Regulated 1-V output up to 15 A, steady-state output current
- Convenient test points for probing critical waveforms
- Two fully independent circuits
- USB-TO-GPIO interface for convenient $I^2C$ Programming (optional)

## 2.3 TPS542A50EVM-059 PCB

A top-down 3D view of the TPS542A50EVM-059 is shown in Figure 2-1. Some components are not populated by default. As previously described, the EVM features two fully independent circuits. The layers of the EVM PCB are presented in greater detail in Section 5.

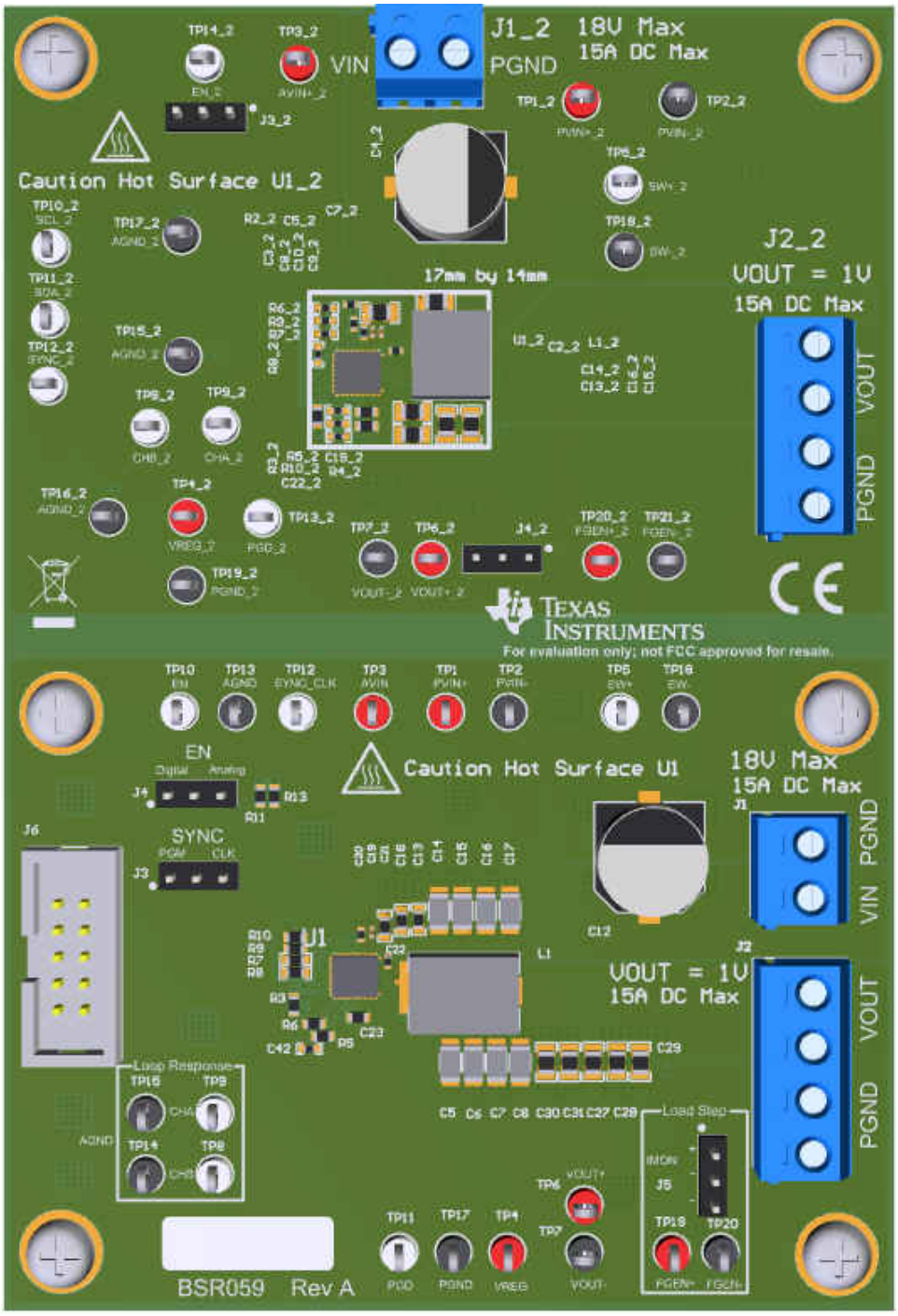


**Figure 2-1. TPS542A50EVM-059 PCB View**

# 3 TPS542A50EVM-059 Bottom Circuit

The first circuit that will be discussed is the bottom (lower) circuit on the TPS542A50EVM-059 shown in Figure 2-1. In this circuit, the TPS542A50 converter IC is indicated as "U1". This circuit has been designed to highlight the performance and efficiency of the TPS542A50 across a wide range of operating conditions. The schematic for this circuit is shown in Figure 3-1.

## 3.1 Modifications

This EVM is designed to provide access to the features of the TPS542A50-EVM. Some of the useful modifications are outline in this section of the user's guide.

### 3.1.1 Output Voltage Setpoint

The output voltage is set by the resistor divider network of R5 and R6, as shown in Figure 3-1. The divider is connected between SREF and AGND pins, where the mid-point of the divider is tapped to the VSET pin. Unlike many converters, the output voltage is not set by connecting a resistor divider directly to the output node. This allows the use of a differential remote sense for improved output voltage accuracy.

It is recommended to use R5 and R6 in the range of 1 kΩ to 100 kΩ, and the total impedance must be greater than 10 kΩ. A footprint for a small capacitor, C42, has been added for high frequency noise filtering, but is typically not necessary and is not populated by default.

The value of R5 for a desired output voltage, $V_{OUT}$, can be calculated using Equation 1.

$$R5 = R6 \times \left( \frac{5 \times V_{SREF}}{V_{OUT}} - 1 \right) \quad (1)$$

$V_{SREF}$ = 1.2 V

R6 = 20.0 kΩ (default EVM value)

Note that for output voltages below 1 V, the value of R6 should be reduced to keep R5 and R6 between 1 kΩ and 100 kΩ, while still maintaining a total impedance greater than 10 kΩ.

Using $I^2C$, the TPS542A50 output voltage can be adjusted in 0.25% increments from -20% to +10% of the set output voltage. This allows the tolerance of the resistors used to set the output voltage to be completely eliminated, and gives an output voltage accuracy of -0.5% to +0.5% across the entire temperature range. Note that this adjustment to the output voltage over $I^2C$ can only be performed after PGOOD goes high.

### 3.1.2 Enable and Undervoltage Lockout

The operation of the TPS542A50 can be enabled or disabled using J4. The EN pin of the TPS542A50 is connected to J4-2 (pin 2 of J4) and TP10. The EN pin threshold is 1.2 V. By leaving J4-2 floating, a pullup current source internal to the TPS542A50 enables the device, and the device is operational across all valid input voltages (4 V - 18 V).

Undervoltage lockout (UVLO) can be implemented by connecting a jumper between J4-2 and J4-3. In this configuration, R11 and R13 should be populated according to the TPS542A50 device data sheet based on the desired UVLO requirements. By default, R11 and R13 are not populated.

The TPS542A50 can be disabled by pulling J4-2 (the EN pin) below 1.2 V. When J4-2 is brought below 1.2 V, the regulator stop switching and enters into a low power shutdown mode. This can be accomplished in multiple ways.

The first method is to connect a control signal directly to the EN test point (TP10), referenced to AGND (TP13, TP14, or TP15, recommended between 0 V and 5.5 V). Using this method, a jumper on J4 is not necessary.

Another method is to connect a jumper between J4-1 and J4-2, and connect a control signal to J6-1, or use a TI USB-TO-GPIO connected to J6 to control the EN pin.

Default setting: J4 open, EN floating for always-on operation.

**Table 3-1. Enable Pin Selection**

| J4 connection | Enable Selection |
|---|---|
| J4-2 floating | Device is enabled |
| J4-2 and J4-3 shorted | UVLO implemented if R11 and R13 are populated - see data sheet for details |
| J4-1 and J4-2 shorted | Enable can be controlled with external control signal |

### 3.1.3 Programming and External Clock Synchronization

To enter programming mode or use external clock synchronization, J3 is used. To program the TPS542A50, the SYNC pin must be brought high while keeping the EN pin low. The device is then programmed via the $I^2C$ pins, SCL (J6-9) and SDA (J6-10). If J6 is used to program the TPS542A50 via a TI USB-TO-GPIO programmer, a jumper should be placed between J3-1 and J3-2. After the device is enabled, all registers are read-only. Details on the valid $I^2C$ registers and instructions are provided in the TPS542A50 data sheet.

An external signal (recommended 0-V to 3.3-V) can be used as an external clock synchronization source. To use this feature, the TPS542A50 must be enabled, either by pulling the EN pin high or leaving it floating as described in Enable and Undervoltage Lockout. A jumper should be placed between J3-2 and J3-3, and the external clock signal should be applied to the SYNC_CLK (TP12) test point, referenced to AGND. The external clock synchronization signal applied to the SYNC pin must also be within -10% to +10% of the configured switching frequency. This is true whether the switching frequency is selected using a resistor from FSEL to AGND (R10), or selected via $I^2C$.

### 3.1.4 Load Step with Function Generator

The TPS542A50EVM-059 provides a convenient location to connect a function generator for applying load steps to the output. The postive and negative connections of the function generator are applied to FGEN+ (TP19) and FGEN- (TP20), respectively. It is recommended that a 50-Ω termination on the output of the function generator is configured.

The FGEN+ input drives the gate of a Texas Instruments CSD17527Q5A N-Channel NexFET Power MOSFET. Two 0.02-Ω resistors in parallel (R14, R15), connected from the source of the CSD17527Q5A to PGND, provide a 0.01-ohm resistance to measure the voltage across for determining output current, which is nominally equal to 10 mV/A. The voltage across these two resistors is measured from J5-1 and J5-2/3, for the positive and negative terminals, respectively. TI recommends driving the CSD17527Q5A gate with at least 5 V to minimize the $R_{DS(on)}$ of the CSD17527Q5A. The safe operating area of the CSD17527Q5A must be observed at all times when using this feature.

## 3.2 TPS542A50EVM-059 Bottom Circuit Schematic

The schematic of the bottom circuit of the TPS542A50EVM-059 is shown in Figure 3-1. The components that are not populated by default are shown with a red "X" through them.

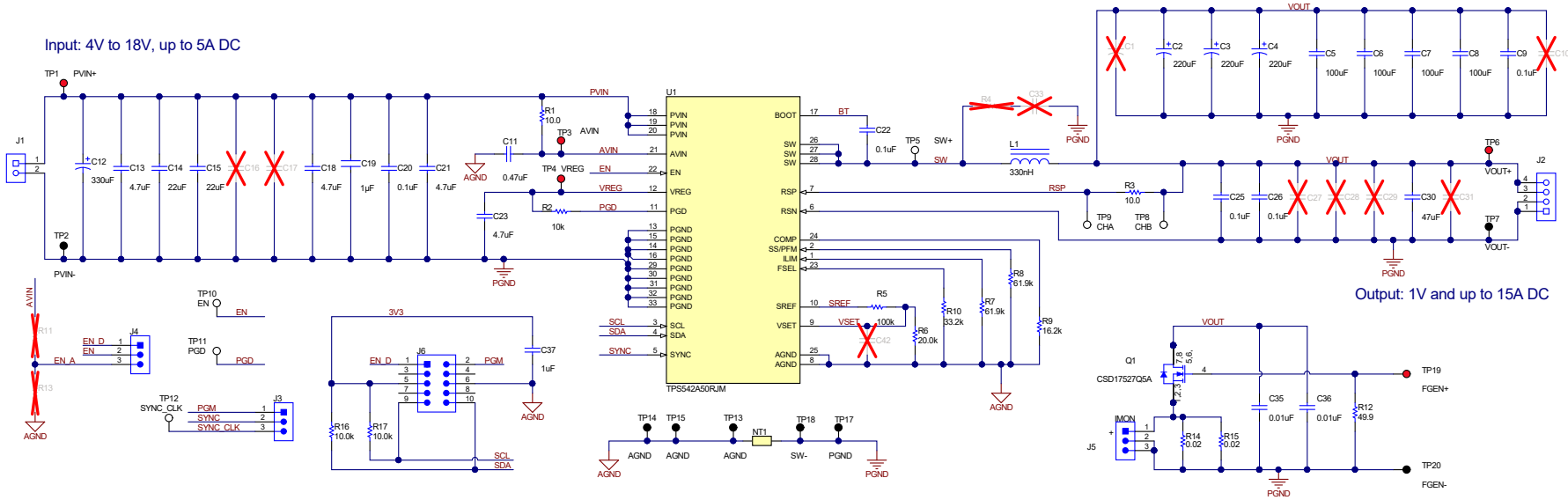


**Figure 3-1. TPS542A50EVM-059 Bottom Circuit Schematic**

## 3.3 Test Setup and Results

This section descibes how to properly connect, set up, and use the bottom circuit of the TPS542A50EVM-059. This section also includes test results typical for the evaluation module and covers efficiency, power loss, load regulation, transient response, loop response, output voltage ripple, and thermal data. For a more complete set of data, please refer to the TPS542A50 data sheet.

### 3.3.1 Input/Output Connections

The TPS542A50EVM-059 is provided with input/output connectors and test points as shown in Table 3-2. A power supply capable of supplying at least 5 A at the desired EVM input voltage must be connected to J1 through a pair of 20-AWG or greater wires. The load must be connected to J2 through a pair of 18-AWG or greater wires. The maximum load current capability is 15 A.

Wire lengths must be minimized to reduce losses and parasitic inductance in the wires. PVIN+ (TP1) provides a test point to monitor the VIN input voltages with PVIN- (TP2) providing a convenient reference to PGND. VOUT+ (TP6) is used to monitor the output voltage with VOUT- (TP7) providing a reference to PGND.

**Table 3-2. Top Circuit Connections and Test Points**

| Connection and Test Points | Description |
|---|---|
| J1 | VIN, PGND connection (see Table 1-1 for input voltage range) |
| J2 | VOUT, PGND connection: 5.5 V at 15 A maximum (default is 1 V out at 15 A) |
| J3 | Programming mode and external clock synchronization |
| J4 | Enable configuration |
| J5 | Output current sensing points when using function generator as load control signal |
| J6 | For connecting a TI USB-TO-GPIO programmer |
| PVIN+ (TP1), PVIN- (TP2) | VIN voltage sensing test points |
| VOUT+ (TP6), VOUT- (TP7) | VOUT voltage sensing test points |
| AVIN (TP3) | AVIN voltage sensing test points |
| VREG (TP4) | VREG voltage sensing test point |
| SW+ (TP5), SW- (TP18) | SW node sensing test points |
| CHA (TP9), CHB (TP8) | Loop measurement test points |
| EN (TP10) | EN pin test point |
| PGD (TP11) | Open-drain PGD test point |
| SYNC_CLK (TP12) | For connecting and measuring external clock synchronization |
| AGND (TP13, TP14, TP15) | AGND connection - multiple provided to reduce oscilloscope ground probe loop inductance |
| PGND (TP17) | PGND connection |
| FGEN+ (TP19), FGEN- (TP20) | Function generator connection points - referenced to PGND |

### 3.3.2 Start Up Procedure

1. Make sure the EN jumper (J4) is open to float the EN pin, enabling the TPS542A50. Alternatively, the device can be enabled as described in Enable and Undervoltage Lockout.
2. If using an external load, connect the load to VOUT and PGND of J2 using copper wire capable of handling at least 15 A (18-AWG or greater). If using the built-in load with a function generator, connect the positive and negative connections of the function generator to FGEN+ (TP19) and FGEN- (TP20), respectively.
3. Apply appropriate VIN voltage to the VIN and PGND terminals of J1.

### 3.3.3 Electrical Performance Specifications and Results

The typical electrical perfomance specifications of the TPS542A50EVM bottom circuit are shown in Table 3-3. Unless stated otherwise, the measurements were taken with the converter operating in FCCM and $T_{AMB}$ = 25°C.

**Table 3-3. Bottom Circuit Electrical Performance Specifications**

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $V_{IN}$ voltage range | | 5 | 12 | 14 | V |

**Table 3-3. Bottom Circuit Electrical Performance Specifications (continued)**

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Output voltage | | | 1 | | V |
| Output current range | | 0 | | 15 | A |
| Load regulation | $V_{IN}$ = 12 V, $I_O$ = 0 A to 15 A, FCCM | -0.2 | | +0.2 | % |
| $\Delta V_{OUT}$, total undershoot/overshoot | $V_{IN}$ = 12 V, $I_O$ = 2-A to 12-A to 2-A load step @ 10 A/µs | | 91 | | mV |
| Loop bandwidth | $V_{IN}$ = 12 V, $I_O$ = 10 A | | 120 | | kHz |
| Phase margin | $V_{IN}$ = 12 V, $I_O$ = 10 A | | 65 | | ° |
| Output voltage ripple | $V_{IN}$ = 12 V, $I_O$ = 0 A | | 12.1 | | mV |
| | $V_{IN}$ = 12 V, $I_O$ = 10 A | | 12.1 | | mV |
| IC case temperature | $V_{IN}$ = 12 V, $I_O$ = 15 A, $T_{amb}$ = 25C | | 78.4 | | °C |
| Switching frequency | FCCM | | 1000 | | kHz |

### 3.3.4 Efficiency

Figure 3-2 shows the efficiency of the TPS542A50EVM-059 when operating in forced continuous-conduction mode (FCCM). The light-load efficiency can be improved by operating the converter in DCM as described in the TPS542A50 data sheet. The default setting on the EVM is FCCM operation.

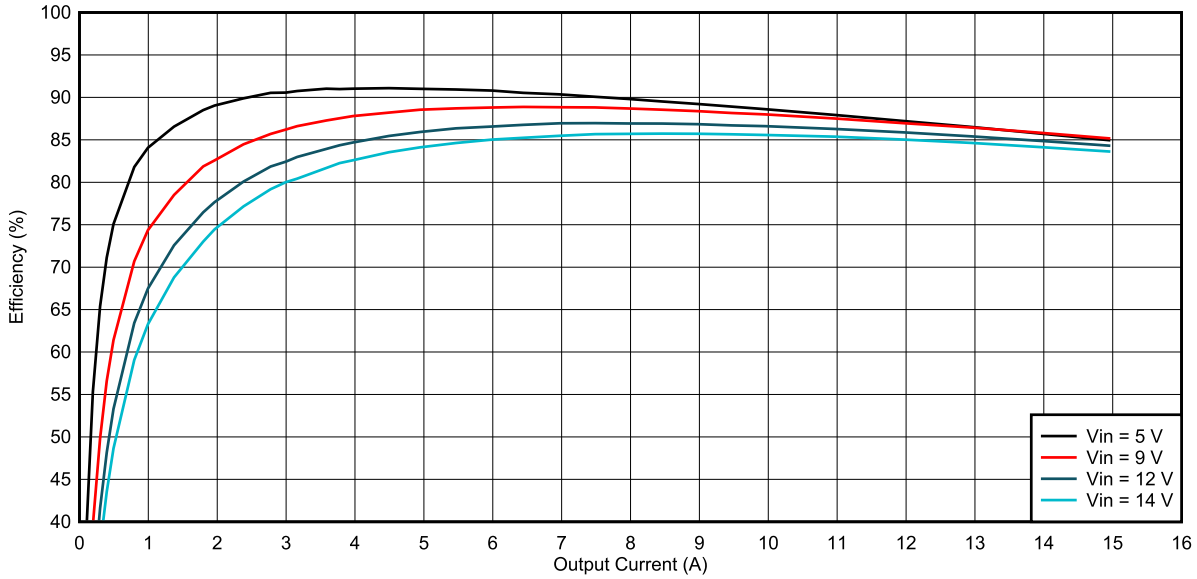


**Figure 3-2. Efficiency - FCCM, $f_{sw}$ = 1000 kHz, $T_{amb}$ = 25°C**

### 3.3.5 Power Loss

The power loss of the bottom circuit when operating in FCCM is shown in Figure 3-3. The power loss includes all losses of the converter, including the losses of the output inductor.

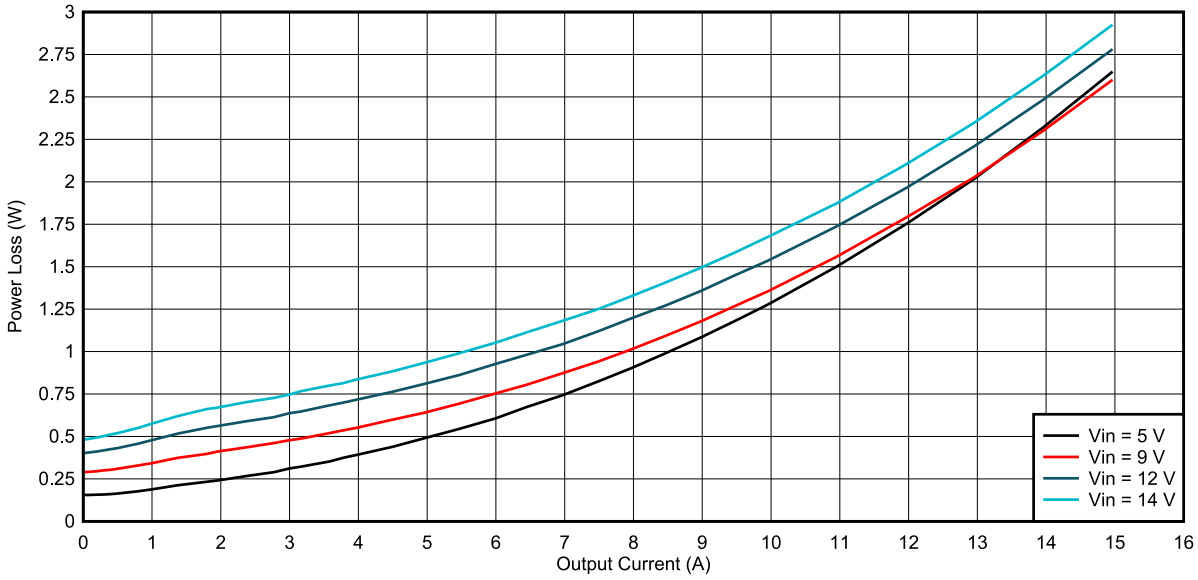


**Figure 3-3. Power Loss - FCCM, $f_{sw}$ = 1000 kHz, $T_{amb}$ = 25°C**

### 3.3.6 Load Regulation

The EVM bottom circuit load regulation for ambient temperatures of -40°C to +105°C and input voltages of 5 V and 12 V is shown in Figure 3-4.

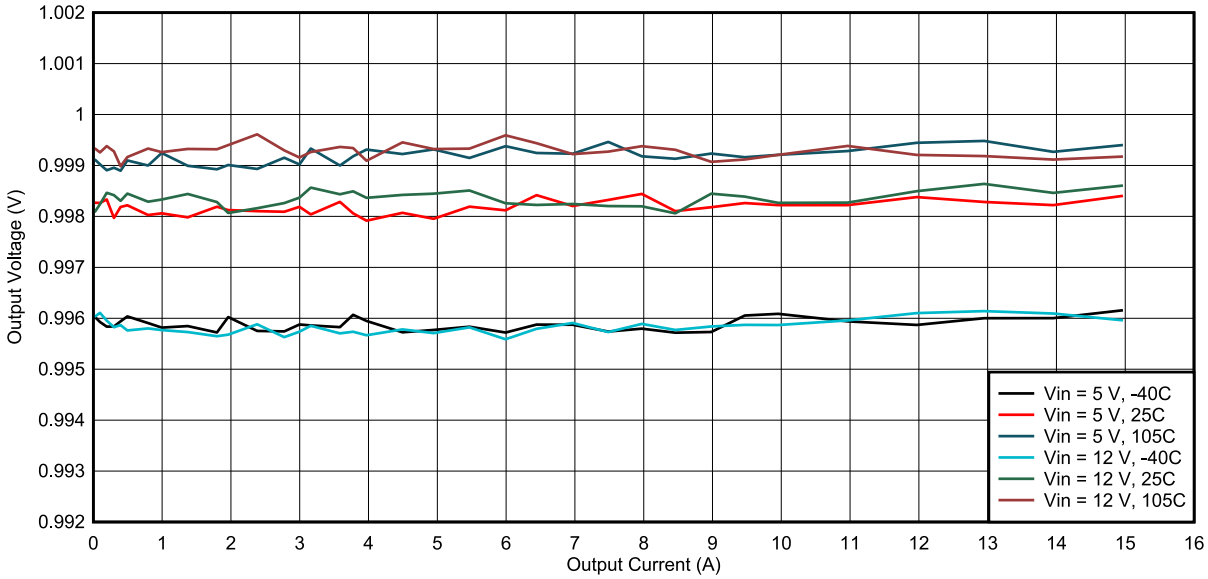


**Figure 3-4. Load regulation - FCCM, $f_{sw}$ = 1000 kHz, $T_{amb}$ = -40°C to +105°C**

### 3.3.7 Transient Response

Figure 3-5 shows the transient response of the converter when operating in FCCM. The total undershoot and overshoot in response to a 10-A load transient (2-A to 12-A to 2-A) with a slew rate of 10 A/µs is 91.1 mV.

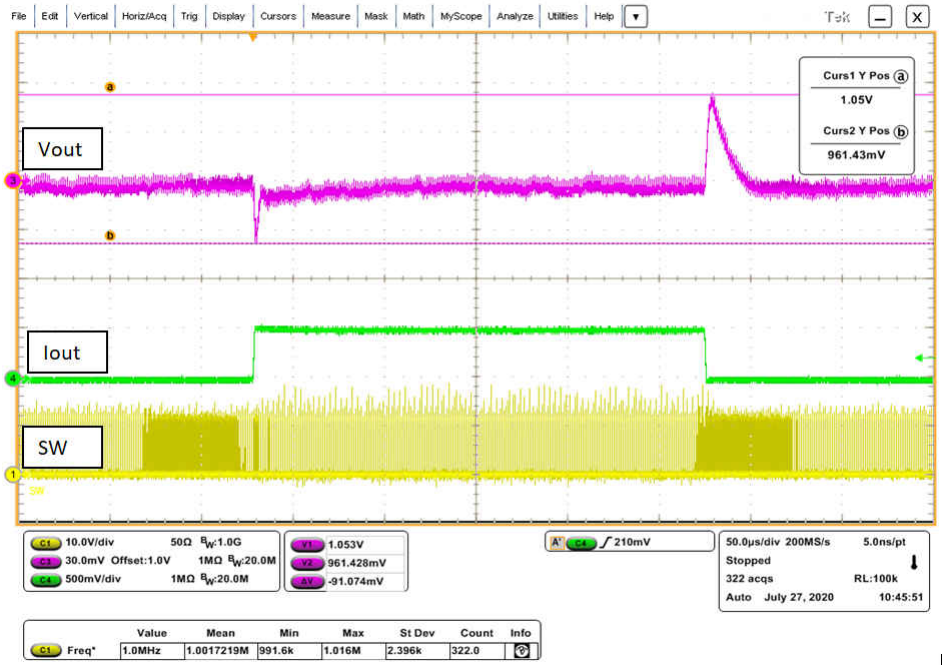


**Figure 3-5. Transient response - 2-A to 12-A to 2-A load @10 A/µs, ΔVout = 91.1 mV, $f_{sw}$ = 1000 kHz, FCCM**

### 3.3.8 Loop Response

The loop response of the bottom circuit of the TPS542A50EVM-059 with a 10-A load is shown in Figure 3-6. The bandwidth of the loop is 120 kHz, and the phase margin is 65°.

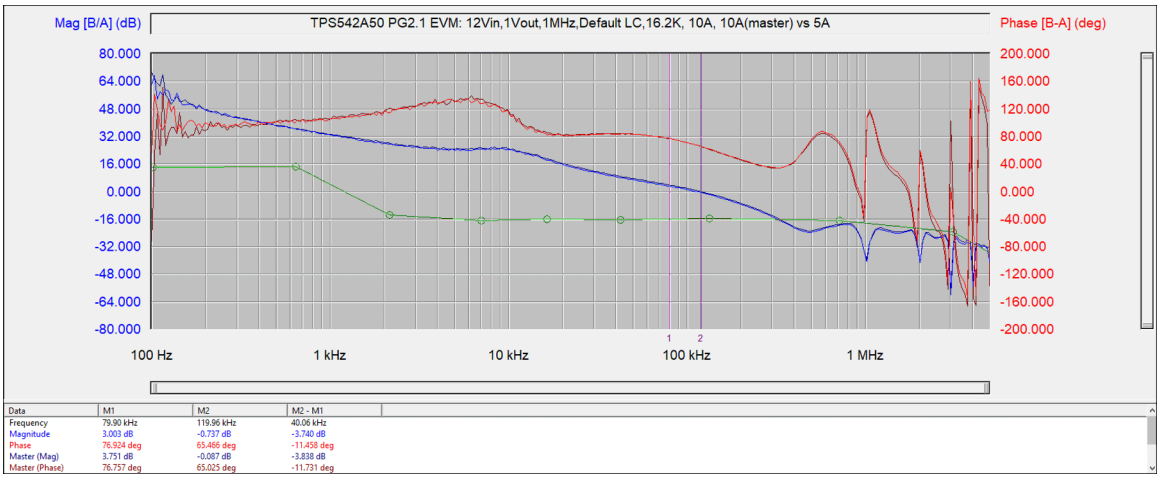


**Figure 3-6. Loop response - $I_{OUT}$ = 10 A, Loop Bandwidth = 120 kHz, Phase Margin = 65°**

### 3.3.9 Output Voltage Ripple

Figure 3-7 shows an output voltage ripple of 12.1 mV with a load of 0 A. Figure 3-8 shows an output voltage ripple of 12.1 mV with a load of 10 A.

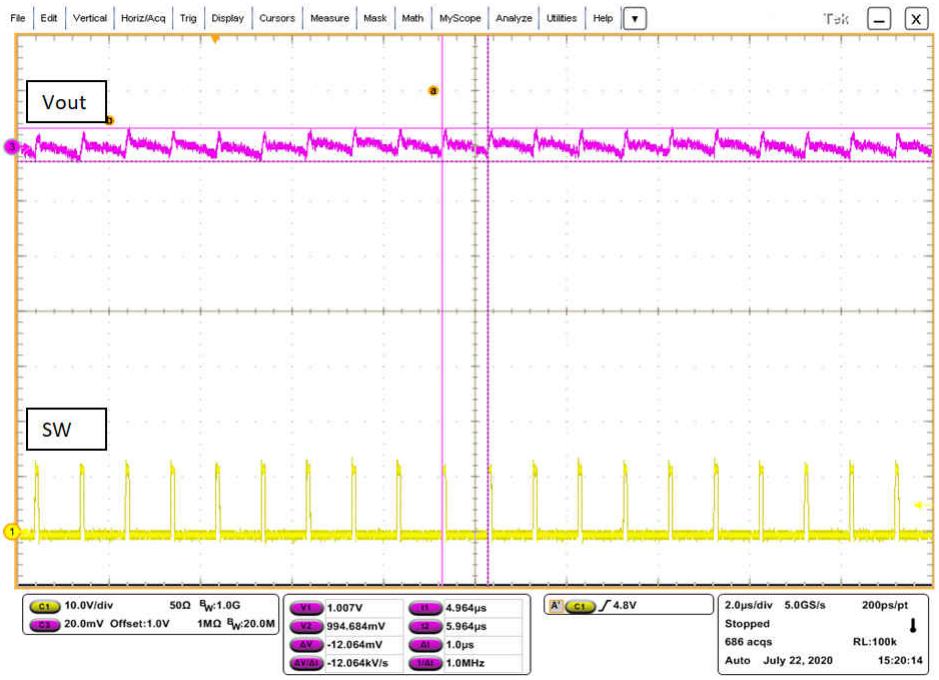


**Figure 3-7. Output voltage ripple - 0-A load, ΔVout = 12.1 mV, $f_{sw}$ = 1000 kHz, FCCM**

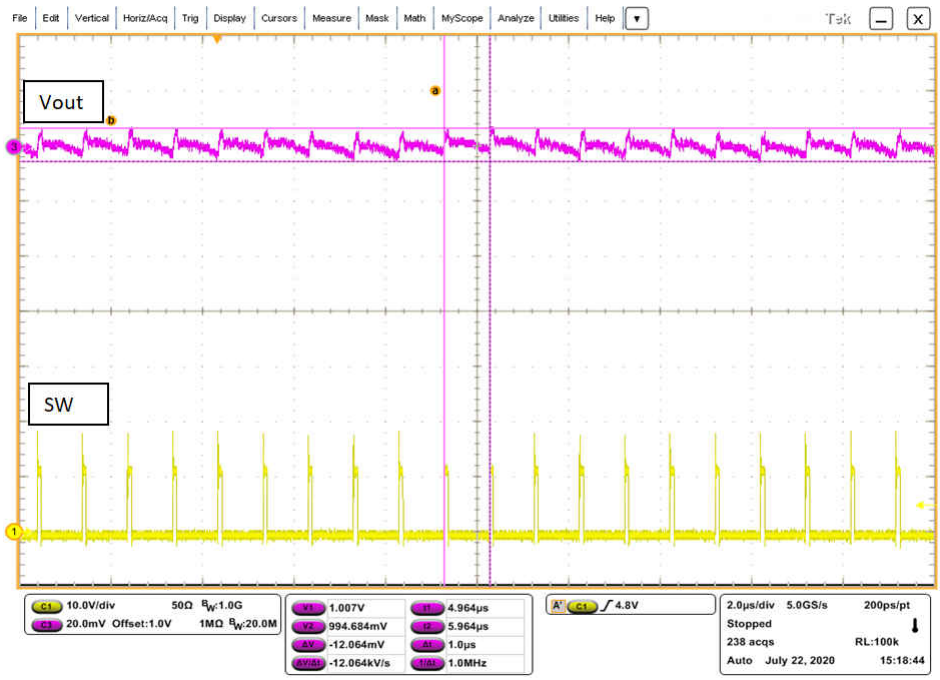


**Figure 3-8. Output voltage ripple - 10-A load, ΔVout = 12.1 mV, $f_{sw}$ = 1000 kHz, FCCM**

### 3.3.10 Thermal Data

Figure 3-9 shows a thermal image of the TPS542A50 operating at a load current of 15 A and $T_{amb}$ = 25°C. The IC case temperature is 78.4°C.

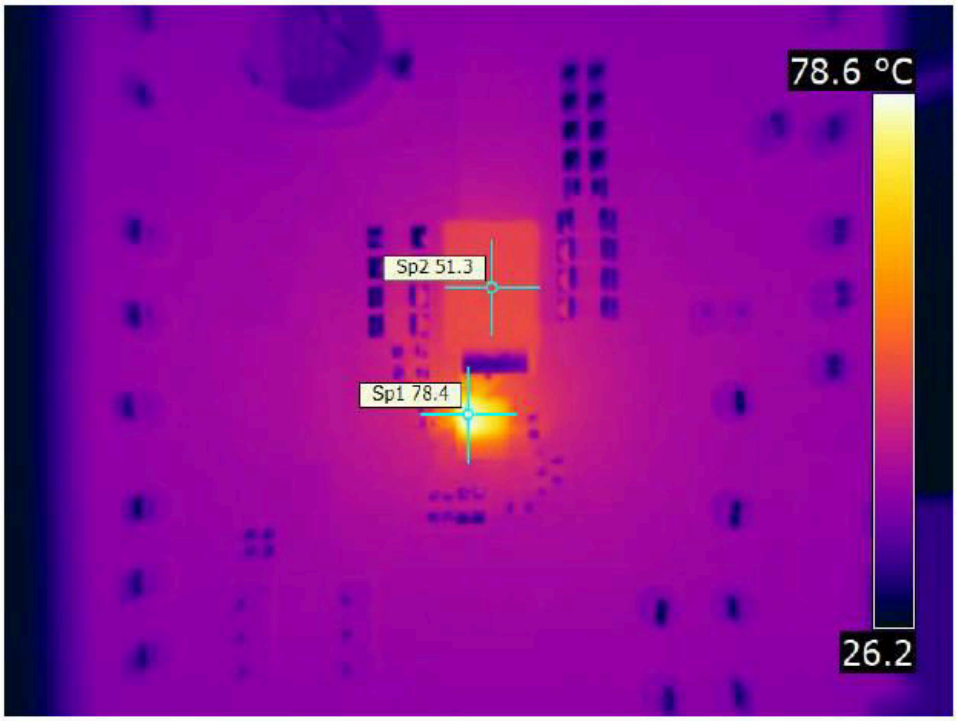


**Figure 3-9. Thermal Image - 15-A load, $T_{CASE}$ = 78.4°C, $T_{amb}$ = 25°C**

# 4 TPS542A50EVM-059 Top Circuit (Small layout area design)

The second circuit that will be discussed is the top (upper) circuit on the TPS542A50EVM-059 shown in Figure 2-1. In this circuit, the TPS542A50 converter IC is indicated as U1_2. This circuit has been designed with a minimal layout area for applications where space is limited. The default switching frequency is 1.2 MHz, which allows for the use of smaller output inductance and capacitance. The converter and all associated components fit inside a 17 mm x 14 mm layout area (238 $mm^2$) while still delivering high performance for space-critical applications.

## 4.1 Modifications

This EVM is designed to provide access to the features of the TPS542A50EVM-059. Some of the useful modifications are outline in this section of the user's guide.

### 4.1.1 Output Voltage Setpoint

The output voltage is set by the resistor divider network of R5_2 and R10_2, as shown in Figure 4-1. The divider is connected between SREF and AGND pins, where the mid-point of the divider is tapped to the VSET pin. Unlike many converters, the output voltage is not set by connecting a resistor divider directly to the output node. This allows the use of a differential remote sense for improved output voltage accuracy.

It is recommended to use R5_2 and R10_2 in the range of 1 kΩ to 100 kΩ, and the total impedance must be greater than 10 kΩ. A footprint for a small capacitor, C22_2, has been added for high frequency noise filtering, but is typically not necessary and is not populated by default..

The value of R5_2 for a desired output voltage, $V_{OUT}$, can be calculated using Equation 2.

$$R5\_2 = R10\_2 \times \left(\frac{5 \times V_{SREF}}{V_{OUT}} - 1\right) \quad (2)$$

$V_{SREF}$ = 1.2 V

R10_2 = 20.0 kΩ

Note that for Vout below 1 V, the value of R10_2 should be reduced to keep R5_2 and R10_2 between 1 kΩ and 100 kΩ, while still maintaining a total impedance greater than 10 kΩ.

Using $I^2C$, the TPS542A50 output voltage can be adjusted in 0.25% increments from -20% to +10% of the set output voltage. This allows the tolerance of the resistors used to set the output voltage to be completely eliminated, and gives an output voltage accuracy of -0.5% to +0.5% across the entire temperature range. Note that this adjustment to the output voltage over $I^2C$ can only be performed after PGOOD goes high.

### 4.1.2 Enable and Undervoltage Lockout

The operation of the TPS542A50 can be enabled or disabled using J3_2. The EN pin of the TPS542A50 is connected to J3_2-2 (pin 2 of J3_2) and TP14_2. The EN pin threshold is 1.2 V. By leaving J3_2-2 floating, a pullup current source internal to the TPS542A50 enables the device, and the device is operational across all valid input voltages (4 V - 18 V).

Undervoltage lockout (UVLO) can be implemented by connecting a jumper between J3_2-2 and J3_2-3. In this configuration, R12_2 and R15_2 should be populated according to the TPS542A50 device data sheet based on the desired UVLO requirements. By default, R12_2 and R15_2 are not populated.

The TPS542A50 can be disabled by pulling J3_2-2 (the EN pin) below 1.2 V. When J3_2-2 is brought below 1.2 V, the regulator stop switching and enters into a low power shutdown mode.

To externally control the EN pin of the TPS542A50, a control signal referenced to AGND (TP15_2, TP16_2, or TP17_2, recommended between 0 V and 5.5 V) can be connected directly to the EN_2 test point (TP14_2). Using this method, a jumper on J3_2 is not necessary.

The converter can be put into shutdown mode manually by connecting a jumper between J3_2-2 and J3_2-1, which grounds the EN pin.

Default setting: J3_2 open, EN floating for always-on operation.

**Table 4-1. Enable Pin Selection**

| J3_2 connection | Enable Selection |
|---|---|
| J3_2-2 floating | Device is enabled |
| J3_2-2 and J3_2-3 shorted | UVLO implemented if R12_2 and R15_2 are populated - see data sheet for details |
| J3_2-1 and J3_2-2 shorted | Converter is disabled |

### 4.1.3 Programming and External Clock Synchronization

To enter programming mode, the SYNC pin (TP12_2) must be brought high while keeping the EN pin (J3_2-2 or TP14_2) low. The device is then programmed via the $I^2C$ pins (SCL and SDA). In this circuit, the SCL pin is connected to TP10_2, and the SDA pin is connected to TP11_2. After the device is enabled, all registers are read-only. Details on the valid $I^2C$ registers and instructions are provided in the TPS542A50 data sheet.

**Note**

This circuit does not have $I^2C$ pull-up resistors and must be provided by externally or by the $I^2C$ master device. The maximum recommended $I^2C$ pull-up voltage is 5.5 V.

An external signal (recommended 0-V to 3.3-V) can be used as an external clock synchronization source. To use this feature, the TPS542A50 must be enabled by bringing the EN pin (J3_2-2 or TP14_2) high, or leaving it floating. The external clock synchronization signal should be applied to the SYNC (TP12_2) pin, referenced to AGND. The external clock synchronization source must also be within -10% to +10% of the set switching frequency. This is true whether the switching frequency is selected using a resistor from FSEL to AGND (R6_2), or selected via $I^2C$.

### 4.1.4 Load Step with Function Generator

The TPS542A50EVM-059 has a built-in load that can be controlled using the function generator inputs, FGEN+_2 (TP20_2) and FGEN-_2 (TP21_2). The positive connection of the function generator output is connected to FGEN+_2, and the negative connection of the function generator is connected to FGEN-_2. It is recommended that a 50-Ω termination on the output of the function generator is configured.

The FGEN+_2 input drives the gate of a Texas Instruments CSD17527Q5A N-channel NexFET Power MOSFET. Two 0.02-ohm resistors in parallel (R13_2, R14_2), connected from the source of the CSD17527Q5A to PGND, provide a 0.01-ohm resistance to measure the voltage across to determine output current, which is equal to approximately 10 mV/A. The voltage across these two resistors is measured from J4_2-1 and J4_2-2/3, for the positive and negative terminals, respectively. TI recommends driving the CSD17527Q5A gate with at least 5 V to minimize $R_{DS(on)}$ of the CSD17527Q5A. The safe operating area of the CSD17527Q5A must always be observed when using this feature.

## 4.2 TPS542A50EVM-059 Top Circuit (Small Layout Area) Schematic

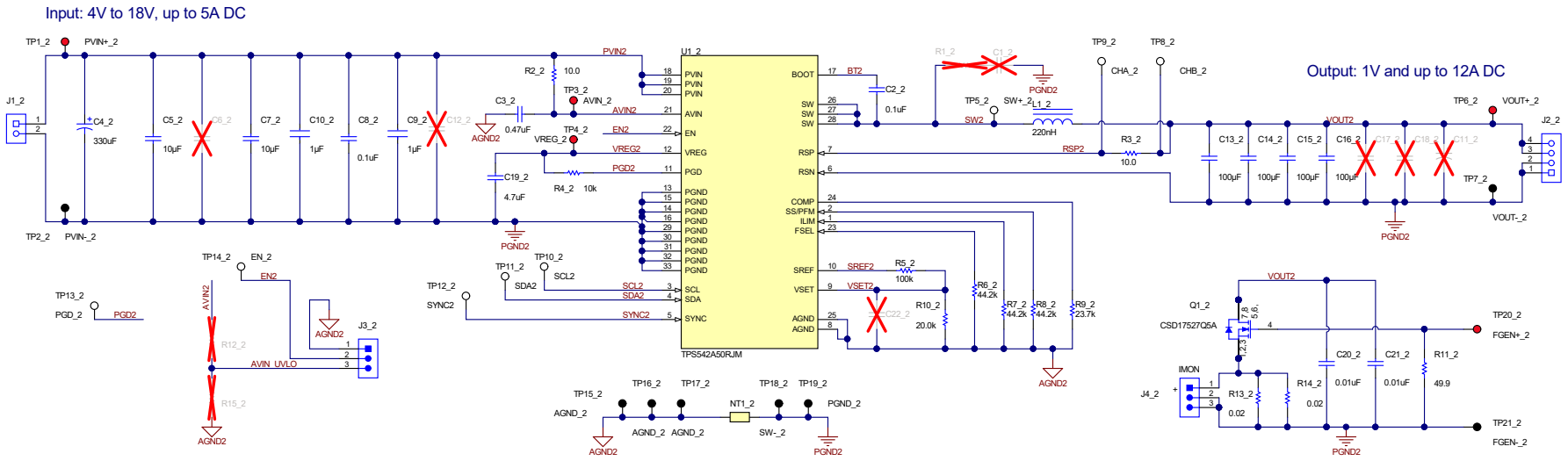


**Figure 4-1. TPS542A50EVM-059 Top Circuit Schematic**

## 4.3 Test Setup and Results

This section descibes how to properly connect, set up, and use the top circuit of the TPS542A50EVM-059. This section also includes test results typical for the evaluation module and covers efficiency, power loss, load regulatiom, line regulation, transient response, loop response, output voltage ripple, and start up. For a more complete set of data, please consult the TPS542A50 data sheet.

### 4.3.1 Input/Output Connections

The TPS542A50EVM-059 is provided with input/output connectors and test points as shown in Table 4-2. A power supply capable of supplying at least 5 A at the desired EVM input voltage must be connected to J1_2 through a pair of 20-AWG or greater wires. The load must be connected to J2_2 through a pair of 18-AWG or greater wires. The maximum load current capability of the top ciricuit is 12 A, as limited by R7_2.

Wire lengths must be minimized to reduce losses and parasitic inductance in the wires. PVIN+_2 (TP1_2) provides a tets point to monitor the VIN input voltages with PVIN-_2 (TP2_2) providing a convenient reference to PGND. VOUT+_2 (TP6_2) is used to monitor the output voltage with VOUT-_2 (TP7_2) providing a reference to PGND.

**Table 4-2. Bottom Circuit Connections and Test Points**

| Connection and Test Points | Description |
|---|---|
| J1_2 | VIN, PGND connection (see Table 1-1 for input voltage range) |
| J2_2 | VOUT, PGND connection: 5.5 V at 15 A maximum (default is 1 V out at 12 A) |
| J3_2 | Enable configuration |
| J4_2 | Output current sensing points when using function generator as load control signal |
| PVIN+_2 (TP1_2), PVIN-_2 (TP2_2) | VIN voltage sensing test points |
| VOUT+_2 (TP6_2), VOUT-_2 (TP7_2) | VOUT voltage sensing test points |
| AVIN_2 (TP3_2) | AVIN voltage sensing test points |
| VREG_2 (TP4_2) | VREG voltage sensing test point |
| SW+_2 (TP5_2), SW-_2 (TP18_2) | SW node sensing test points |
| CHA_2 (TP9_2), CHB_2 (TP8_2) | Loop measurement test points |
| SCL2 (TP10_2), SDA2 (TP11_2) | $I^2C$ connections |
| EN_2 (TP14_2) | EN pin test point |
| PGD_2 (TP13_2) | Open-drain PGD test point |
| SYNC2 (TP12_2) | For connecting and measuring external clock synchronization |
| AGND_2 (TP15_2, TP16_2, TP17_2) | AGND connection - multiple provided to reduce oscilloscope ground probe loop inductance |
| PGND_2 (TP18_2, TP19_2) | PGND connection |
| FGEN+_2 (TP20_2), FGEN-_2 (TP21_2) | Function generator connection points - referenced to PGND |

### 4.3.2 Start Up Procedure

1. Make sure the EN jumper (J3_2) is open to float the EN pin, enabling the TPS542A50.
2. If using an external load, connect the load to VOUT and PGND of J2_2 using copper wire capable of handling at least 15 A (18-AWG or greater). If using the built-in load with a function generator, connect the positive and negative connections of the function generator to FGEN+_2 (TP20_2) and FGEN-_2 (TP21_2), respectively.
3. Apply appropriate VIN voltage to the VIN and PGND terminals of J1_2.

### 4.3.3 Electrical Performance Specifications and Results

The typical electrical perfomance specifications of the TPS542A50EVM top circuit are shown in Table 4-3. Unless stated otherwise, the measurements were taken with the converter operating in FCCM and $T_{AMB}$ = 25°C.

**Table 4-3. Top Circuit Electrical Performance Specifications**

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $V_{IN}$ voltage range | | 5 | 12 | 14 | V |

**Table 4-3. Top Circuit Electrical Performance Specifications (continued)**

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $I_{IN}$ input current | $V_{IN}$ = 12 V, $I_O$ = 0 A | | 35 | | mA |
| | $V_{IN}$ = 12 V, $I_O$ = 12 A | | 1190 | | |
| Output voltage | | | 1 | | V |
| Output current range | | 0 | | 12 | A |
| Load regulation | $V_{IN}$ = 12 V, $I_O$ = 0 A to 12 A, | -0.2 | | +0.2 | % |
| Line regulation | $V_{IN}$ = 5 V to 14 V, $I_{OUT}$ = 0 A | -0.2 | | +0.2 | % |
| | $V_{IN}$ = 5 V to 14 V, $I_{OUT}$ = 12 A | -0.2 | | +0.2 | % |
| $\Delta V_{OUT}$, total overshoot/undershoot | $V_{IN}$ = 12 V, $I_O$ = 5-A to 10-A to 5-A load step @ 5A/µs | | 62.1 | | mV |
| Loop bandwidth | $V_{IN}$ = 12 V, $I_O$ = 10 A | | 105 | | kHz |
| Phase margin | | | 52 | | ° |
| Output voltage ripple | $V_{IN}$ = 12 V, $I_O$ = 0 A | | 11.6 | | mV |
| | $V_{IN}$ = 12 V, $I_O$ = 12 A | | 14.4 | | mV |
| Switching frequency | FCCM | | 1200 | | kHz |

### 4.3.4 Efficiency

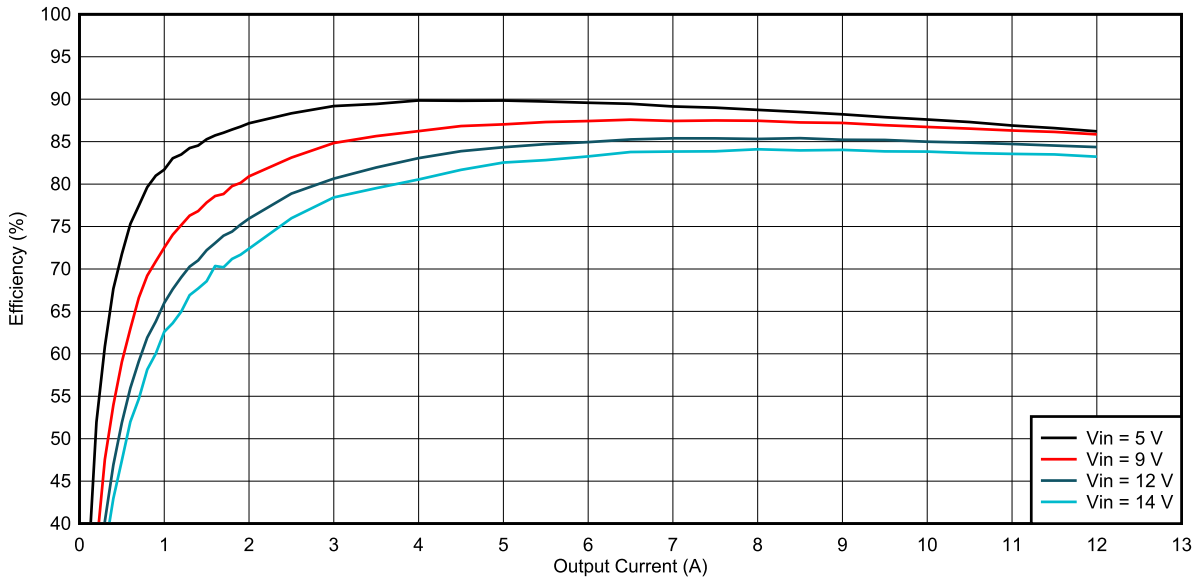


**Figure 4-2. Efficiency - FCCM, $f_{sw}$ = 1200 kHz**

### 4.3.5 Power Loss

The power loss of the circuit is shown in Figure 4-3. The losses of the top circuit are slightly higher due to the increased switching losses associated with a higher switching frequency.

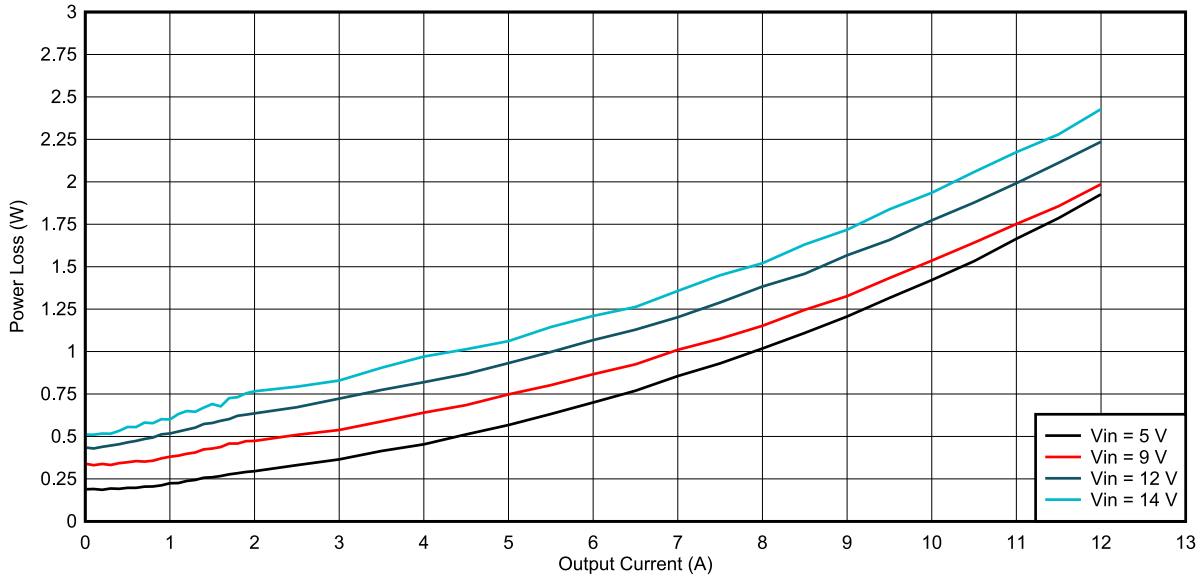


**Figure 4-3. Power Loss - FCCM, $f_{sw}$ = 1200 kHz**

### 4.3.6 Load Regulation

The load regulation for $V_{IN}$ = 5 V to 14 V is shown in Figure 4-4.

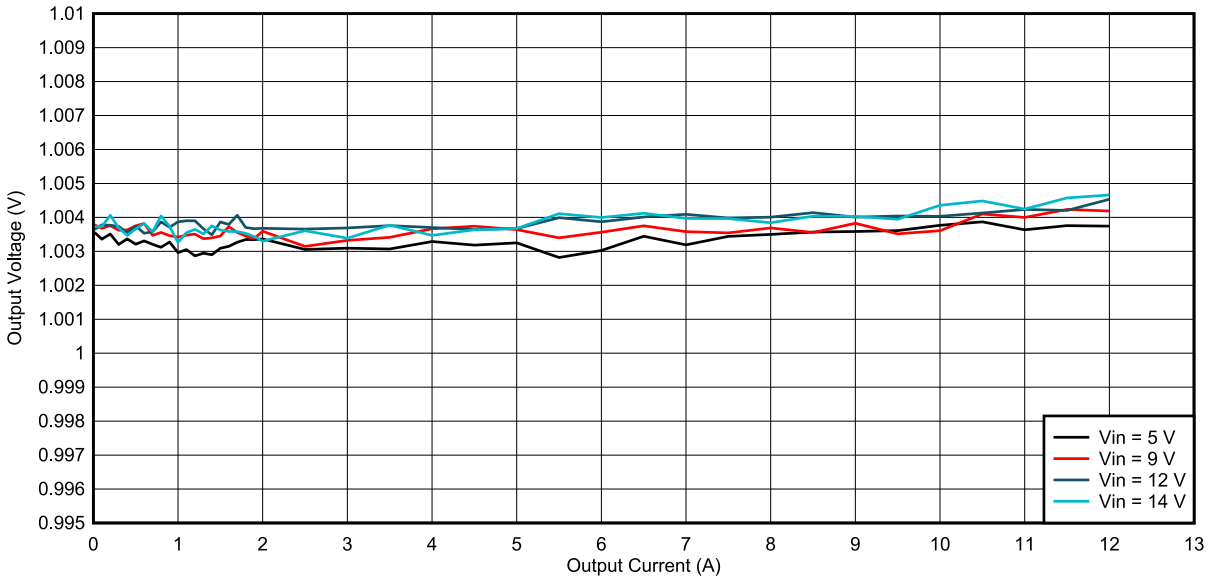


**Figure 4-4. Load regulation - FCCM, $f_{sw}$ = 1200 kHz**

### 4.3.7 Line Regulation

The line regulation for output currents of 0 A, 7 A, and 12 A is shown in Figure 4-5.

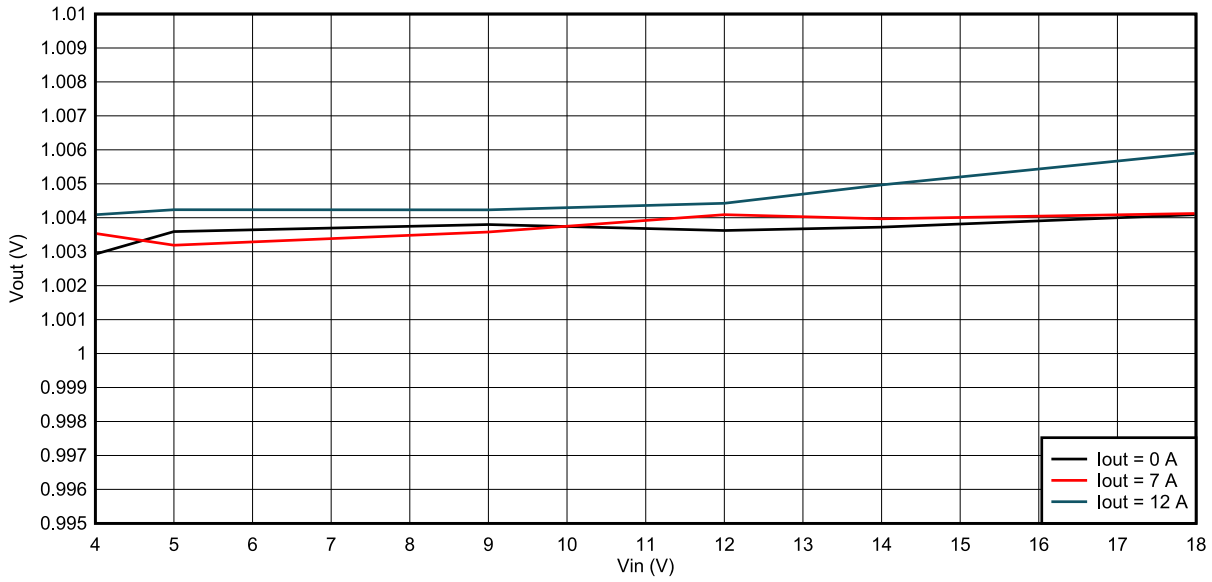


**Figure 4-5. Line regulation - FCCM, $f_{sw}$ = 1200 kHz**

### 4.3.8 Transient Response

Figure 4-6 shows the transient response of the converter when operating in FCCM. The total undershoot and overshoot in response to a 5-A load transient (5-A to 10-A to 5-A) with a slew rate of 5 A/µs is 62.1 mV.


**Figure 4-6. Transient response - 5-A to 10-A to 5-A load @5 A/µs, ΔVout = 62.1 mV, fsw = 1200 kHz, FCCM**

### 4.3.9 Loop Response

The loop response of the top circuit of the TPS542A50EVM-059 with a 10-A load is shown in Figure 4-7. The bandwidth of the loop is 105 kHz, and the phase margin is 52°.

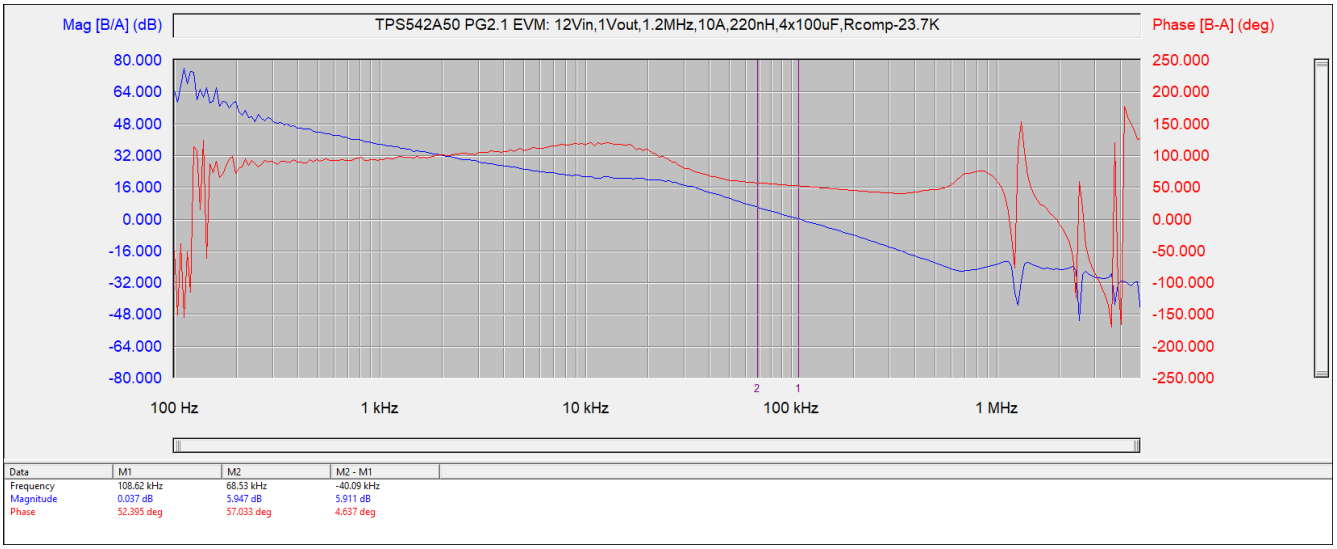


**Figure 4-7. Loop response - $I_{OUT}$ = 10 A, Loop Bandwidth = 105 kHz, Phase Margin = 52°**

### 4.3.10 Output Voltage Ripple

Figure 4-8 shows an output voltage ripple with a 0-A load, and Figure 4-9 shows the output voltage ripple with a 12-A load.

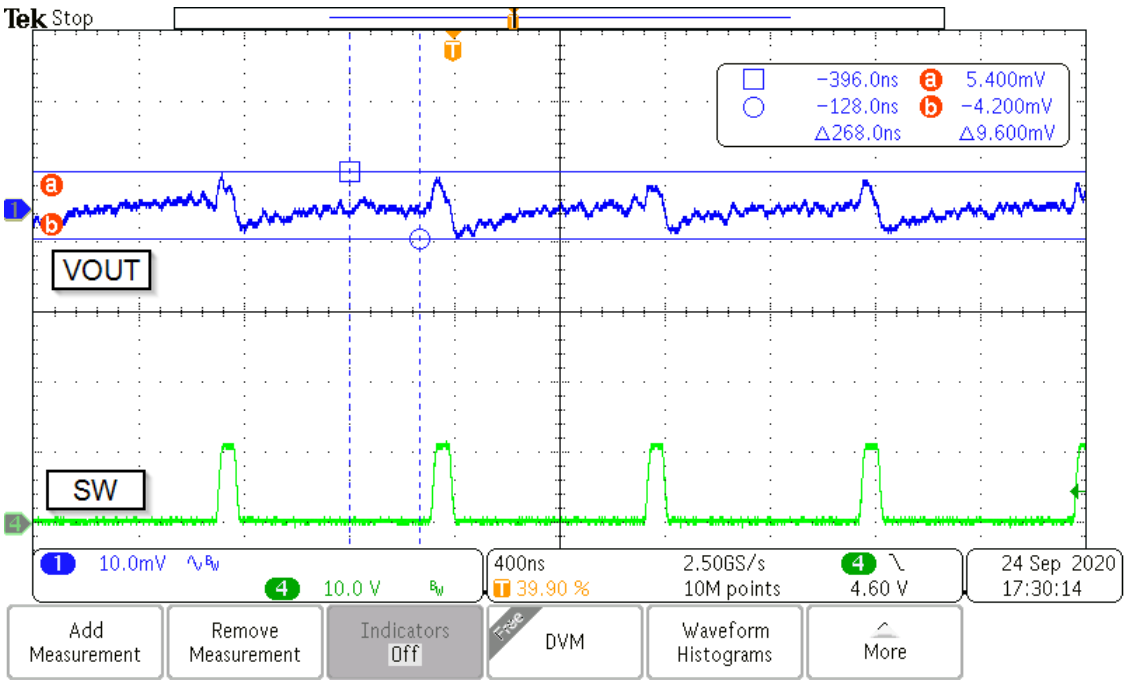


**Figure 4-8. Output Voltage Ripple - 0-A load, $\Delta V_{OUT}$ = 11.6 mV, $f_{sw}$ = 1200 kHz, FCCM**

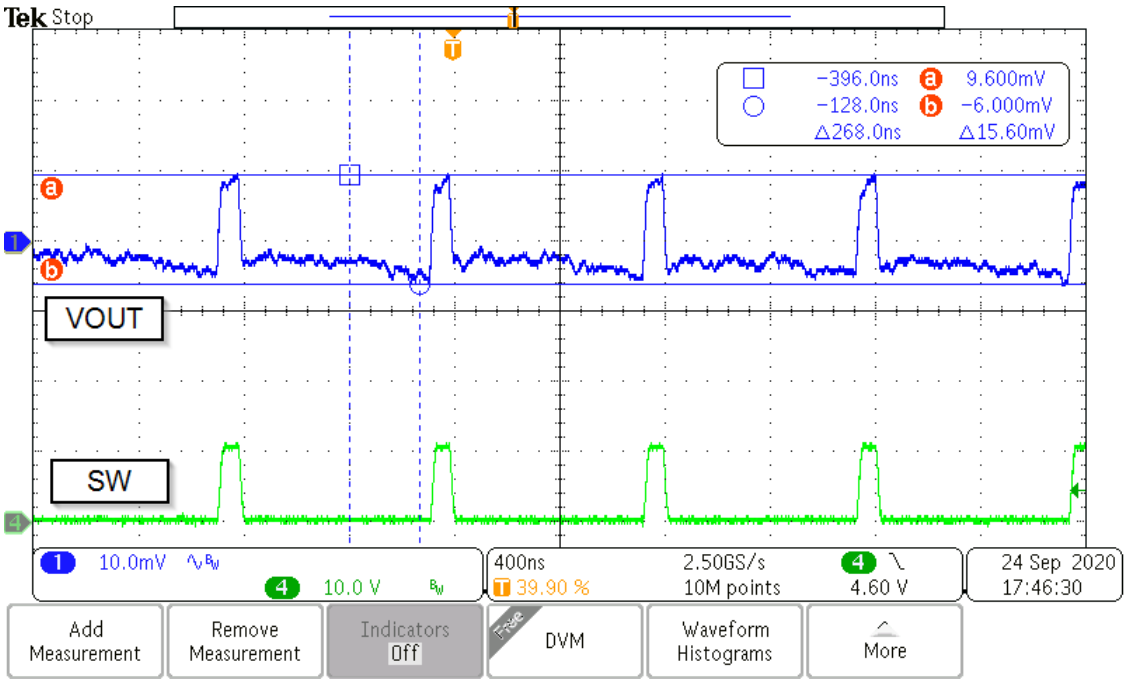


**Figure 4-9. Output Voltage Ripple - 12-A load, $\Delta V_{OUT}$ = 14.4 mV, $f_{sw}$ = 1200 kHz, FCCM**

### 4.3.11 Start Up

Figure 4-10 shows the $V_{OUT}$, EN, PGOOD, and SW start up waveforms with a 12-A load. The time between the rising edge of the EN signal and the rising edge of PGOOD is approximately 1.95 ms.

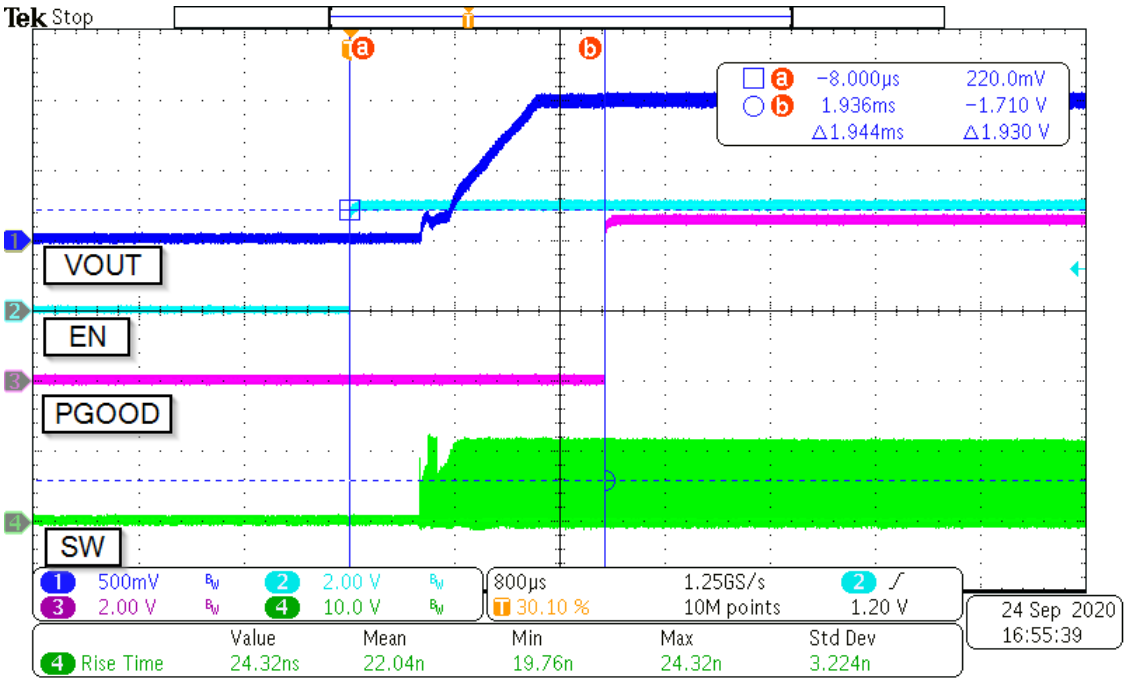


**Figure 4-10. Start up - 12-A load, $f_{sw}$ = 1200 kHz, FCCM**

# 5 TPS542A50EVM-059 PCB Layout

The PCB layout of the TPS542A50EVM-059 is shown in Figure 5-1 through Figure 5-8. The top, internal, and bottom layers are all 2 oz. copper.

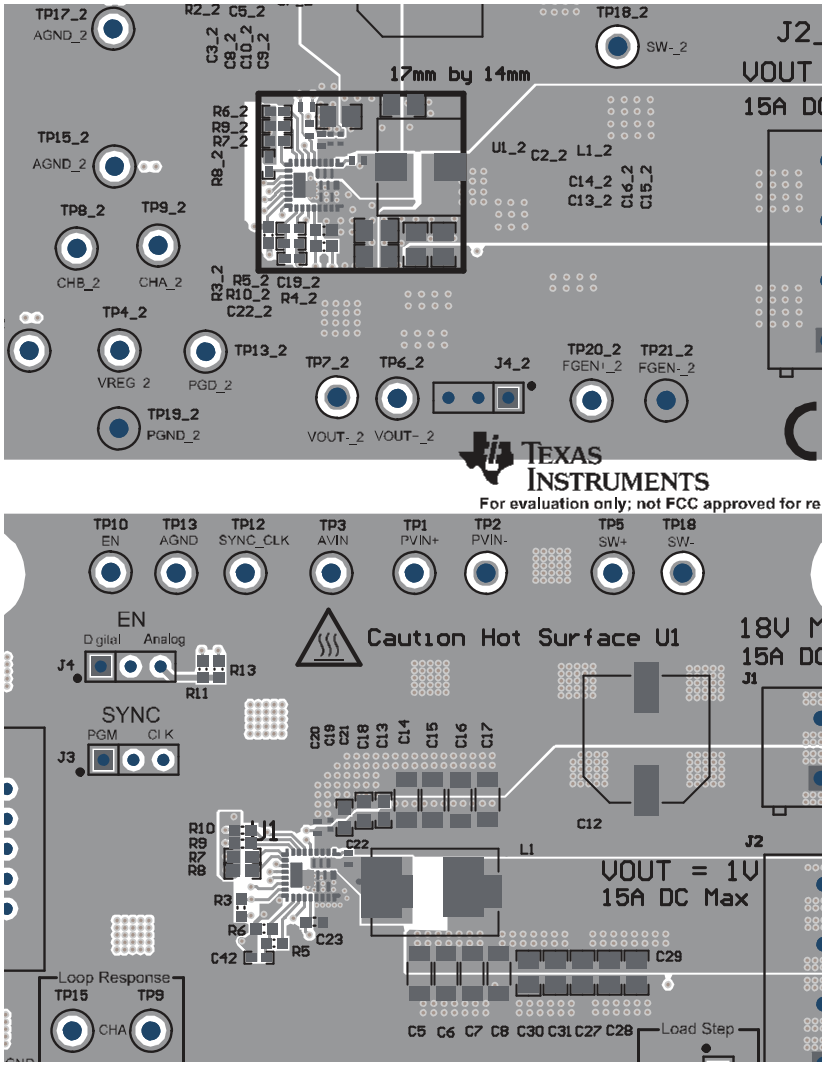


**Figure 5-1. Top-Side Composite View**

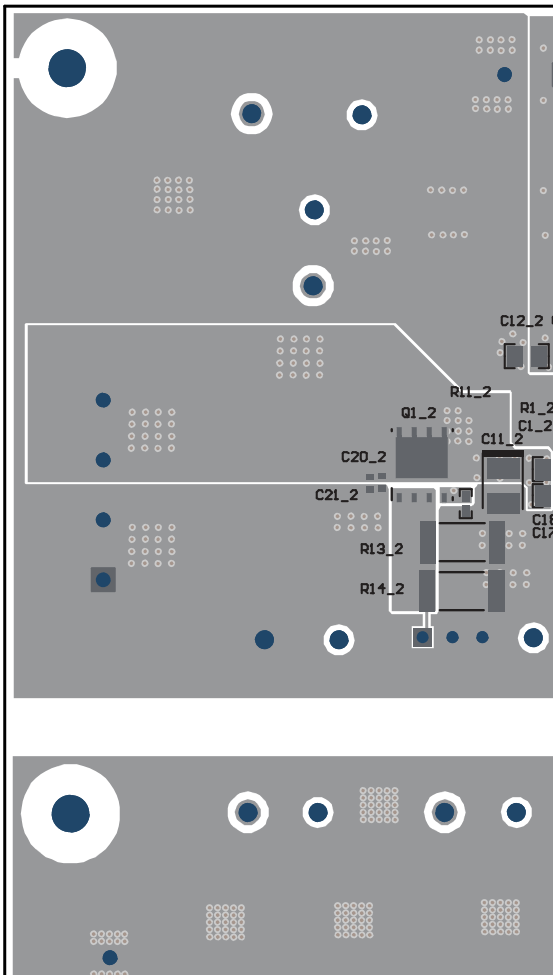


**Figure 5-2. Bottom-Side Composite View (Viewed From Bottom)**

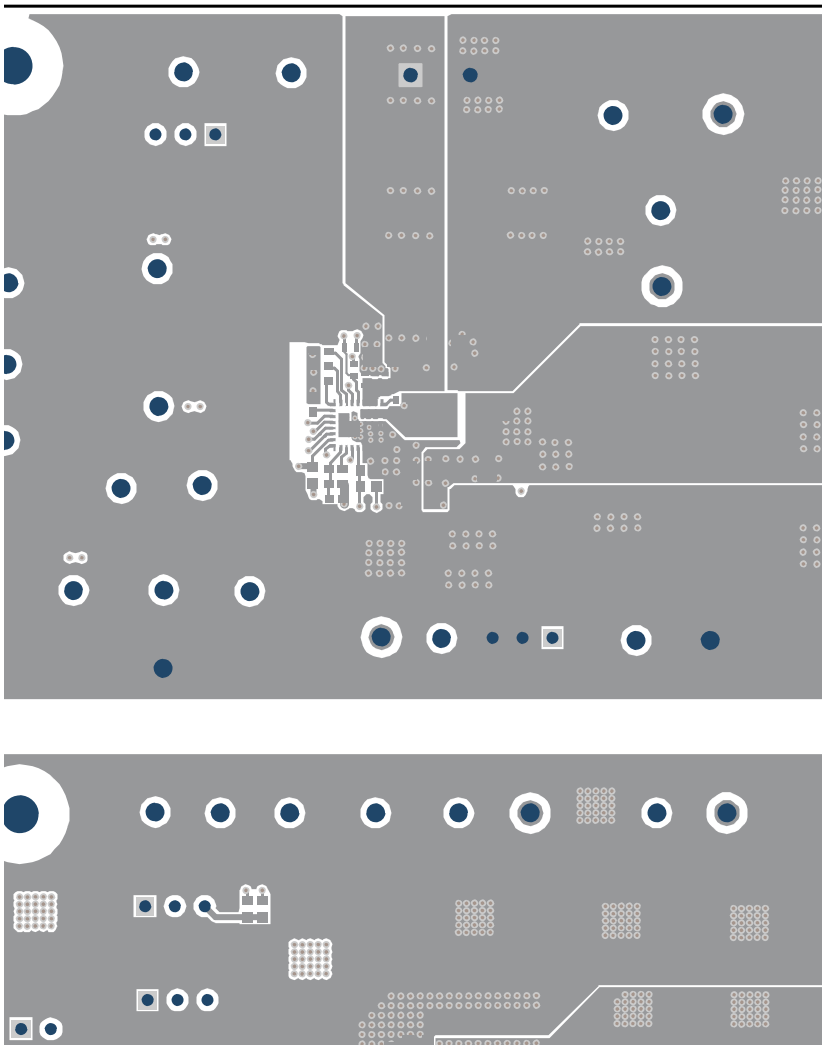

**Figure 5-3. Top-Side Layout (Top-Down View)**

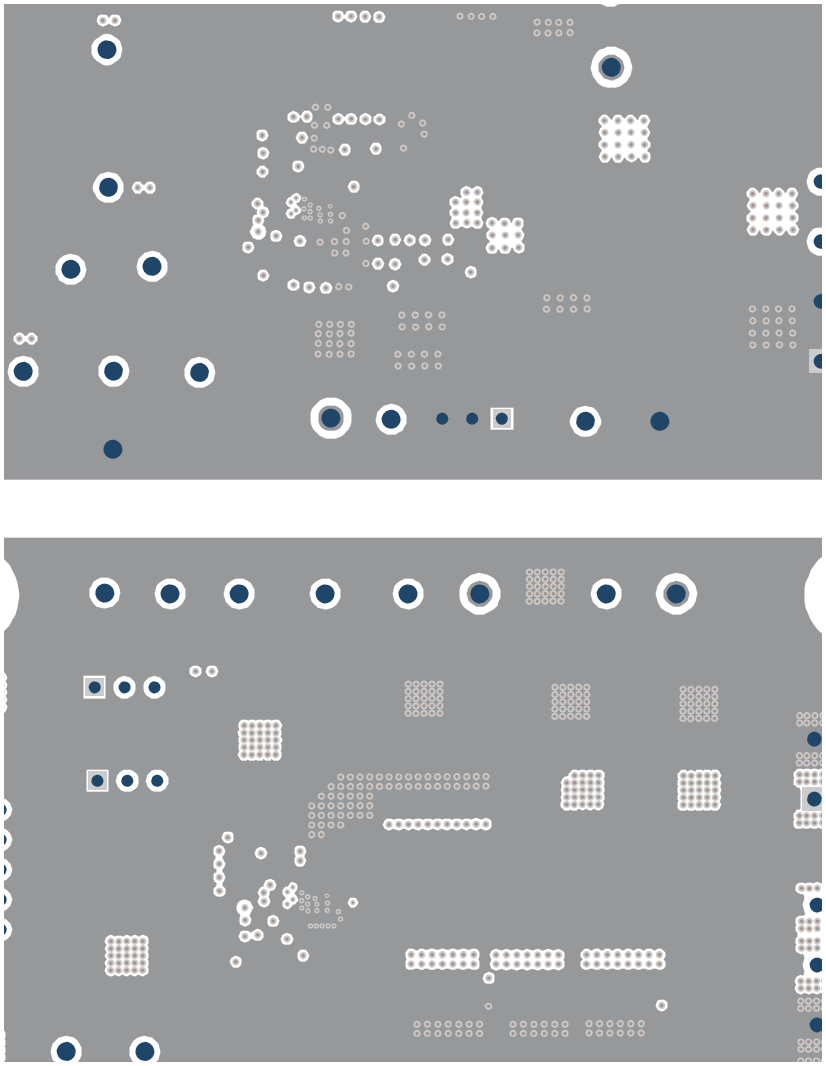

**Figure 5-4. Internal Layer-1 Layout (Top-Down View)**

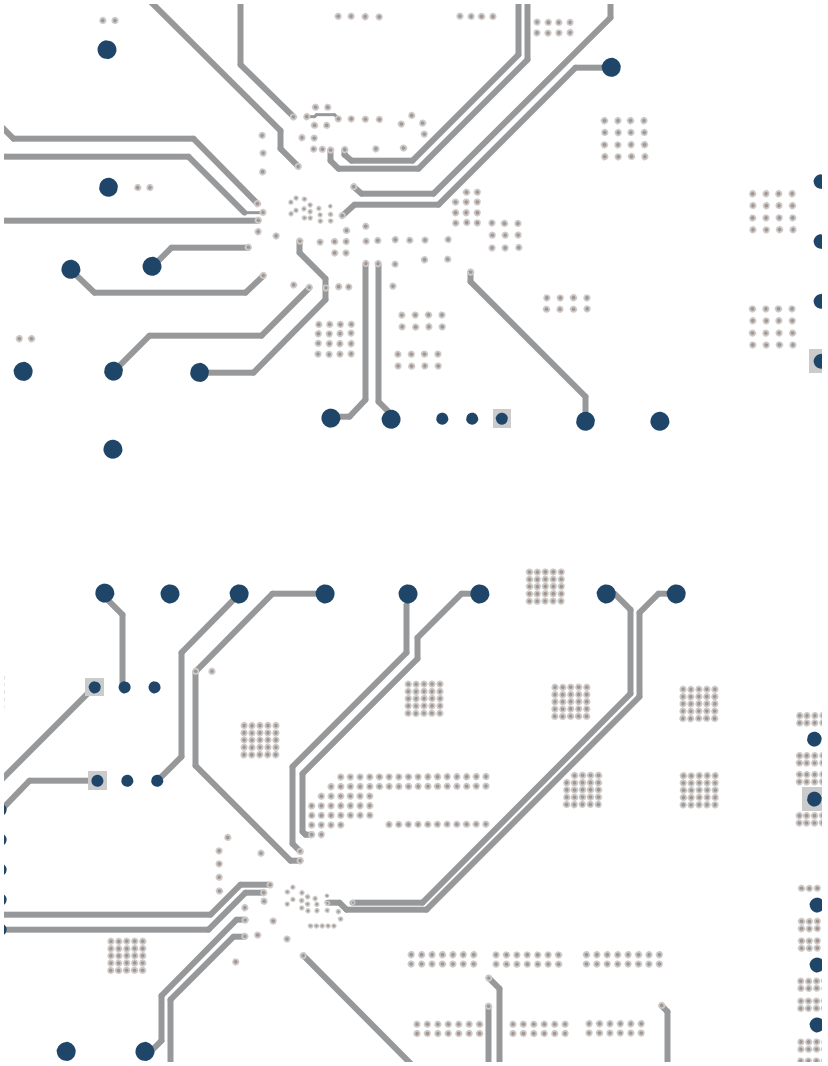

**Figure 5-5. Internal Layer-2 Layout (Top-Down View)**

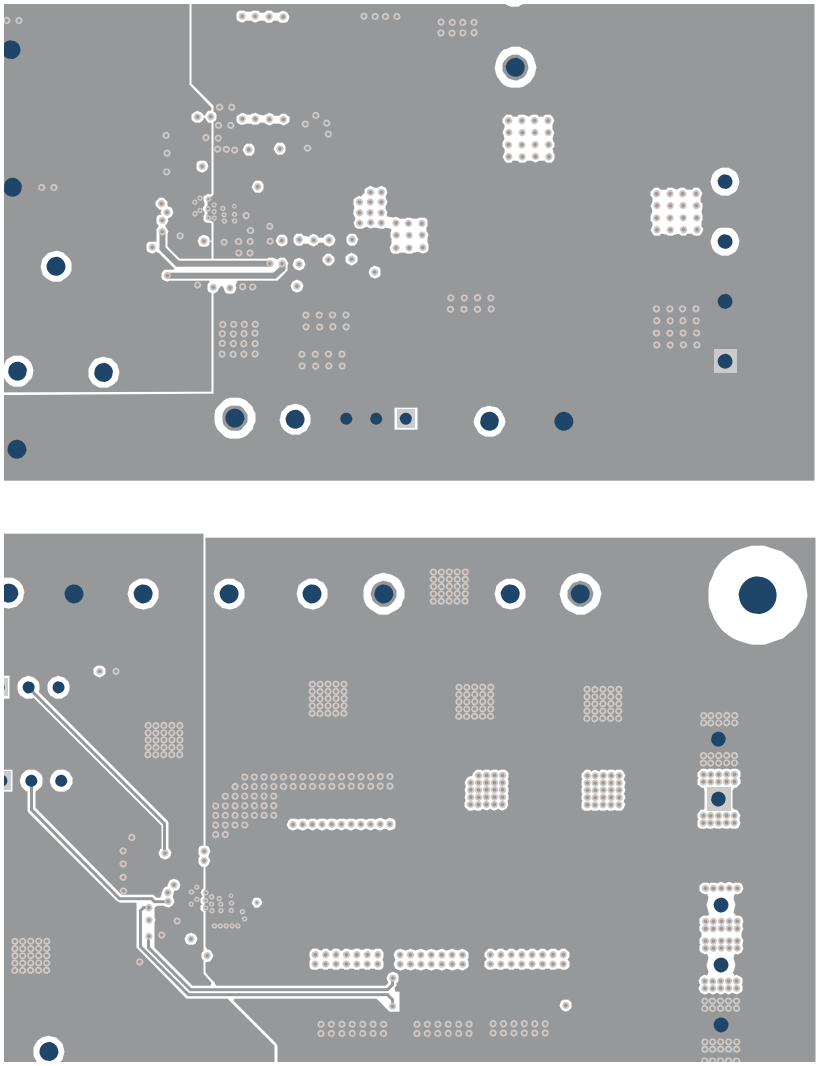

**Figure 5-6. Internal Layer-3 Layout (Top-Down View)**

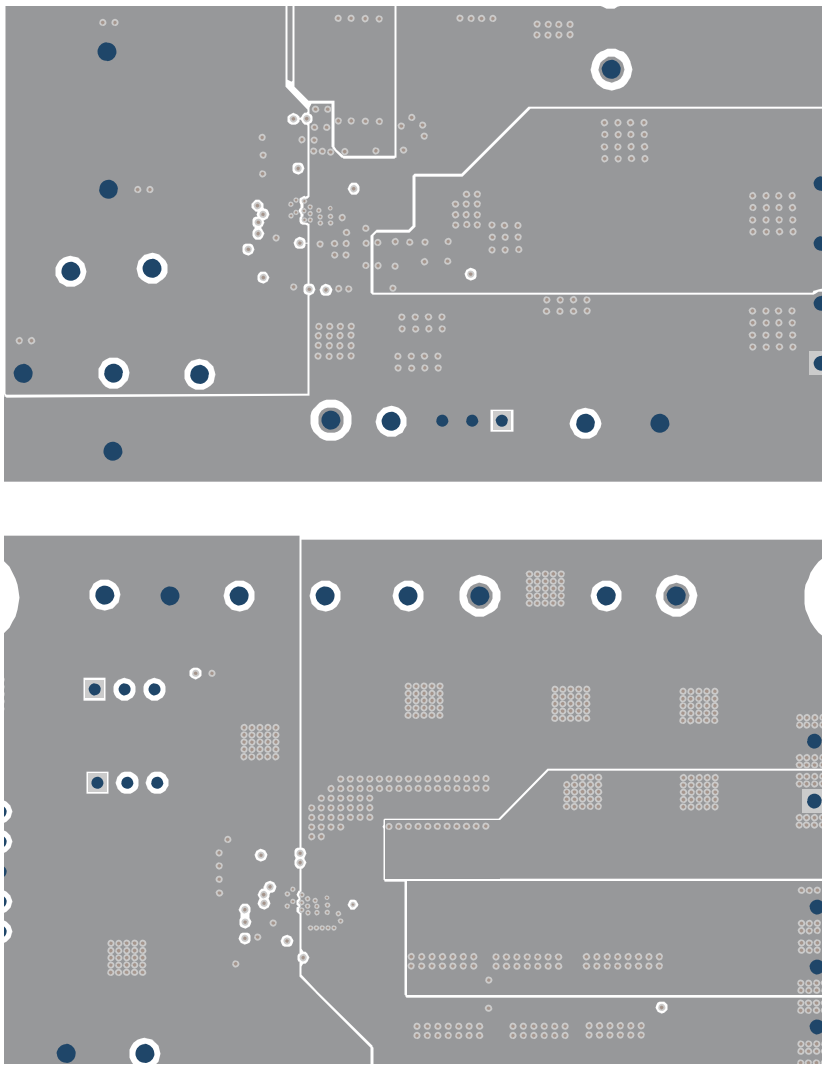

**Figure 5-7. Internal Layer-4 Layout (Top-Down View)**

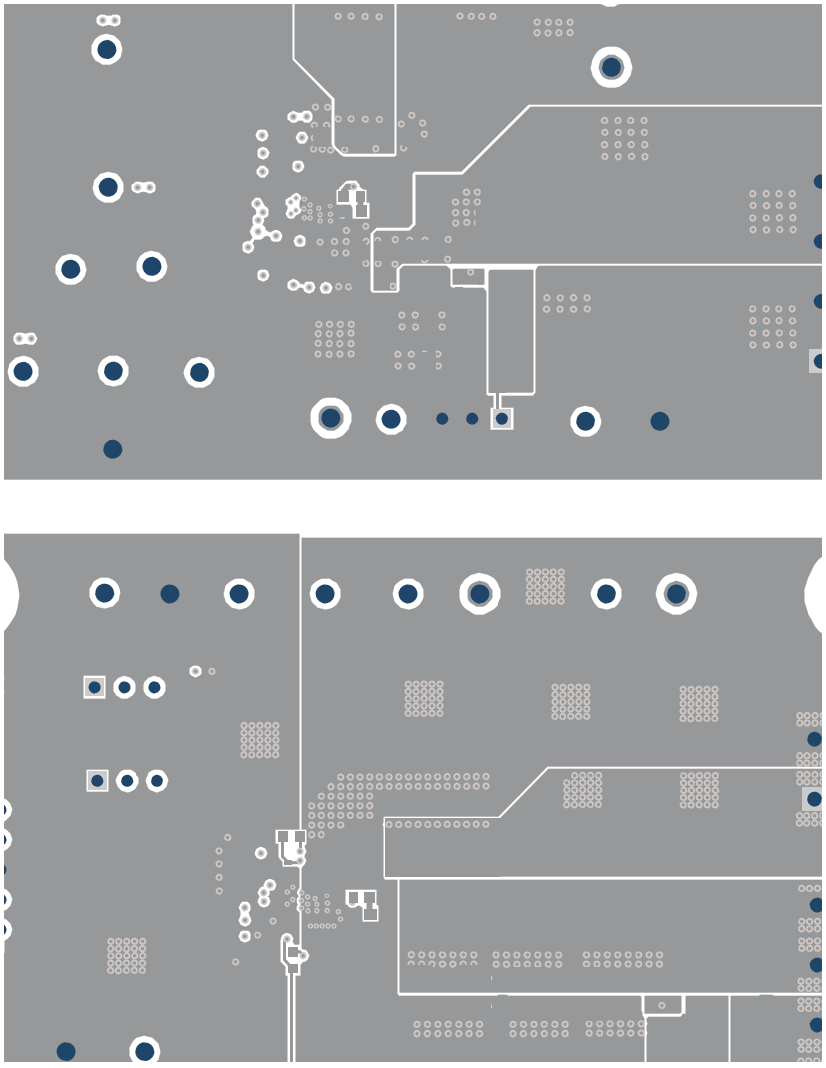

**Figure 5-8. Bottom-Side Layout (Top-Down View)**

# 6 List of Materials

The EVM components list, according to the schematic, is shown in Table 6-1.

**Table 6-1. TPS542A50EVM-059 List of Materials**

| Designator | Quantity | Value | Description | Package Reference | Part Number | Manufacturer |
|---|---|---|---|---|---|---|
| !PCB1 | 1 | | Printed Circuit Board | | BSR059 | Any |
| C1, C11_2 | 0 | DNP, 220uF | CAP, Tantalum Polymer, 220 uF, 6.3 V, +/- 20%, 0.035 ohm, 3.5x1.9x2.8mm SMD | 3.5x1.9x2.8mm | 6TPE220MAZB | Panasonic |
| C1_2, C33 | 0 | 220pF | CAP, CERM, 220 pF, 50 V, +/- 10%, X7R, 0603 | 0603 | C0603X221K5RACTU | Kemet |
| C2, C3, C4 | 3 | 220uF | CAP, Tantalum Polymer, 220 uF, 6.3 V, +/- 20%, 0.035 ohm, 3.5x1.9x2.8mm SMD | 3.5x1.9x2.8mm | 6TPE220MAZB | Panasonic |
| C2_2, C22 | 2 | 0.1uF | CAP, CERM, 0.1 uF, 25 V, +/- 10%, X7R, 0402 | 0402 | GRM155R71E104KE14D | MuRata |
| C3_2, C11 | 2 | 0.47uF | CAP, CERM, 0.47 uF, 25 V,+/- 10%, X5R, 0402 | 0402 | GRM155R61E474KE01D | MuRata |
| C4_2, C12 | 2 | 330uF | CAP, AL, 330 uF, 25 V, +/- 20%, 0.15 ohm, SMD | SMT Radial G | EEE-FC1E331P | Panasonic |
| C5, C6, C7, C8 | 4 | 100uF | CAP, CERM, 100 uF, 4 V, +/- 20%, X6T, 1206 | 1206 | GRM31CD80G107ME39L | MuRata |
| C5_2, C7_2 | 2 | 10uF | CAP, CERM, 10 µF, 25 V,+/- 10%, X6S, 0805 | 0805 | GRM21BC81E106KE51L | MuRata |
| C6_2, C12_2 | 0 | 10uF | CAP, CERM, 10 µF, 25 V,+/- 10%, X6S, 0805 | 0805 | GRM21BC81E106KE51L | MuRata |
| C8_2, C9, C20, C25, C26 | 5 | 0.1uF | CAP, CERM, 0.1 uF, 25 V, +/- 20%, X7R, 0402 | 0402 | TMK105B7104MV-FR | Taiyo Yuden |
| C9_2, C10_2, C19 | 3 | | CAP CER 1UF 25V X6S 0402 | 0402 | GRM155C81E105KE11D | Murata |
| C10 | 0 | 0.1uF | CAP, CERM, 0.1 uF, 25 V, +/- 20%, X7R, 0402 | 0402 | TMK105B7104MV-FR | Taiyo Yuden |
| C13, C18, C21 | 3 | 4.7uF | CAP, CERM, 4.7 uF, 25 V, +/- 10%, X6S, 0603 | 0603 | GRM188C81E475KE11D | MuRata |
| C13_2, C14_2, C15_2, C16_2 | 4 | 100uF | CAP, CERM, 100 µF, 4 V,+/- 20%, X6S, 0805 | 0805 | GRM21BC80G107ME15L | MuRata |
| C14, C15 | 2 | 22uF | CAP, CERM, 22 uF, 25 V, +/- 20%, X6S, 1206_190 | 1206_190 | GRM31CC81E226ME11L | MuRata |
| C16, C17 | 0 | 22uF | CAP, CERM, 22 uF, 25 V, +/- 20%, X6S, 1206_190 | 1206_190 | GRM31CC81E226ME11L | MuRata |
| C17_2, C18_2 | 0 | 100uF | CAP, CERM, 100 µF, 4 V,+/- 20%, X6S, 0805 | 0805 | GRM21BC80G107ME15L | MuRata |
| C19_2, C23 | 2 | 4.7uF | CAP, CERM, 4.7 uF, 16 V, +/- 10%, X5R, 0603 | 0603 | GRM188R61C475KAAJ | MuRata |
| C20_2, C21_2 | 2 | 0.01uF | CAP, CERM, 0.01 uF, 50 V, +/- 5%, X7R, 0402 | 0402 | C0402C103J5RACTU | Kemet |
| C22_2, C42 | 0 | 1000pF | CAP, CERM, 1000 pF, 50 V, +/- 10%, X7R, 0402 | 0402 | GRM155R71H102KA01D | MuRata |
| C27, C28, C29, C31 | 0 | 47uF | CAP, CERM, 47 uF, 6.3 V, +/- 20%, X5R, AEC-Q200 Grade 3, 0805 | 0805 | GRT21BR60J476ME13L | MuRata |
| C30 | 1 | 47uF | CAP, CERM, 47 uF, 6.3 V, +/- 20%, X5R, AEC-Q200 Grade 3, 0805 | 0805 | GRT21BR60J476ME13L | MuRata |
| C35, C36 | 2 | 0.01uF | CAP, CERM, 0.01 uF, 50 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603 | 0603 | GCM188R71H103KA37D | MuRata |
| C37 | 1 | 1uF | CAP, CERM, 1 uF, 16 V, +/- 10%, X7R, 0603 | 0603 | EMK107B7105KA-T | Taiyo Yuden |
| H1, H2, H3, H4, H9, H11 | 6 | | Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead | Screw | NY PMS 440 0025 PH | B&F Fastener Supply |
| H5, H6, H7, H8, H10, H12 | 6 | | Standoff, Hex, 0.5"L #4-40 Nylon | Standoff | 1902C | Keystone |
| J1, J1_2 | 2 | | Terminal Block, 5.08 mm, 2x1, Brass, TH | 2x1 5.08 mm Terminal Block | ED120/2DS | On-Shore Technology |
| J2, J2_2 | 2 | | Terminal Block, 5.08 mm, 4x1, Brass, TH | 4x1 5.08 mm Terminal Block | ED120/4DS | On-Shore Technology |
| J3, J3_2, J4, J4_2, J5 | 5 | | Header, 100mil, 3x1, Tin, TH | Header, 3 PIN, 100mil, Tin | PEC03SAAN | Sullins Connector Solutions |
| J6 | 1 | | Header(Shrouded), 2.54mm, 5x2, Gold, TH | Header, 2.54mm, 5x2, TH | AWHW-10G-0202-T | Assman WSW |
| L1 | 1 | 330nH | Inductor, Shielded Drum Core, Ferrite, 330 nH, 27 A, 0.00037 ohm, SMD | 10.1x6.8x7mm | 744308033 | Wurth Elektronik |
| L1_2 | 1 | 220nH | Inductor, Shielded Drum Core, Ferrite, 220 nH, 29 A, 0.00033 ohm, SMD | 7.4x7x7.2mm | 744307022 | Wurth Elektronik |

**Table 6-1. TPS542A50EVM-059 List of Materials (continued)**

| Designator | Quantity | Value | Description | Package Reference | Part Number | Manufacturer |
|---|---|---|---|---|---|---|
| LBL1 | 1 | | Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll | PCB Label 0.650 x 0.200 inch | THT-14-423-10 | Brady |
| Q1, Q1_2 | 2 | 30V | MOSFET, N-CH, 30 V, 65 A, DQJ0008A (VSONP-8) | DQJ0008A | CSD17527Q5A | Texas Instruments |
| R1, R3, R3_2 | 3 | 10.0 | RES, 10.0, 1%, 0.1 W, 0603 | 0603 | RC0603FR-0710RL | Yageo America |
| R1_2, R4 | 0 | 1.0 | RES, 1.0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603 | 0603 | CRCW06031R00JNEA | Vishay-Dale |
| R2, R4_2, R16, R17 | 4 | 10.0k | RES, 10.0 k, 1%, 0.1 W, 0603 | 0603 | RCG060310K0FKEA | Vishay Draloric |
| R2_2 | 1 | 10.0 | RES, 10.0, 1%, 0.063 W, 0402 | 0402 | RK73H1ETTP10R0F | KOA Speer |
| R5 | 1 | 100k | RES, 100 k, 1%, 0.1 W, 0603 | 0603 | RC0603FR-07100KL | Yageo America |
| R5_2 | 1 | 100k | RES, 100 k, 1%, 0.0625 W, 0402 | 0402 | RC0402FR-07100KL | Yageo America |
| R6 | 1 | 20.0k | RES, 20.0 k, 1%, 0.1 W, 0603 | 0603 | RC0603FR-0720KL | Yageo America |
| R6_2, R7_2, R8_2 | 2 | 44.2k | RES, 44.2 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402 | 0402 | CRCW040244K2FKED | Vishay-Dale |
| R7, R8 | 2 | 61.9k | RES, 61.9 k, 1%, 0.1 W, 0603 | 0603 | RC0603FR-0761K9L | Yageo |
| R9 | 1 | 16.2k | RES, 16.2 k, 1%, 0.1 W, 0603 | 0603 | RC0603FR-0716K2L | Yageo America |
| R9_2 | 1 | 23.7k | RES, 23.7 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402 | 0402 | CRCW040223K7FKED | Vishay-Dale |
| R10 | 1 | 33.2k | RES, 33.2 k, 1%, 0.1 W, 0603 | 0603 | RC0603FR-0733K2L | Yageo America |
| R10_2 | 1 | 20.0k | RES, 20.0 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402 | 0402 | CRCW040220K0FKED | Vishay-Dale |
| R11, R12_2, R13, R15_2 | 0 | 10.0k | RES, 10.0 k, 1%, 0.1 W, 0603 | 0603 | RCG060310K0FKEA | Vishay Draloric |
| R11_2, R12 | 2 | 49.9 | RES, 49.9, 1%, 0.063 W, AEC-Q200 Grade 0, 0402 | 0402 | CRCW040249R9FKED | Vishay-Dale |
| R13_2, R14, R14_2, R15 | 4 | 0.02 | RES, 0.02, 1%, 3 W, 2512 | 2512 | CRA2512-FZ-R020ELF | Bourns |
| SH-J1, SH-J2, SH-J3, SH-J4, SH-J5 | 5 | | Shunt, 100mil, Gold plated, Black | Shunt 2 pos. 100 mil | 881545-2 | TE Connectivity |
| TP1, TP1_2, TP3, TP3_2, TP4, TP4_2, TP6, TP6_2, TP19, TP20_2 | 10 | | Test Point, Multipurpose, Red, TH | Red Multipurpose Testpoint | 5010 | Keystone |
| TP2, TP2_2, TP7, TP7_2, TP13, TP14, TP15, TP15_2, TP16_2, TP17, TP17_2, TP18, TP18_2, TP19_2, TP20, TP21_2 | 16 | | Test Point, Multipurpose, Black, TH | Black Multipurpose Testpoint | 5011 | Keystone |
| TP5, TP5_2, TP8, TP8_2, TP9, TP9_2, TP10, TP10_2, TP11, TP11_2, TP12, TP12_2, TP13_2, TP14_2 | 14 | | Test Point, Multipurpose, White, TH | White Multipurpose Testpoint | 5012 | Keystone |
| U1, U1_2 | 2 | | 4-V to 18-V Input, 15-A, Synchronous Buck Converter with Differential Remote Sense and I2C, RJM0033A (VQFN-HR-33) | RJM0033A | TPS542A50RJM | Texas Instruments |

# 7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision * (September 2020) to Revision A (October 2021) | Page |
|---|---|
| • Updated the numbering format for tables, figures, and cross-references throughout the document. | 3 |
| • Updated the user's guide title. | 3 |

# IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265