UCC21220EVM-009

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1 Introduction

The UCC21220EVM-009 device is designed for evaluation of the UCC21220 family of devices, with a 4-A source and 6-A sink peak current for driving Si MOSFETs, IGBTs, and GaN FETs. Developed for high voltage applications where isolation and reliability are required, the UCC21220 device delivers reinforced isolation of 3-kV_{RMS} and a surge immunity tested up to 7.8-kV, with a common mode transient immunity (CMTI) greater than 100 V/ns. The device has an impressive propagation delay of 25 ns and the tightest channel-to-channel delay matching in the industry of less than 5 ns, which enables high-switching frequency, high-power density, and efficiency.

The flexible, universal capability of the UCC21220 device, with up to 5-V VCCI and 18-V VDDA and VDDB, allows it to be used as a low-side, high-side, high-side/low-side, or half-bridge driver with dual PWM input or single PWM input. With its integrated components, advanced protection features (UVLO, enable and disable), and optimized switching performances, the UCC21220 device enables designers to build smaller, more robust designs for enterprise, telecom, automotive, and industrial applications, allowing for faster time to market.

The UCC21220EVM-009 can also be used for evaluation of pin-to-pin compatible drivers with dead time control such as the UCC21222, with footprints for a surface mount potentiometer and noise reduction capacitor.

2 Description

The UCC21220EVM-009 evaluation board has independent connection points for VCCI, VDDA, and VDDB supplies, including separate ground points. Three-position headers with jumpers for all the key input signals, such as PWM inputs (INA, INB, or PWM) and the disable function (DIS), let designers easily evaluate different protection functions. A variety of testing points support most of the key-feature probing of the UCC21220 device. Moreover, the PCB layout is not only optimized with minimized loop area in each gate driver loop and power supply loop with bypassing capacitors, but it also supports high voltage testing between the primary side and secondary side, with a 40-mil PCB board cutout. Importantly, the creepage distance between two output channels is maximized with a TO252-2 (DPAK) bootstrap diode, which facilitates high-voltage, half-bridge testing for a wide variety of power converter topologies. For detailed device information, see the UCC21220 4-A/6-A, Dual Channel Isolated Gate Driver data sheet and Isolated Gate Driver Solutions, from TI.

2.1 Features

- Evaluation module for UCC21220 and other pin-to-pin compatible drivers in SOIC-16 (D) package
- 3-V to 5-V VCCI power supply range, with up to 18-V VDDA/VDDB power supply range
- 4-A source and 6-A sink current capability
- 3-kV_{RMS} isolation for 1 minute per UL 1577
- TTL/CMOS compatible inputs
- 3-position header for INA, INB, and DIS pins
- Optional footprints for dead time potentiometer, capacitor, and 3-position header
- PCB layout optimized for power supply bypassing capacitors, gate driver loop
- PCB board cutout facilitates high-voltage isolation test between primary side and secondary side
- Maximized creepage distance between two output channels
- Support half-bridge test with MOSFETs, IGBTs, and SiC MOSFETs, with connection to external power stage
- Testing points allow probing all the key pins of the UCC21220 device and other SOIC-16 isolated driver parts

2.2 I/O Description

Table 1 lists the test points and jumpers.

Table 1. Test Points and Jumpers

Pins	Description
TP1	Primary supply positive input
TP2	Primary supply negative input
TP3	VCC measurement point (main capacitor)
TP4	VCC measurement point (IC pins)
TP5	INA negative input (input side GND)
TP6	INB negative input (input side GND)
TP7	INA positive input
TP8	INB positive input
TP9	INA measurement point (IC pins)
TP10	INB measurement point (IC pins)
TP11	Input side GND (IC pins)
TP12	Disable pin input/measurement point
TP13	Dead time programming pin input/measurement point(1)
TP14	VDDA measurement point (IC pins)
TP15	VSSA measurement point (IC pins)
TP16	A-channel supply positive input
TP17	A-channel output, measured after gate drive resistor
TP18	A-channel supply negative input
TP19	VDDB measurement point (IC pins)
TP20	VSSB measurement point (IC pins)
TP21	B-channel supply positive input
TP22	B-channel output, measured after gate drive resistor
TP23	B-channel supply negative input
J1-1	Connected to VCCI
J1-2	Connected to INA
J1-3	Connected to GND
J2-1	Connected to VCCI
J2-2	Connected to INB
J2-3	Connected to GND
J3-3	Connected to VCCI
J3-2	Connected to disable pin
J3-3	Connected to GND
J4-1	Connected to VCCI
J4-2	Dead time programming pin(1)
J4-3	Connected to optional dead time programming potentiometer(1)

(1) The UCC21220 device does not have dead time control. Pin 6 of the UCC21220 is not connected internally. J4 header, and footprints for optional trimmer potentiometer and dead time capacitor, are included for other pin-to-pin compatible isolated drivers with dead time control.

2.3 Jumpers (Shunt) Setting

Table 2 lists the jumper settings.

Table 2. Jumpers Setting

Header	Jumper Setting Options		Factory Setting
J1	Option A	Jumper not installed, INA provided by external signal and this pin is low by default if left open	Option A
	Option B	Jumper on J1-2 and J1-3 sets INA low	
	Option C	Jumper on J1-2 and J1-1 sets INA high	
J2	Option A	Jumper not installed, INB provided by external signal, and this pin is low by default if left open	Option A
	Option B	Jumper on J2-2 and J2-3 sets INB low	
	Option C	Jumper on J2-2 and J2-1 sets INB high	
J3	Option A	Jumper not installed	Option C
	Option B	Jumper on J3-2 and J3-3 sets DIS low (part is enabled)	
	Option C	Jumper on J3-2 and J3-1 sets DIS high (part is disabled)	
J4 (1)	Option A	Jumper not installed	Option B
	Option B	Jumper on J4-2 and J4-1 sets pin 6 high.	
	Option C	Jumper on J4-2 and J4-3 connects pin 6 to the optional trimmer potentiometer.	

(1) The UCC21220 device does not have dead time control. Pin 6 of the UCC21220 device is not connected internally. J4 header, and footprints for optional trimmer potentiometer and dead time capacitor, are included for other pin-to-pin compatible isolated drivers with dead time control.

3 Electrical Specifications

Table 3 lists the UCC21220EVM-009 electrical specifications.

Table 3. UCC21220EVM-009 Electrical Specifications

Description		MIN	TYP	MAX	UNIT
V_{CCI}	Primary-side power supply	3		5.5	V
V_{DDA}, V_{DDB}	Driver output power supply for UCC21220	9.2		18	V
F_{SW}	Switching frequency	0		10	MHz
T_J	Operating junction temperature range	–40		130	°C

4 Test Summary

In this section, the default factory configuration for the jumper settings must be changed to enable the part as per Figure 1. Different jumper settings, PWM signal input options, and voltage source settings are described in Section 2 and Section 3.

4.1 Equipment

4.1.1 Power Supplies

Three DC power supplies with voltage/current above 18 V and 1 A, respectively are required, for example: Agilent E3634A.

4.1.2 Function Generators

One 2-channel function generator over 20 MHz is required, for example: Tektronics AFG3252.

4.2 Equipment Setup

4.2.1 DC Power Supply Settings

- DC power supply 1
  - Voltage setting: 5 V
  - Current limit: 0.05 A
- DC power supply 2
  - Voltage setting: 12 V
  - Current limit: 0.1 A
- DC power supply 3
  - Voltage setting: 12 V
  - Current limit: 0.1 A

4.2.2 Digital Multi-Meter (DMM) Settings

- Digital multi-meter 1:
  - DC current measurement, auto-range.
- Digital multi-meter 2:
  - DC current measurement, auto-range.

4.2.3 Two-Channel Function Generator Settings

Table 4 lists the 2-channel function generator settings.

Table 4. Two-Channel Function Generator Settings

	Mode	Frequency	Duty	Delay	High	Low	Output Impedance
Channel 1	Pulse	10 MHz	50%	0 ns	3.3 V	0 V	High Z
Channel 2				500 ns			

4.2.4 Oscilloscope Setting

Table 5 lists the oscilloscope setting.

Table 5. Oscilloscope Settings

	Bandwidth	Coupling	Termination	Scale Settings	Inverting
Channel 1	500 MHz or above	DC	1 MΩ or automatic	10× or automatic	Off
Channel 2					

4.2.5 Jumper (Shunt) Settings

The jumper on header J3 must be installed by the user between pins J3-2 and J3-3 to enable the part for testing. The jumper on header J4 may be placed in any position or removed (see Figure 1).

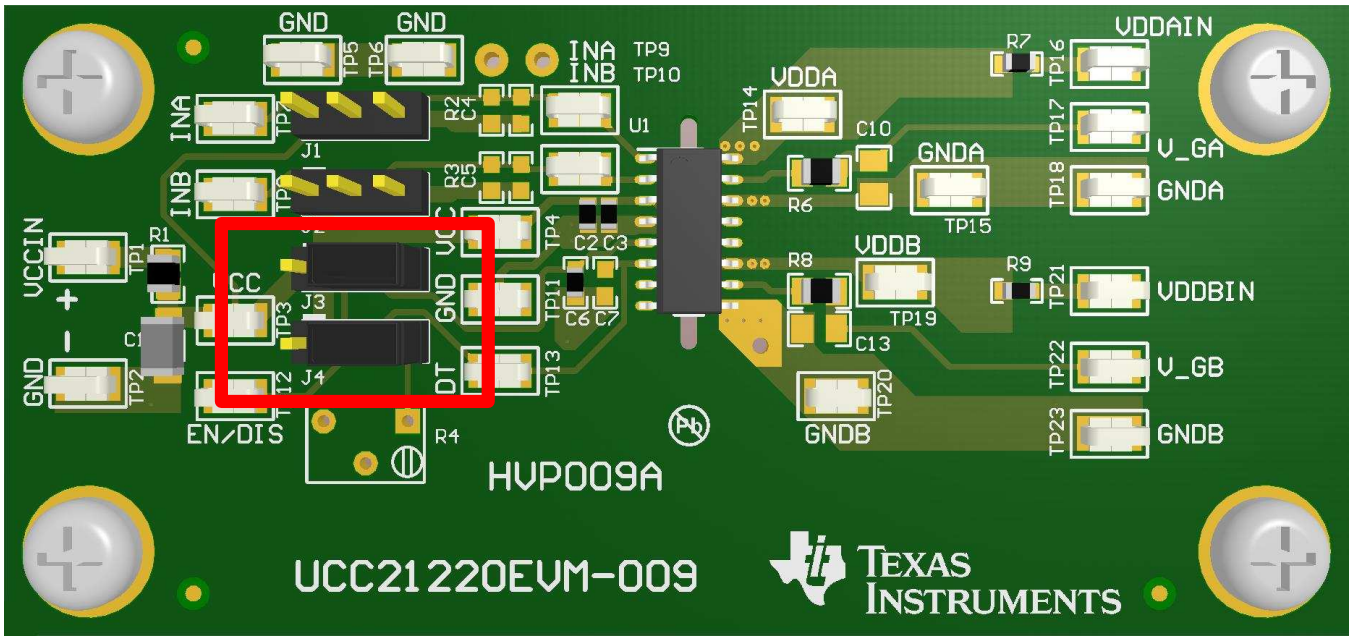

Figure 1. Jumpers Installation Position

4.2.6 Bench Setup Diagram

The current bench setup diagram includes the function generator and oscilloscope connections.

Follow this connection procedure, Figure 2 can be used as a reference.

1. Ensure the output of the function generator and voltage sources are disabled before connection.
2. Connect the function generator channel 1 to TP7 (INA) and TP5 (GND), see Figure 2.
3. Connect the function generator channel 2 to TP8 (INB) and TP6 (GND), see Figure 2.
4. Power supply 1: Connect the positive lead to TP1 (VCCIN). Connect the negative lead to TP2 (GND).
5. Power supply 2: Connect the positive lead to the current meter input of DMM1, and connect the current meter output of DMM1 to TP16 (VDDAIN). Connect the negative lead directly to TP18 (GNDA).
6. Power supply 3: Connect the positive lead to the current meter input of DMM2, and connect the current meter output of DMM2 to TP21 (VDDBIN). Connect the negative lead directly to TP23 (GNDB).
7. Connect the oscilloscope channel 1 probe to TP17 (V_GA) and TP15 (GNDA). The probe loop area should be minimized.
8. Connect the oscilloscope channel 2 probe to TP22 (V_GB) and TP20 (GNDB). The probe loop area should be minimized.

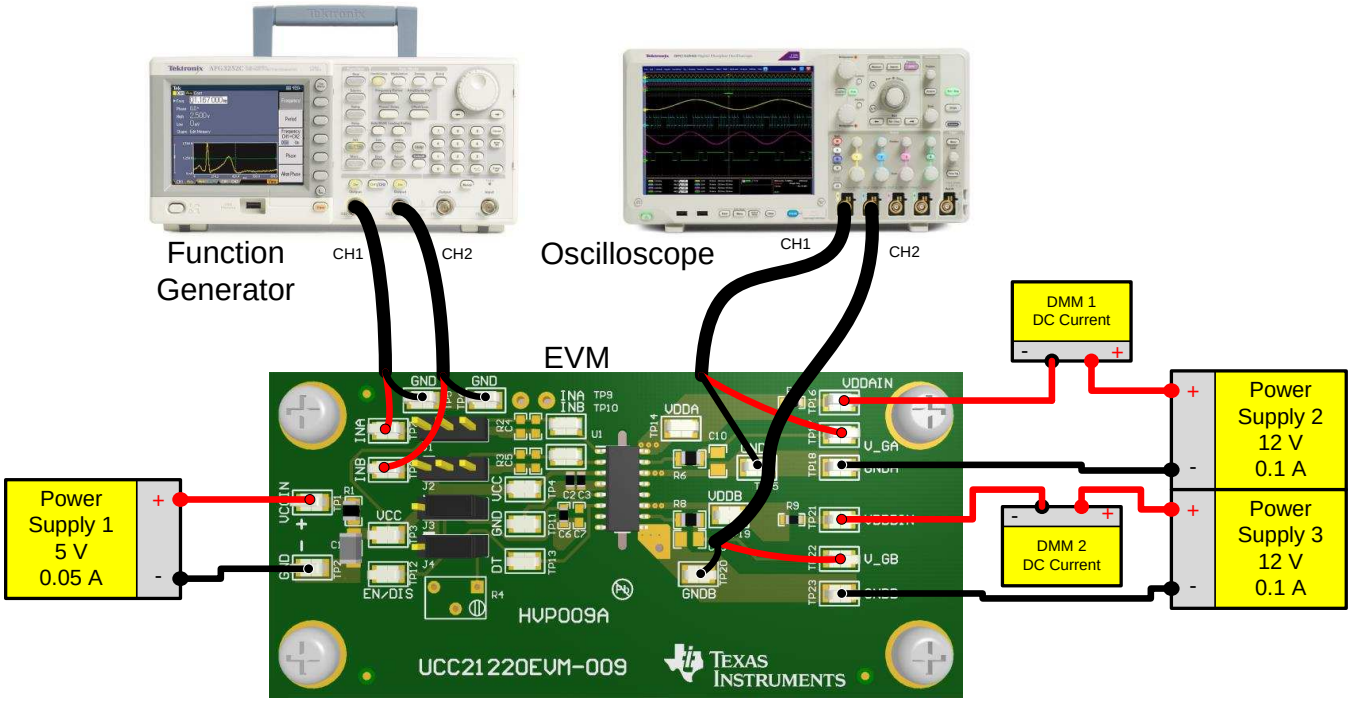

Figure 2. Bench Setup Diagram and Configuration

5 Power Up and Power Down Procedure

5.1 Power Up

1. Before preceding with the power up test procedure, ensure that the steps in Section 4.2.6 are complete. Figure 3 can be used as a reference.
2. Enable power supply 1.
3. Enable power supplies 2 and 3. The quiescent current on DMM1 and DMM2 should be approximately 1 mA to 3 mA if everything is set correctly.
4. Enable the function generator outputs.
5. Verify that the following occurs:
    1. Stable pulse output appears on channel 1 and channel 2 in the oscilloscope, see Figure 3.
    2. Oscilloscope frequency measurement matches programmed function generator frequency.
    3. DMM1 and DMM2 currents should read 14 ± 2 mA under no load conditions. For more information about the operating current, see the UCC21220 4-A/6-A, Dual Channel Isolated Gate Driver data sheet.

Figure 3. Example Input and Output Waveforms (Inputs: CH1 and CH2, Outputs: CH3 and CH4)

Figure 4 shows a zoomed-in view of the example input and output waveforms.

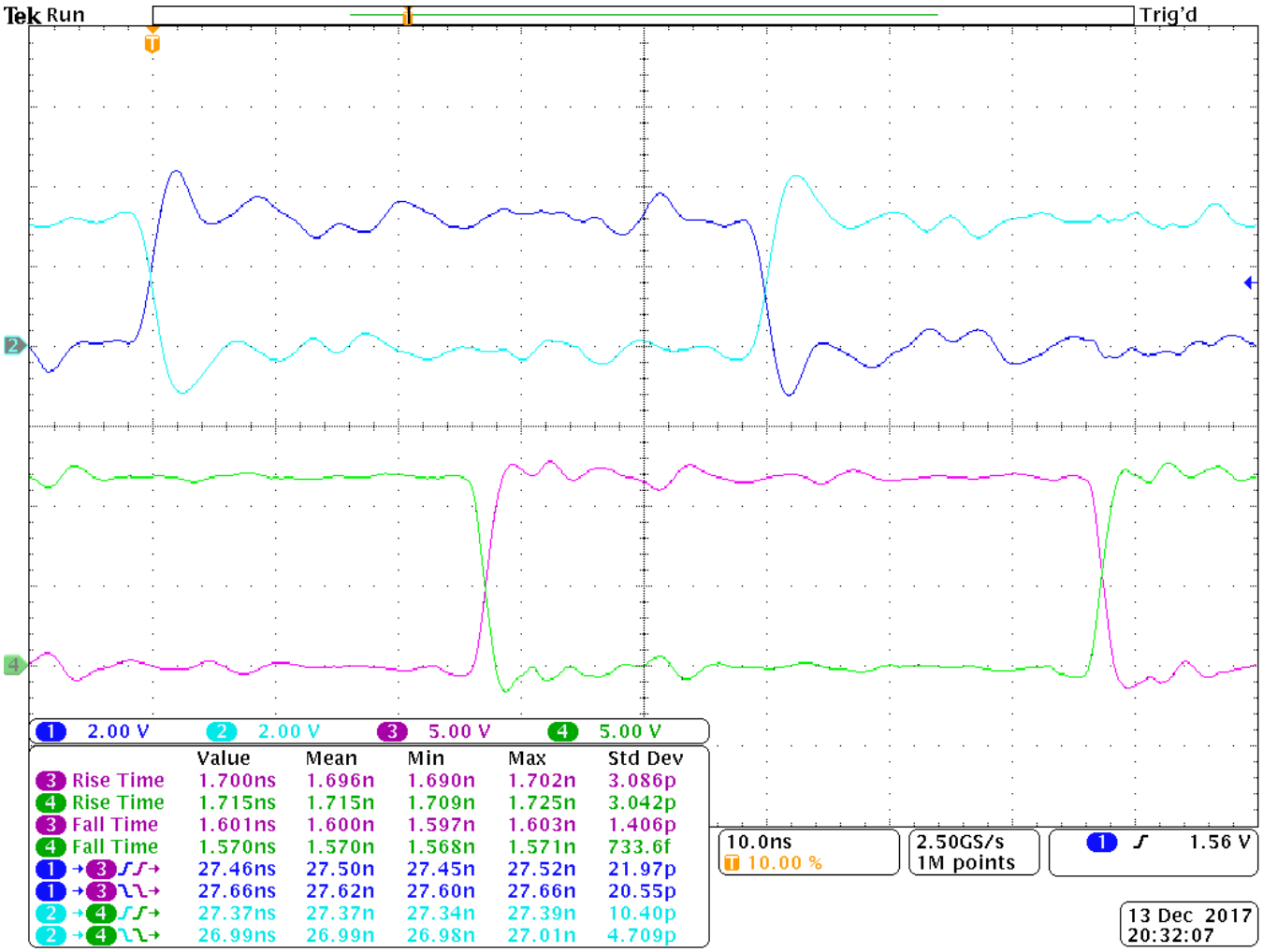

Figure 4. Example Input and Output Waveforms, Zoom In (Inputs: CH1 and CH2, Outputs: CH3 and CH4)

5.2 Power Down

The following lists the procedure to power down the EVM.

1. Disable the function generator.
2. Disable power supplies 2 and 3.
3. Disable power supply 1.
4. Disconnect the cables and probes.

6 Schematic

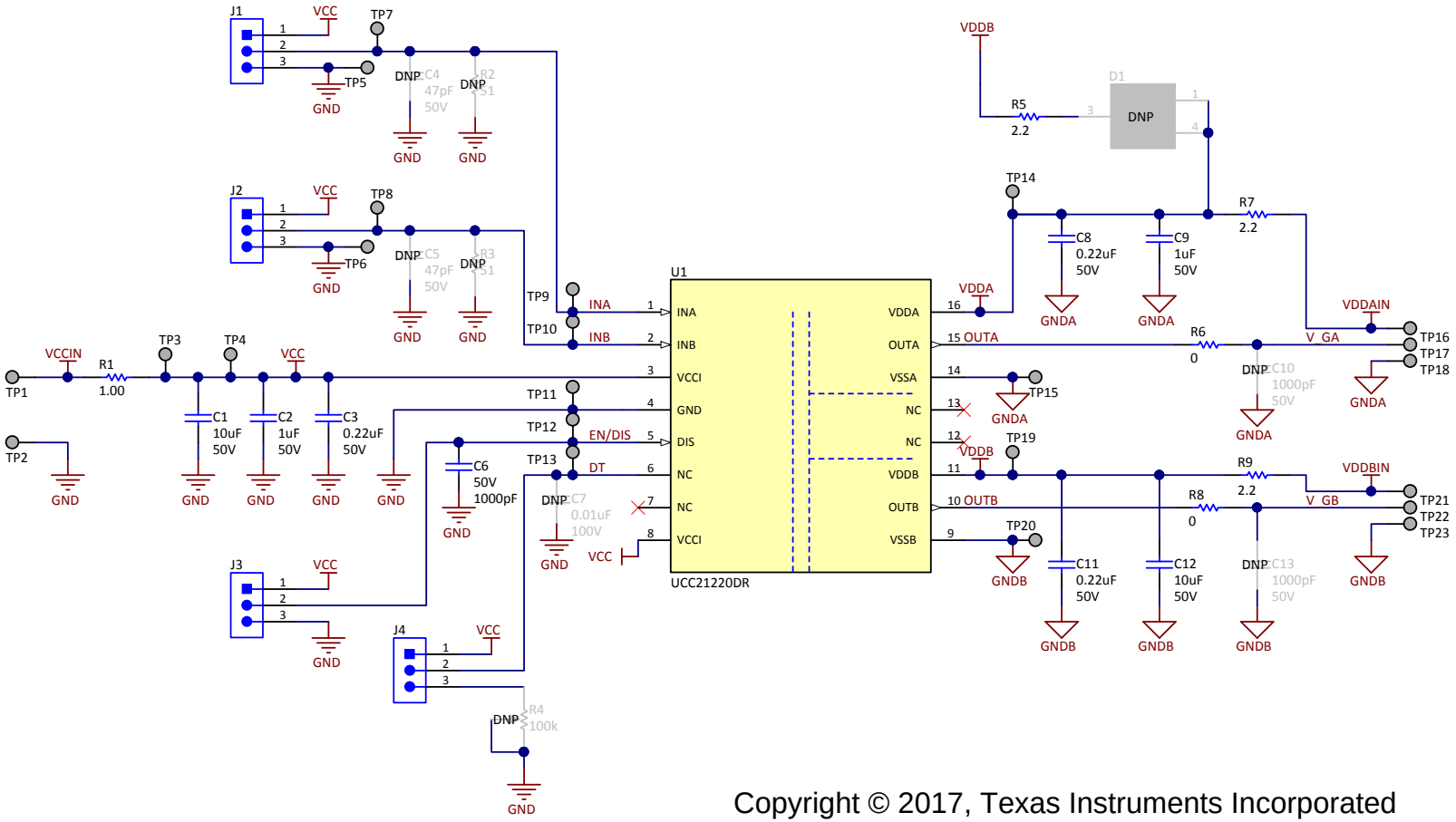

Figure 5. UCC21220EVM-009 Schematic

7 Layout Diagrams

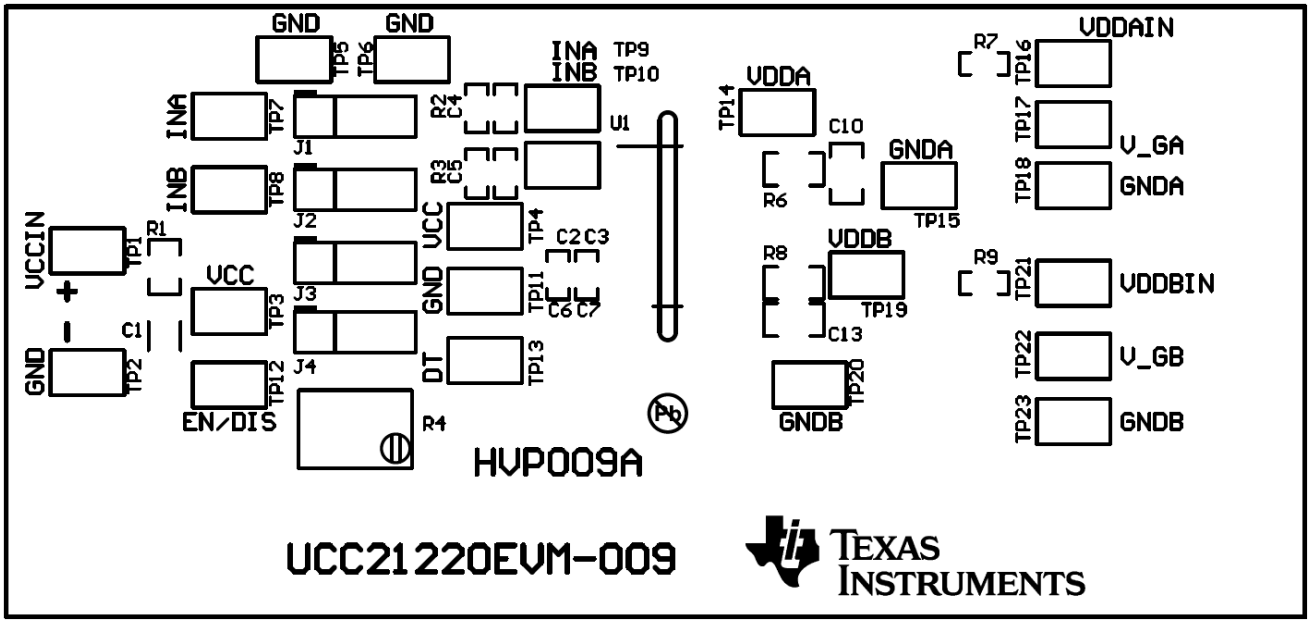

Figure 6. Top Overlay

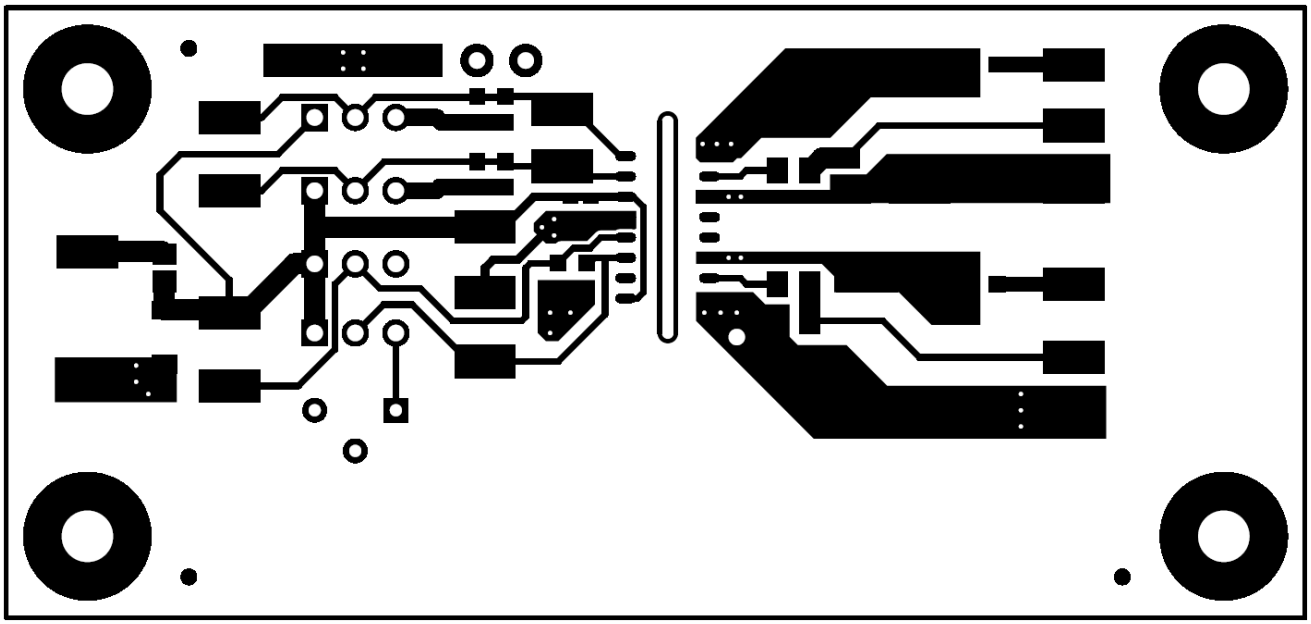

Figure 7. Top Layer

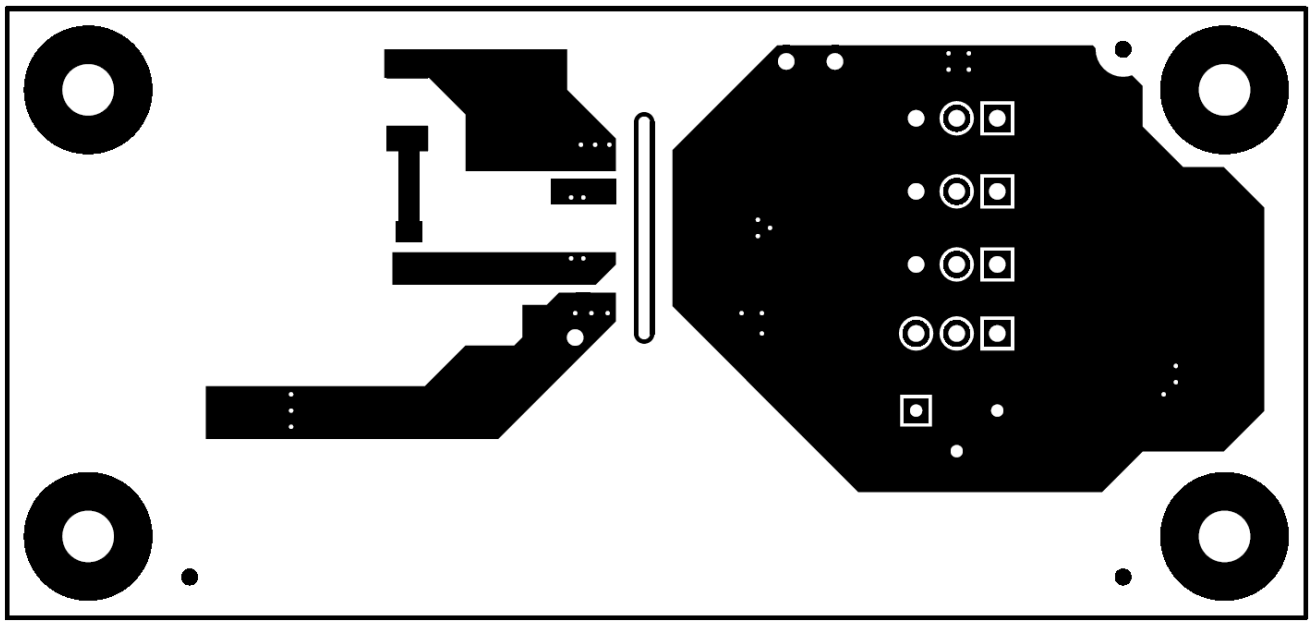

Figure 8. Bottom Layer (Flipped)

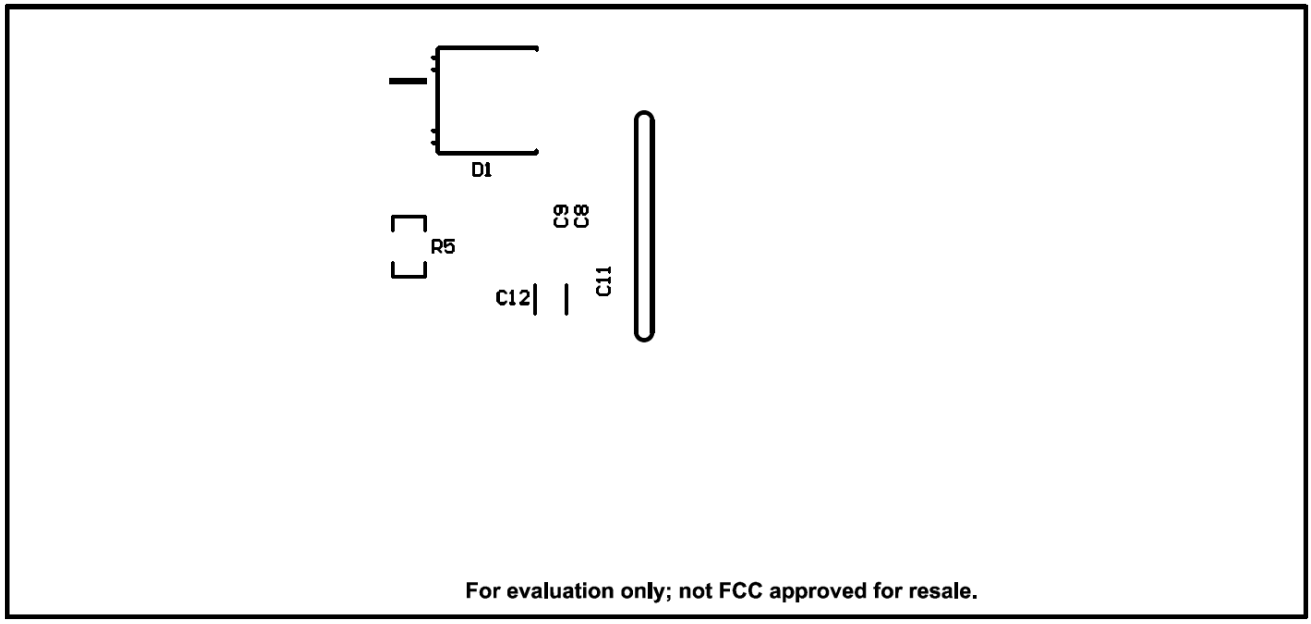

Figure 9. Bottom Overlay (Flipped)

8 Bill of Materials

Table 6. UCC21220EVM-009 Bill of Materials

QTY	Designator	Description	Part Number	Manufacturer
2	C1, C12	Capacitor, ceramic, 10 μF, 50 V, ± 10%, X5R, 1206	–	Any
2	C2, C9	Capacitor, ceramic, 1 μF, 50 V, ± 10%, X5R, 0603	–	Any
3	C3, C8, C11	Capacitor, ceramic, 0.22 μF, 50 V, ± 10%, X7R, 0603	–	Any
1	C6	Capacitor, ceramic, 1000 pF, 50 V, ± 5%, C0G/NP0, 0603	–	Any
4	H1, H2, H3, H4	Machine screw, round, no. 4 – 40 × 1/4	–	Any
4	H5, H6, H7, H8	Standoff, 0.5" L, no. 4 – 40	–	Any
4	J1, J2, J3, J4	Header, 100 mil, 3 × 1, TH	–	Any
1	R1	Resistor, 1.00 Ω, 1%, 0.125 W, 0805	–	Any
1	R5	Resistor, 2.2 Ω, 5%, 0.125 W, 0805	–	Any
2	R6, R8	Resistor, 0 Ω, 5%, 0.125 W, 0805	–	Any
2	R7, R9	Resistor, 2.2 Ω, 5%, 0.1 W, 0603	–	Any
2	SH1, SH2	Shunt, 100 mil, flash gold, black	–	Any
23	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18, TP19, TP20, TP21, TP22, TP23	Test point, miniature, SMT	–	Any
1	U1	4-A, 6-A, 3-kV_{RMS} isolated dual-channel gate driver, D0016A (SOIC-16)	UCC21220DR	Texas Instruments
0	C4, C5	Capacitor, ceramic, 47 pF, 50 V, ± 1%, C0G/NP0, 0603	–	Any
0	C7	Capacitor, ceramic, 0.01 μF, 100 V, ± 5%, X7R, 0603	–	Any
0	C10, C13	Capacitor, ceramic, 1000 pF, 50 V, ± 5%, C0G/NP0, 0805	–	Any
0	D1	Diode, Schottky, 600 V, 8 A, DPAK	–	Any
0	R2, R3	Resistor, 51 Ω, 5%, 0.1 W, 0603	–	Any
0	R4	Trimmer, 100 kΩ, 0.25 W, TH	–	Any

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (December 2017) to B Revision	Page
• Added clarification about evaluating other pin-to-pin compatible drivers in the *Introduction* and *Description* sections	2

Changes from Original (November 2017) to A Revision	Page
• Changed *Test Points and Jumpers* table and added table note	4
• Changed *Jumper (Shunt) Settings* section and *Jumpers Installation Position* image	7
• Changed *Bench Setup Diagram* section and *Bench Setup Diagram and Configuration* image	8
• Changed *Schematic* image	11
• Changed *BOM* table	14

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