

User's Guide

TPS543C20 2-Phase SWIFT™ Step-Down Converter Evaluation Module User's Guide



TEXAS INSTRUMENTS

ABSTRACT

This user's guide describes the characteristics, operation, and use of the TPS543C20 evaluation module (EVM). The user's guide includes test information, descriptions, and results. A complete schematic diagram, printed-circuit board layouts, and bill of materials are also included in this document. Throughout this user's guide, the abbreviations *EVM*, *TPS543C20EVM*, and the term *evaluation module* are synonymous with the TPS543C20EVM-869, unless otherwise noted.

Table of Contents

1 Introduction	3
1.1 Before You Begin.....	3
2 Description	4
2.1 Typical End-User Applications.....	4
2.2 EVM Features.....	4
3 EVM Electrical Performance Specifications	4
4 Schematic	5
5 Test Equipment	6
6 TPS543C20EVM-869	7
7 List of Test Points, Jumpers, and Switches	8
8 Test Procedure	9
8.1 Line and Load Regulation Measurement Procedure.....	9
8.2 Efficiency.....	9
8.3 Equipment Shutdown.....	10
9 Performance Data and Typical Characteristic Curves	10
9.1 Load Regulation.....	10
9.2 Efficiency.....	10
9.3 Power Loss.....	11
9.4 Transient Response.....	11
9.5 Output Ripple.....	13
9.6 Enable On.....	14
9.7 Control On and Off.....	15
9.8 Thermal Image.....	16
10 EVM Assembly Drawing and PCB Layout	17
11 List of Materials	22
12 Revision History	24

List of Figures

Figure 4-1. TPS543C20EVM-869 Schematic.....	5
Figure 6-1. TPS543C20EVM-869 Overview.....	7
Figure 6-2. Tip and Barrel Measurement.....	7
Figure 9-1. Load Regulation of 0.9-V Output vs Load.....	10
Figure 9-2. Efficiency of 0.9-V Efficiency vs Load.....	10
Figure 9-3. Power Loss of 0.9-V Power Loss vs Load.....	11
Figure 9-4. Transient Response of 0.9-V Output at 12 V _{IN} . Transient is 25 A to 50 A, Step is 25 A at 30 A/μs.....	11
Figure 9-5. Transient Response of 25-A to 50-A Load at 30 A/μs Rise.....	12
Figure 9-6. Transient Response of 50-A to 25-A Load at 30 A/μs Fall.....	12
Figure 9-7. Output Ripple and SW Node of 0.9-V Output at 12 V _{IN} , 80-A Output.....	13
Figure 9-8. Output Ripple and SW Node of 0.9-V Output at 12 V _{IN} , 0-A Output.....	13

Trademarks

Figure 9-9. Start-Up from Enable, 0.9-V Output at 12 V _{IN} , 80-A Output.....	14
Figure 9-10. 0.6-V Pre-Bias Start-Up From Enable, 0.9-V Output at 12 V _{IN} , 0-A Output.....	14
Figure 9-11. Output Voltage Start-Up and Shutdown, 0.9-V Output at 12 V _{IN} , 5-A Output.....	15
Figure 9-12. Controller-Target 180° Synchronization.....	15
Figure 9-13. Thermal Image at 0.9-V Output at 12 V _{IN} , 80-A Output, at 25°C Ambient.....	16
Figure 10-1. TPS543C20EVM-869 Top Layer Assembly Drawing (Top View).....	17
Figure 10-2. TPS543C20EVM-869 Top Solder Mask (Top View).....	17
Figure 10-3. TPS543C20EVM-869 Top Layer (Top View).....	18
Figure 10-4. TPS543C20EVM-869 Inner Layer 1 (Top View).....	18
Figure 10-5. TPS543C20EVM-869 Inner Layer 2 (Top View).....	19
Figure 10-6. TPS543C20EVM-869 Inner Layer 3 (Top View).....	19
Figure 10-7. TPS543C20EVM-869 Inner Layer 4 (Top View).....	20
Figure 10-8. TPS543C20EVM-869 Bottom Layer (Top View).....	20
Figure 10-9. TPS543C20EVM-869 Bottom Solder Mask (Top View).....	21
Figure 10-10. TPS543C20EVM-869 Bottom Overlay Layer (Top View).....	21

List of Tables

Table 3-1. TPS543C20EVM-869 Electrical Performance Specifications.....	4
Table 7-1. Test Point Functions.....	8
Table 8-1. List of Test Points for Line and Load Measurements.....	9
Table 8-2. List of Test Points for Efficiency Measurements.....	9
Table 11-1. TPS543C20EVM-869 List of Materials.....	22

Trademarks

All trademarks are the property of their respective owners.

1 Introduction

The TPS543C20EVM-869 uses the TPS543C20 device. The TPS543C20 is a highly integrated synchronous buck converter that is designed for up to 40-A current output per phase.

1.1 Before You Begin

The following warnings and cautions are noted for the safety of anyone using or working close to the TPS543C20EVM-869. Observe all safety precautions.

**Warning**

The TPS543C20EVM-869 circuit module may become hot during operation due to dissipation of heat. Avoid contact with the board. Follow all applicable safety procedures applicable to your laboratory.

**Caution**

Do not leave the EVM powered when unattended.

WARNING

The circuit module has signal traces, components, and component leads on the bottom of the board. This can result in exposed voltages, hot surfaces, or sharp edges. Do not reach under the board during operation.

CAUTION

The circuit module can be damaged by over temperature. To avoid damage, monitor the temperature during evaluation and provide cooling, as needed, for the system environment.

CAUTION

Some power supplies can be damaged by application of external voltages. If using more than one power supply, check the equipment requirements and use blocking diodes or other isolation techniques, as needed, to prevent damage to the equipment.

CAUTION

The communication interface is not isolated on the EVM. Be sure no ground potential exists between the computer and the EVM. Also be aware that the computer is referenced to the Battery- potential of the EVM.

2 Description

The TPS543C20EVM-869 is a two-phase, buck converter with two stacked TPS543C20 devices. It uses a nominal 12-V bus to produce a regulated 0.9-V output at up to 80-A load current (40-A per phase). The TPS543C20EVM-869 is designed to demonstrate the stacking operation of the TPS543C20 in a two-phase, low-output-voltage application while providing a number of test points to evaluate the performance of the devices. The TPS543C20EVM-869 can be modified to two separated single-phase, buck converters by changing the components assembled. Refer to the [TPS543C20 4-VIN to 14-VIN, 40-A Stackable, Synchrns Step-Down SWIFT™ Converter](#) data sheet for more information on single-phase configuration.

2.1 Typical End-User Applications

- Enterprise storage, SSD, NAS
- Wireless and wired communication infrastructure
- Industrial PCs, automation, ATE, PLC, video surveillance
- Enterprise server, switches, routers
- ASIC, SoC, FPGA, DSP core, and I/O rails

2.2 EVM Features

- Regulated 0.9-V output up to 80-A, steady-state output current
- Convenient test points for probing critical waveforms

3 EVM Electrical Performance Specifications

Table 3-1. TPS543C20EVM-869 Electrical Performance Specifications

Parameter	Test Conditions	Min	Typ	Max	Units
Input Characteristics					
V _{IN}	V _{IN} tied to V _D D	5	12	16	V
Maximum input current	V _{IN} = 12 V, I _O = 40 A, V _{OUT} = 0.9 V, F _{SW} = 500 kHz			17	A
No load input current	V _{IN} = 12 V, I _O = 0 A		105		mA
Output Characteristics					
V _{OUT}	Output voltage	0.9			V
I _{OUT}	Output load current	0	80		A
Output voltage regulation	Line regulation: input voltage = 5 V to 16 V	0.5%			
	Load regulation: output current = 0 A to I _{OUT(max)}	0.5%			
V _{OUT}	Output voltage ripple	10			mV _{PP}
V _{OUT}	Output overcurrent	96			A
Systems Characteristics					
Switching frequency	F _{SW}	500			kHz
V _{OUT}	Peak efficiency	90%			
Operating temperature		0	85		°C

4 Schematic

Figure 4-1 illustrates the EVM schematic.

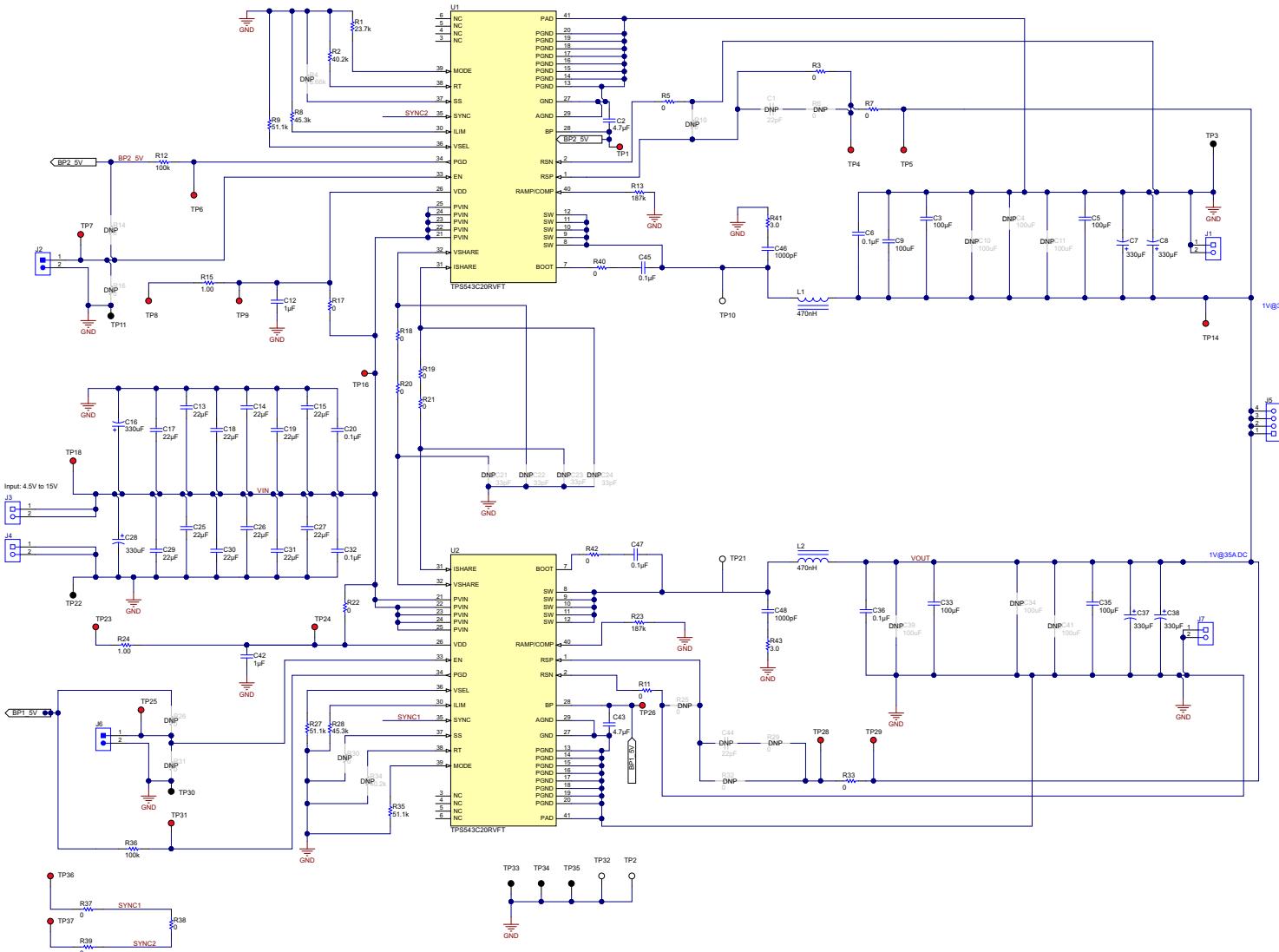


Figure 4-1. TPS543C20EVM-869 Schematic

5 Test Equipment

Voltage source: The input voltage source, V_{IN} , must be a 0-V to 18-V variable DC source capable of supplying at least 20 A_{DC}.

Multimeters: It is recommended to use two separate multimeters. One meter is used to measure V_{IN} and one to measure V_{OUT} .

Output load: A variable electronic load is recommended for testing. It must be capable of 100 A at voltages as low as 0.6 V.

Oscilloscope: An oscilloscope is recommended for measuring output noise and ripple. Output ripple must be measured using a tip-and-barrel method or better as shown in [Figure 6-2](#). The scope must be adjusted to 20-MHz bandwidth, AC coupling at 50 mV/division, and must be set to 1 μ s/division.

Fan: During prolonged operation at high loads, it may be necessary to provide forced air cooling with a small fan aimed at the EVM. Temperature of the devices on the EVM must be maintained below 105°C.

Recommended wire gauge: The voltage drop in the load wires must be kept as low as possible in order to keep the working voltage at the load within its operating range. Use the AWG 14 wire (2 wires parallel for V_{OUT} positive and 2 wires parallel for the V_{OUT} negative) of no more than 1.98 feet between the EVM and the load. This recommended wire gauge and length should achieve a voltage drop of no more than 0.2 V at the maximum 80-A load.

6 TPS543C20EVM-869

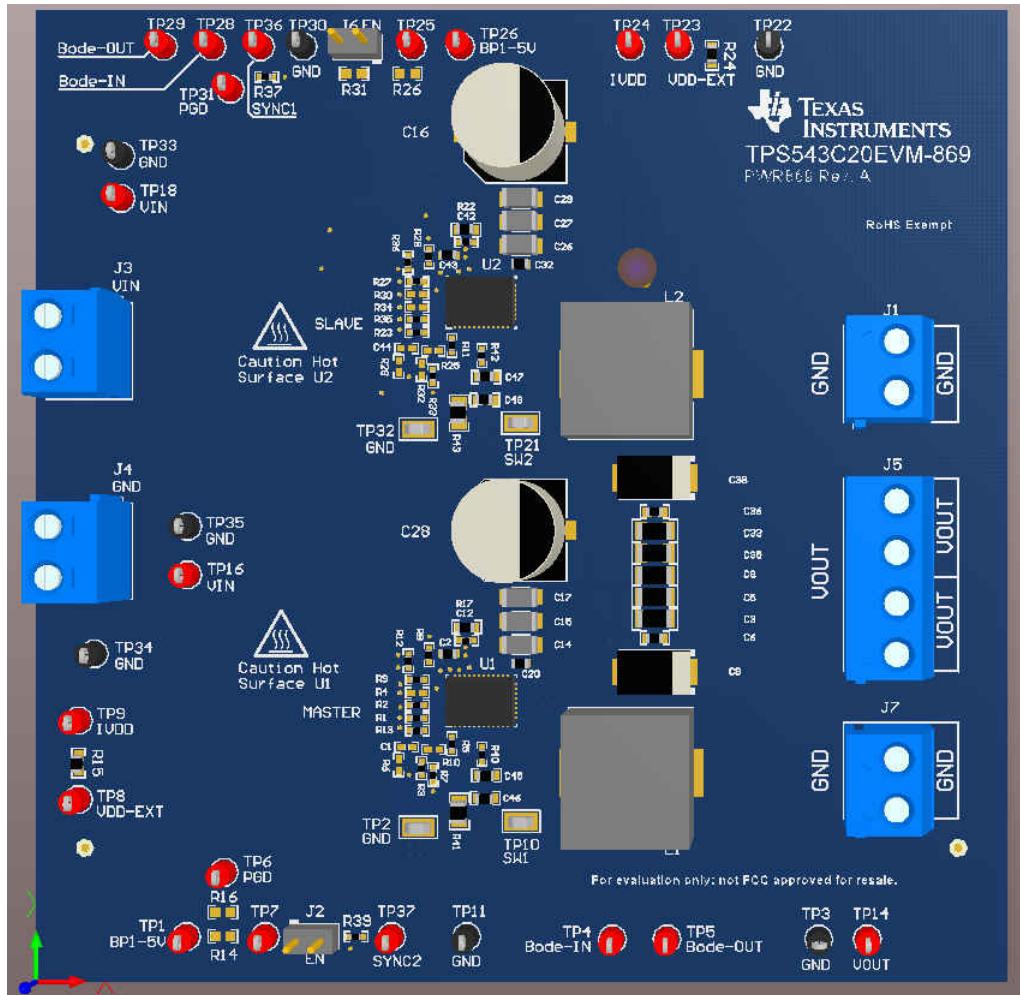


Figure 6-1. TPS543C20EVM-869 Overview

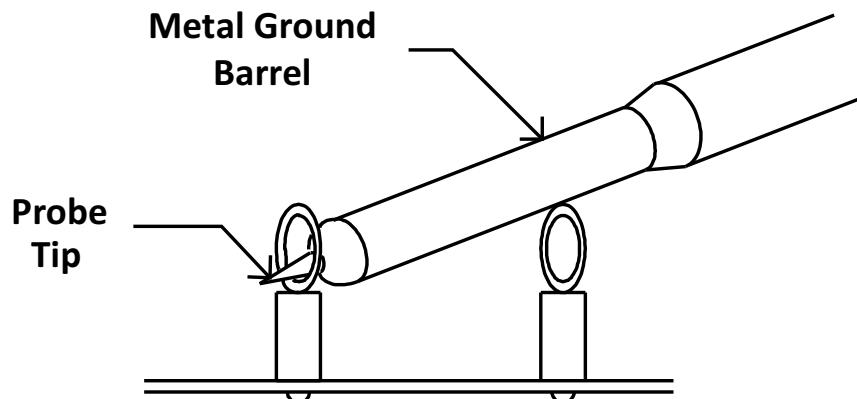


Figure 6-2. Tip and Barrel Measurement

7 List of Test Points, Jumpers, and Switches

Table 7-1 lists the test point functions.

Table 7-1. Test Point Functions

Item	Type	Name	Description
TP10	T-H loop	SW1	Power supply switch node (CONTROLLER)
TP21	T-H loop	SW2	Power supply switch node (TARGET)
TP4	T-H loop	Bode-IN	Measure loop stability (CONTROLLER)
TP28	T-H loop	Bode-IN	Measure loop stability (TARGET)
TP5	T-H loop	Bode-OUT	Measure loop stability (CONTROLLER)
TP29	T-H loop	Bode-OUT	Measure loop stability (TARGET)
TP14	T-H loop	VOUT	Sense VOUT + locally across C9. Use for efficiency and ripple measurements
TP3	T-H loop	GND	Sense VOUT – locally across C9. Use for efficiency and ripple measurements
TP16	T-H loop	VIN	Sense VIN + across C14 (CONTROLLER)
TP18	T-H loop	VIN	Sense VIN + across C26 (TARGET)
TP35	T-H loop	GND	Sense VIN – across C14 (CONTROLLER)
TP33	T-H loop	GND	Sense VIN – across C26 (TARGET)
TP9	T-H loop	VDD	Supplies the internal circuitry (CONTROLLER)
TP24	T-H loop	VDD	Supplies the internal circuitry (TARGET)
TP1	T-H loop	BP1-5V	LDO output (CONTROLLER)
TP26	T-H loop	BP1-5V	LDO output (TARGET)
TP6	T-H loop	PGD	Power good (CONTROLLER)
TP31	T-H loop	PGD	Power good (TARGET)
TP2, TP3, TP11, TP22, TP30, TP32-TP35	T-H loop	PGND	Common GND
J2	2-pin jumper	EN	Enable or disable TPS543C20 IC (CONTROLLER)
J6	2-pin jumper	EN	Enable or disable TPS543C20 IC (TARGET)
TP37	T-H loop	SYNC2	Synchronize with external switching frequency (CONTROLLER)
TP36	T-H loop	SYNC1	Synchronize with external switching frequency (TARGET)

8 Test Procedure

8.1 Line and Load Regulation Measurement Procedure

Use the following procedures for line and load regulation measurement:

1. Connect the electronic load (+) to J5 and electronic load (-) to J1 and J7 ([Figure 6-1](#)).
2. Ensure that the electronic load is set to draw 0 A_{DC}.
3. Ensure the jumper provided on the EVM shorts on J2 and J6 before V_{IN} is applied.
4. Connect input power supply (+) to J3 and input power supply (-) to J4 ([Figure 6-1](#)).
5. Increase V_{IN} from 0 V to 12 V using the digital multimeter to measure input voltage.
6. Remove the jumper on J2 and J6 to enable the controller.
7. Use the other digital multimeter or the oscilloscope to measure output voltage V_{OUT} at TP14 and TP3.

Table 8-1. List of Test Points for Line and Load Measurements

Test Point	Node Name	Description
TP14	VOUT	Sense VOUT+ locally across C9. Use for load and line measurements
TP3	GND	Sense VOUT– locally across C9. Use for load and line measurements
TP16 or TP18	VIN	Sense VIN+ across C14 or C26
TP35 or TP33	GND	Sense VIN– across C14 or C26

8. Vary the load from 0 A_{DC} to the maximum rated output of 80 A_{DC}. V_{OUT} must remain in regulation as defined in [Table 3-1](#).
9. Vary V_{IN} from 5 V to 16 V. V_{OUT} must remain in regulation as defined in [Table 3-1](#).
10. Decrease the load to 0 A.
11. Put the jumper back on J2 and J6 to disable the converter.
12. Decrease V_{IN} to 0 V or turn off the supply.

8.2 Efficiency

To measure the efficiency of the power train on the EVM, it is important to measure the voltages at the correct location. This is necessary; otherwise, the measurements will include losses in efficiency that are not related to the power train itself. Losses incurred by the voltage drop in the copper traces and in the input and output connectors are not related to the efficiency of the power train, and they must not be included in efficiency measurements.

Table 8-2. List of Test Points for Efficiency Measurements

Test Point	Node Name	Description
TP14	VOUT	Sense VOUT+ locally across C9. Use for efficiency and ripple measurements.
TP3	GND	Sense VOUT– locally across C9. Use for efficiency and ripple measurements.
TP16 or TP18	VIN	Sense VIN + across C14 or C26
TP35 or TP33	GND	Sense VIN– across C14 or C26

Input current can be measured at any point in the input wires, and output current can be measured anywhere in the output wires of the output being measured. Using these measurement points result in efficiency measurements that do not include losses due to the connectors and PCB traces.

8.3 Equipment Shutdown

Use the following steps for equipment shutdown:

1. Reduce the load current to 0 A.
2. Reduce the input voltage to 0 V.
3. Shut down the external fan, if in use.
4. Shut down equipment.

9 Performance Data and Typical Characteristic Curves

Figure 9-1 through Figure 9-13 present typical performance curves for the TPS543C20EVM-869.

9.1 Load Regulation

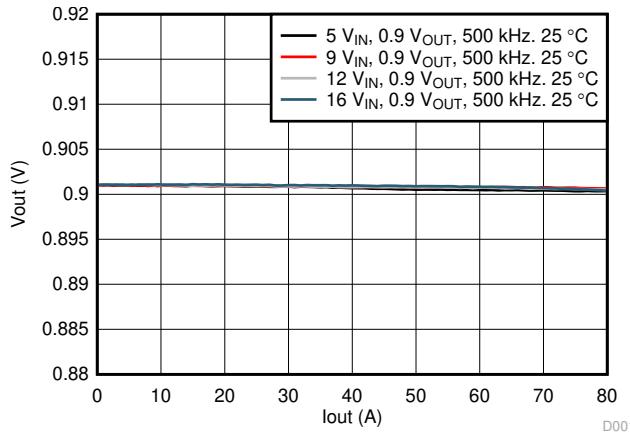


Figure 9-1. Load Regulation of 0.9-V Output vs Load

9.2 Efficiency

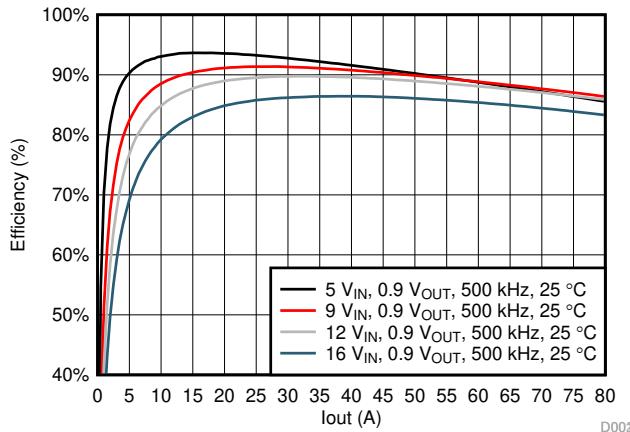


Figure 9-2. Efficiency of 0.9-V Efficiency vs Load

9.3 Power Loss

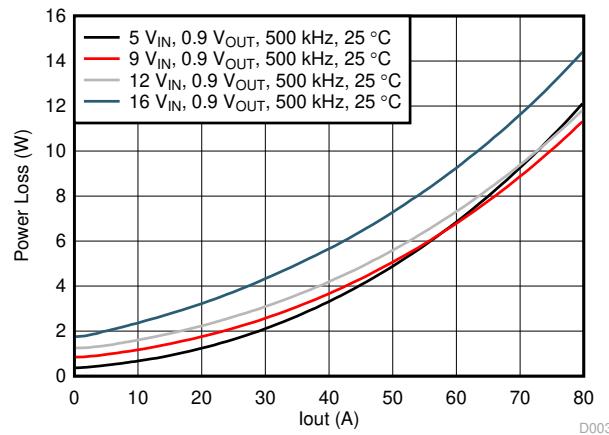


Figure 9-3. Power Loss of 0.9-V Power Loss vs Load

9.4 Transient Response



Figure 9-4. Transient Response of 0.9-V Output at 12 V_{IN}, Transient is 25 A to 50 A, Step is 25 A at 30 A/μs

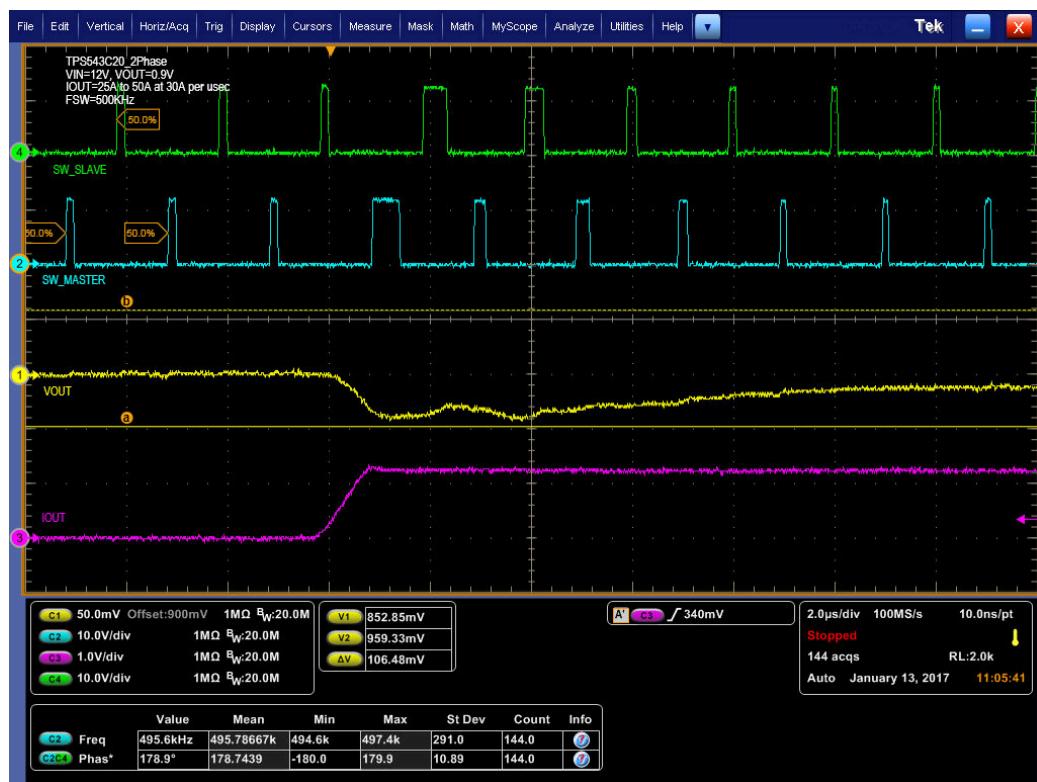


Figure 9-5. Transient Response of 25-A to 50-A Load at 30 A/μs Rise



Figure 9-6. Transient Response of 50-A to 25-A Load at 30 A/μs Fall

9.5 Output Ripple



Figure 9-7. Output Ripple and SW Node of 0.9-V Output at 12 V_{IN}, 80-A Output



Figure 9-8. Output Ripple and SW Node of 0.9-V Output at 12 V_{IN}, 0-A Output

9.6 Enable On

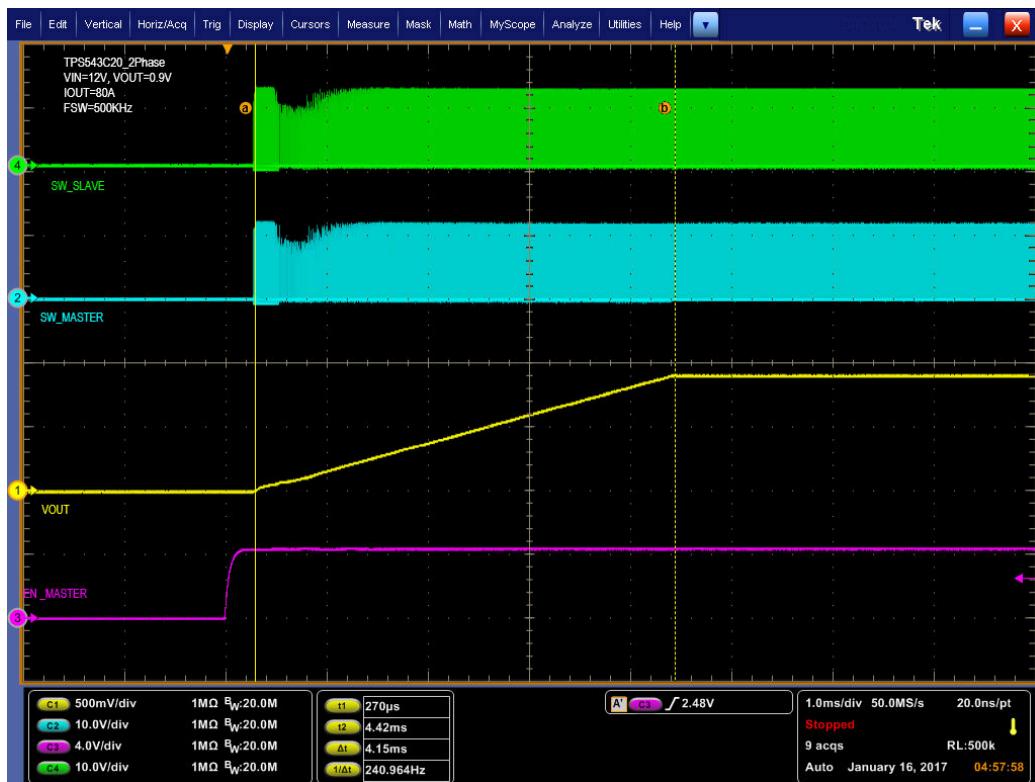


Figure 9-9. Start-Up from Enable, 0.9-V Output at 12 V_{IN}, 80-A Output

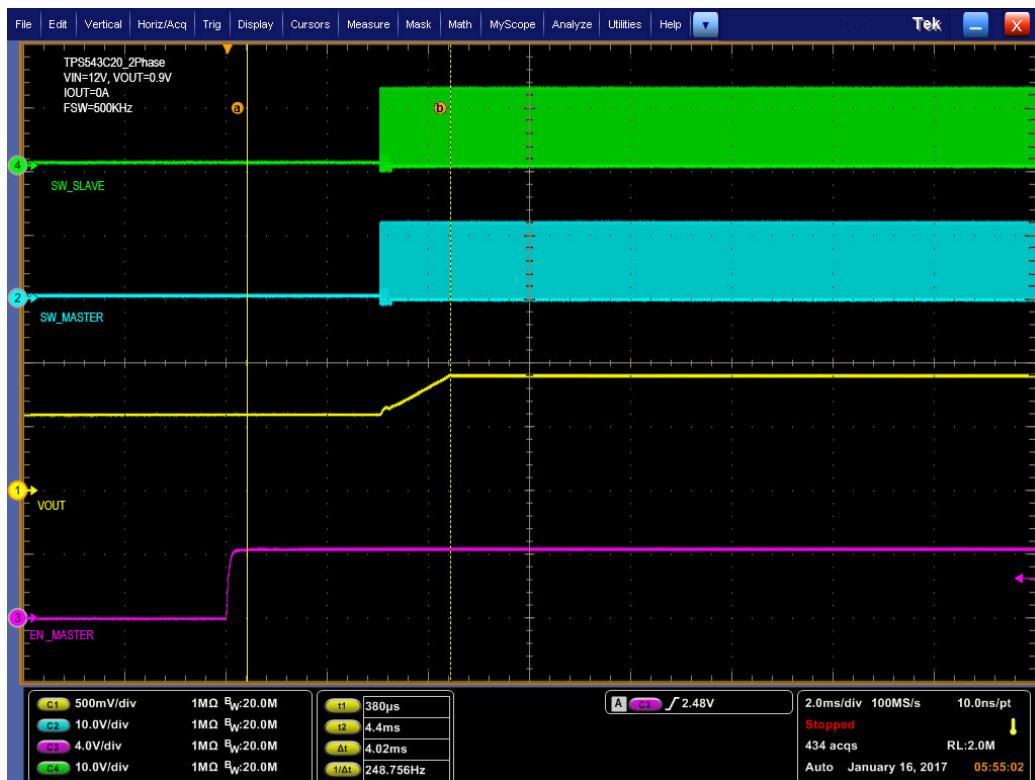


Figure 9-10. 0.6-V Pre-Bias Start-Up From Enable, 0.9-V Output at 12 V_{IN}, 0-A Output

9.7 Control On and Off



Figure 9-11. Output Voltage Start-Up and Shutdown, 0.9-V Output at 12 V_{IN}, 5-A Output

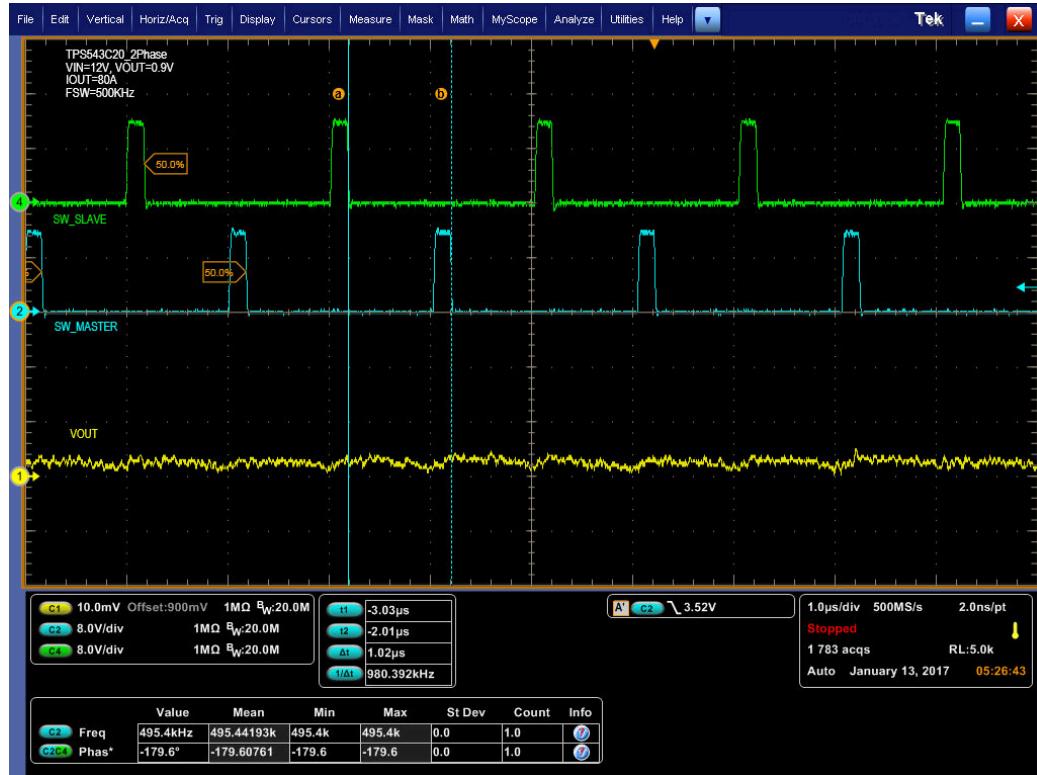


Figure 9-12. Controller-Target 180° Synchronization

9.8 Thermal Image

Figure 9-13 is a thermal image of the device.

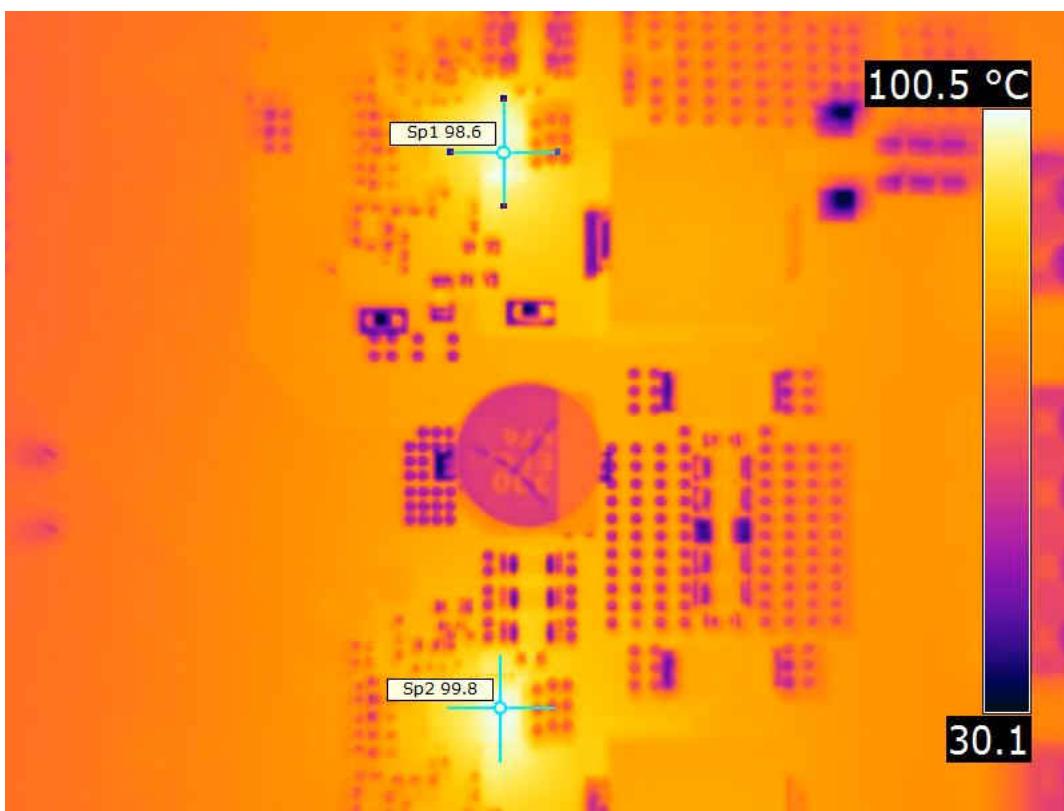


Figure 9-13. Thermal Image at 0.9-V Output at 12 V_{IN}, 80-A Output, at 25°C Ambient

10 EVM Assembly Drawing and PCB Layout

Figure 10-1 through Figure 10-8 show the design of the PWR-869EVM printed-circuit board (PCB). The PWR-869EVM has a 2-oz. copper finish for all layers.

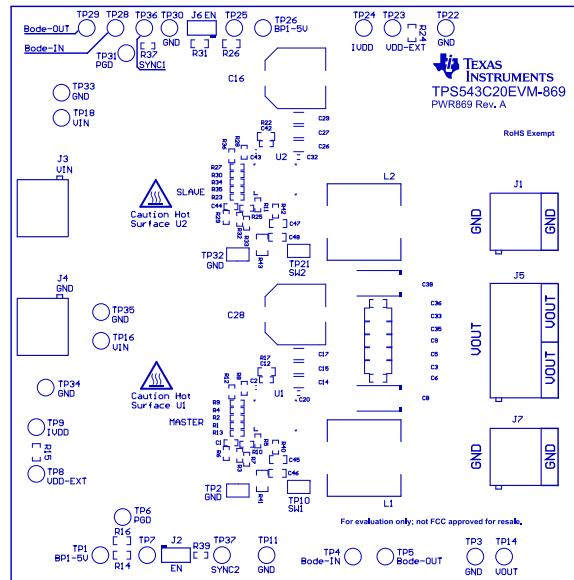


Figure 10-1. TPS543C20EVM-869 Top Layer Assembly Drawing (Top View)



Figure 10-2. TPS543C20EVM-869 Top Solder Mask (Top View)

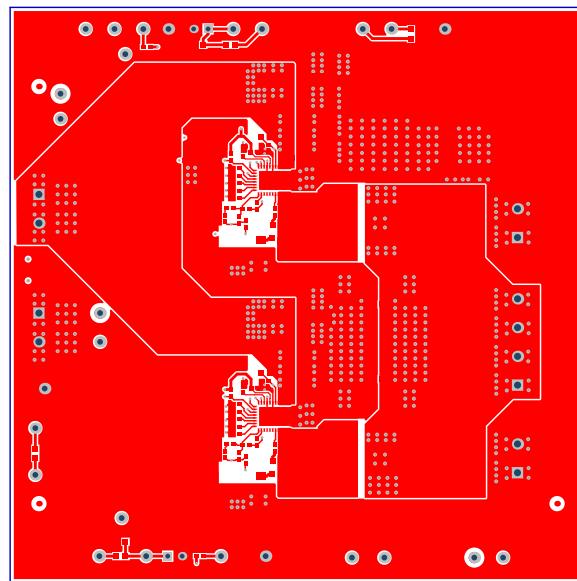


Figure 10-3. TPS543C20EVM-869 Top Layer (Top View)

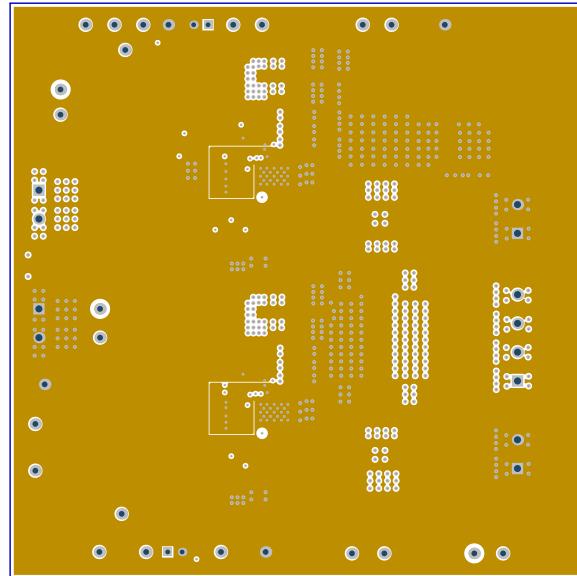


Figure 10-4. TPS543C20EVM-869 Inner Layer 1 (Top View)

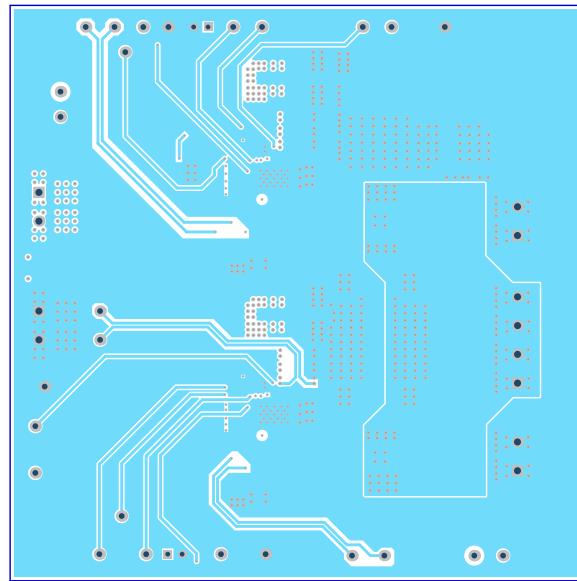


Figure 10-5. TPS543C20EVM-869 Inner Layer 2 (Top View)

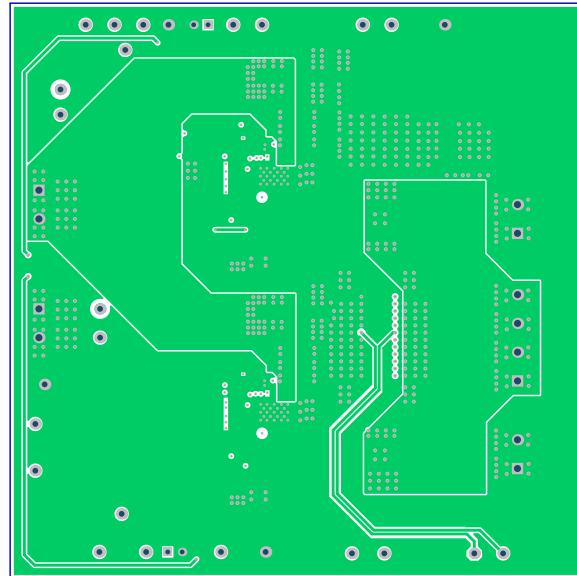


Figure 10-6. TPS543C20EVM-869 Inner Layer 3 (Top View)

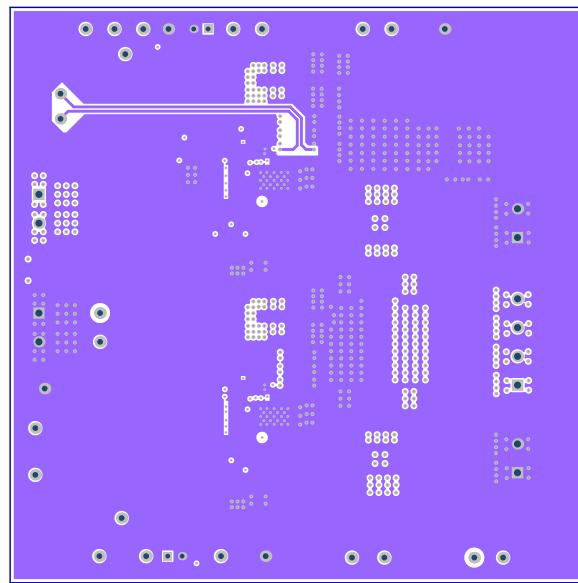


Figure 10-7. TPS543C20EVM-869 Inner Layer 4 (Top View)

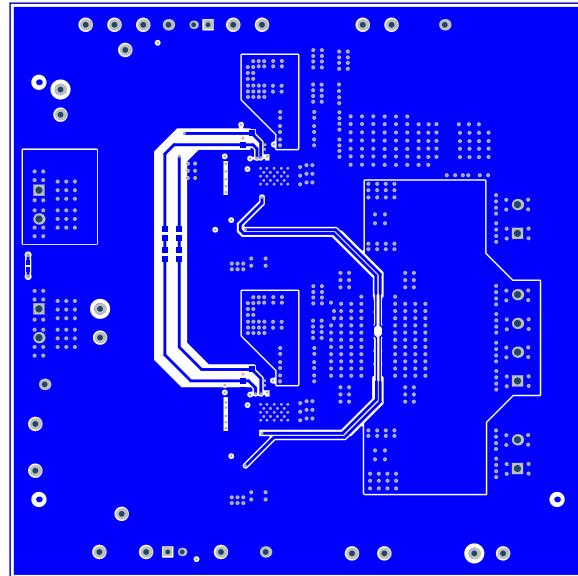


Figure 10-8. TPS543C20EVM-869 Bottom Layer (Top View)

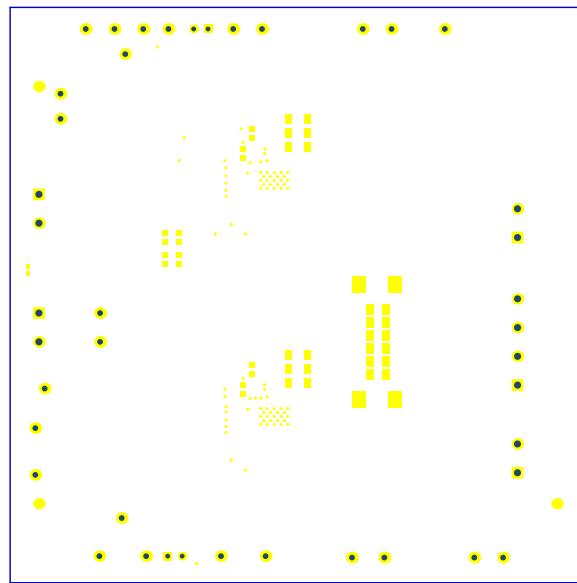


Figure 10-9. TPS543C20EVM-869 Bottom Solder Mask (Top View)

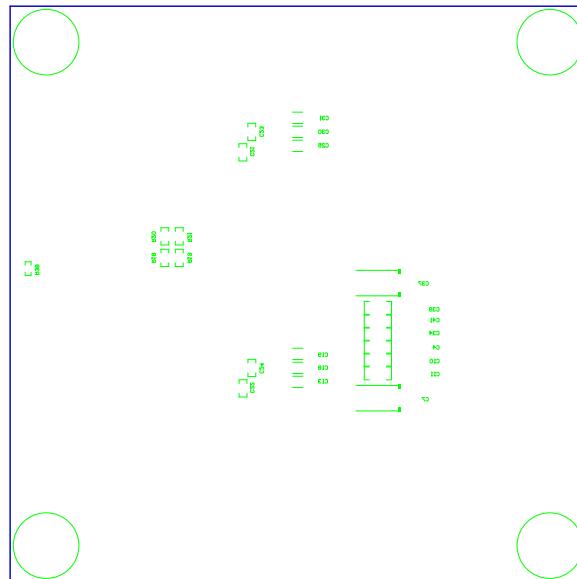


Figure 10-10. TPS543C20EVM-869 Bottom Overlay Layer (Top View)

11 List of Materials

The EVM components list, according to the schematic, is shown in [Table 11-1](#).

Table 11-1. TPS543C20EVM-869 List of Materials

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
IPCB	1		Printed Circuit Board		PWR869	Any
C2, C43	2	4.7 μ F	CAP, CERM, 4.7 μ F, 16 V, \pm 10%, X5R, 0603	0603	GRM188R61C475KAAJ	Murata
C3, C5, C9, C33, C35	5	100 μ F	CAP, CERM, 100 μ F, 6.3 V, \pm 20%, X5R, 1206	1206	GRM31CR60J107ME39L	Murata
C6, C36	2	0.1 μ F	CAP, CERM, 0.1 μ F, 10 V, \pm 10%, X7R, 0603	0603	C0603X104K8RACTU	Kemet
C7, C8, C37, C38	4	330 μ F	CAP, Aluminum Polymer, 330 μ F, 2 V, \pm 20%, 3 m Ω , 7.3 \times 1.8 \times 4.3 mm SMD	7.3 \times 1.8 \times 4.3 mm	EEFGX0D331R	Panasonic
C12, C42	2	1 μ F	CAP, CERM, 1 μ F, 25 V, \pm 10%, X5R, 0402	0402	GRM155R61E105KA12D	Murata
C13, C14, C15, C17, C18, C19, C25, C26, C27, C29, C30, C31	12	22 μ F	CAP, CERM, 22 μ F, 25 V, \pm 20%, X5R, 1206_190	1206_190	C3216X5R1E226M160AB	TDK
C16, C28	2	330 μ F	CAP, AL, 330 μ F, 25 V, \pm 20%, 0.15 Ω , SMD	SMT Radial G	EEE-FC1E331P	Panasonic
C20, C32	2	0.1 μ F	CAP, CERM, 0.1 μ F, 25 V, \pm 10%, X7R, 0603	0603	GRM188R71E104KA01D	Murata
C45, C47	2	0.1 μ F	CAP, CERM, 0.1 μ F, 50 V, \pm 10%, X7R, 0603	0603	06035C104KAT2A	AVX
C46, C48	2	1000 pF	CAP, CERM, 1000 pF, 50 V, \pm 10%, C0G/NP0, 0603	0603	06035A102KAT2A	AVX
H9, H10, H11, H12	4		Bumpon, Hemisphere, 0.44 \times 0.20, Clear	Transparent Bumpon	SJ-5303 (CLEAR)	3M
J1, J3, J4, J7	4		Terminal Block, 5.08 mm, 2 \times 1, Brass, TH	2 \times 1 5.08-mm Terminal Block	ED120/2DS	On-Shore Technology
J2, J6	2		Header, 100 mil, 2 \times 1, TH	Header, 2 \times 1, 100 mil, TH	800-10-002-10-001000	Mill-Max
J5	1		Terminal Block, 5.08 mm, 4 \times 1, Brass, TH	4 \times 1 5.08-mm Terminal Block	ED120/4DS	On-Shore Technology
L1, L2	2	470 nH	Inductor, Shielded Drum Core, Ferrite, 470 nH, 40.5 A, 0.000165 Ω , SMD	12.5 \times 13 mm	744309047	Wurth Elektronik
R1	1	23.7 k	RES, 23.7 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0402	0402	ERJ-2RKF2372X	Panasonic
R2	1	40.2 k	RES, 40.2 k, 1%, 0.063 W, 0402	0402	CRCW040240K2FKED	Vishay-Dale
R3, R5, R7, R11, R33, R37, R38, R39, R40, R42	10	0	RES, 0, 5%, 0.063 W, 0402	0402	CRCW04020000Z0ED	Vishay-Dale
R8, R28	2	45.3 k	RES, 45.3 k, 1%, 0.063 W, 0402	0402	CRCW040245K3FKED	Vishay-Dale
R9, R27, R35	3	51.1 k	RES, 51.1 k, 1%, 0.063 W, 0402	0402	CRCW040251K1FKED	Vishay-Dale
R12, R36	2	100 k	RES, 100 k, 5%, 0.063 W, 0402	0402	CRCW0402100KJNED	Vishay-Dale
R13, R23	2	187 k	RES, 187 k, 1%, 0.063 W, 0402	0402	CRCW0402187KFKED	Vishay-Dale
R15, R24	2	1.00	RES, 1.00, 1%, 0.1 W, 0603	0603	CRCW06031R00FKEA	Vishay-Dale
R17, R19, R21, R22	4	0	RES, 0, 5%, 0.1 W, 0603	0603	CRCW06030000Z0EA	Vishay-Dale
R18, R20	2	0	RES, 0, 5%, 0.1 W, 0603	0603	ERJ-3GEY0R00V	Panasonic
R41, R43	2	3.0	RES, 3.0 Ω , 5%, 0.125W, 0805	0805	RC0805JR-073RL	Yageo America
TP1, TP4, TP5, TP6, TP7, TP8, TP9, TP14, TP16, TP18, TP23, TP24, TP25, TP26, TP28, TP29, TP31, TP36, TP37	19	Red	Test Point, Miniature, Red, TH	Red Miniature Testpoint	5000	Keystone

Table 11-1. TPS543C20EVM-869 List of Materials (continued)

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
TP2, TP10, TP21, TP32	4	SMT	Test Point, Miniature, SMT	Testpoint_Keystone_Miniature	5015	Keystone
TP3, TP11, TP22, TP30, TP33, TP34, TP35	7	Black	Test Point, Miniature, Black, TH	Black Miniature Testpoint	5001	Keystone
U1, U2	2		40-A FIXED FREQUENCY NON-COMPENSATION STACKABLE SYNCHRONOUS BUCK CONVERTER, RVF0040A	RVF0040A	TPS543C20RVFT	Texas Instruments
C1, C44	0	22 pF	CAP, CERM, 22 pF, 50 V, ±5%, C0G/NP0, 0402	0402	C1005C0G1H220J050BA	TDK
C4, C10, C11, C34, C39, C41	0	100 µF	CAP, CERM, 100 µF, 6.3 V, ±20%, X5R, 1206	1206	GRM31CR60J107ME39L	Murata
C21, C22, C23, C24	0	33 pF	CAP, CERM, 33 pF, 100 V, ±5%, C0G/NP0, 0603	0603	06031A330JAT2A	AVX
FID1, FID2, FID3, FID4, FID5, FID6	0		Fiducial mark. There is nothing to buy or mount.	Fiducial	N/A	N/A
R4	0	8.66 k	RES, 8.66 k, 1%, 0.063 W, 0402	0402	CRCW04028K66FKED	Vishay-Dale
R6, R10, R25, R29, R30	0	0	RES, 0, 5%, 0.063 W, 0402	0402	ERJ-2GE0R00X	Panasonic
R14, R16, R26, R31	0	0	RES, 0, 5%, 0.1 W, 0603	0603	CRCW06030000Z0EA	Vishay-Dale
R32	0	0	RES, 0, 5%, 0.063 W, 0402	0402	CRCW04020000Z0ED	Vishay-Dale
R34	0	40.2 k	RES, 40.2 k, 1%, 0.063 W, 0402	0402	CRCW040240K2FKED	Vishay-Dale

12 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (February 2017) to Revision A (February 2022)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.	3
• Updated the user's guide title	3

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated