Application Note

How to Size the VCC Cap for a VCC Self-Biasing Based GaN Flyback Converter

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ABSTRACT

This application note addresses how to size the VCC capacitor for a VCC self-biased gallium nitride (GaN) integrated flyback converter. This document first addresses the benefits of VCC self-bias in USB PD charger applications. Subsequently, the document explains VCC self-bias under different AC line and load conditions, emphasizing the VCC self bias role in maintaining a stable VCC voltage and the impact on no-load power consumption. The discussion further extends to the design calculations for appropriate VCC capacitance, verifying both a stable VCC voltage and a minimized no-load power consumption, targeting as low as 30mW. This comprehensive analysis provides essential guidelines for improving the performance and efficiency of GaN-based flyback converters in power-sensitive applications.

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Trademarks

1 Introduction

AC-DC USB power delivery (PD) charger require higher efficiency with compact size, and this presents a significant challenge for power supply design. For power applications below 100W, the quasi-resonant (QR) flyback is especially popular due to improved efficiency and reduced switching losses, achieved by leveraging valley switching techniques. With advancements in semiconductor technologies such as GaN, the flyback topology continues to achieve higher power density and efficiency, making this an option for applications such as USB PD chargers and other compact power supplies. Figure 1-1 shows TI's GaN integrated flyback with self-bias VCC UCG28826 application.

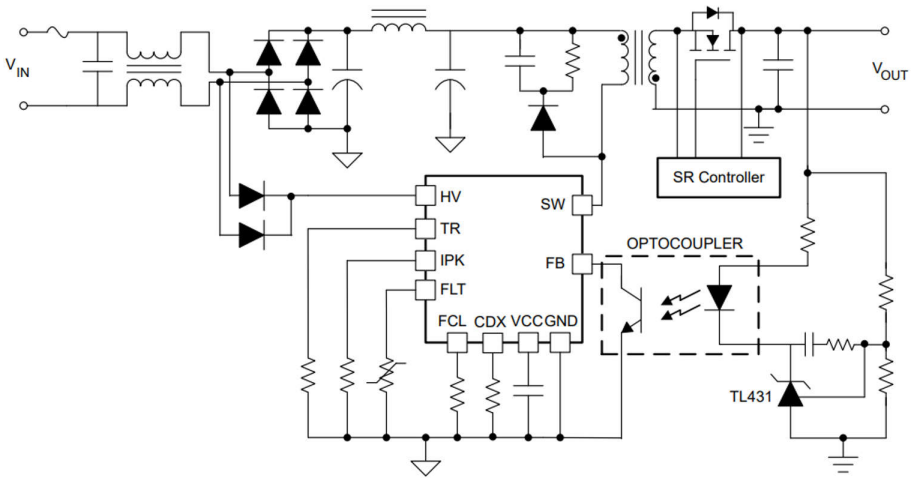

Figure 1-1. Simplified Schematic of AC/DC Flyback Converter using UCG28826

For most flyback controllers, the VCC pin provides the bias to the device, which powers the internal references, gate driver, regulators, control circuits and protection features. An extra rectification circuit through the auxiliary winding is required to offer VCC bias. As a result, the VCC bias obtained using this method is proportional to the output voltage. This consequently raises two issues: auxiliary winding increases the volume of the circuit and applications that require wide output voltage range require an internal and external power conversion stage to reduce to VCC range, increasing external components and reducing efficiency.

Self-biasing VCC circuitry is an option for the problems mentioned above. By adopting a capacitor at the VCC pin, the energy stored in both the switch node and the transformer can be harvested as power supply for the controller. Using this method, auxiliary winding is no longer required. This method leverages proper configuration of external capacitor to achieve accurate voltage sensing and output voltage. Additionally, the elimination of the auxiliary winding not only simplifies transformer manufacturing but also streamlines the EMI design process.

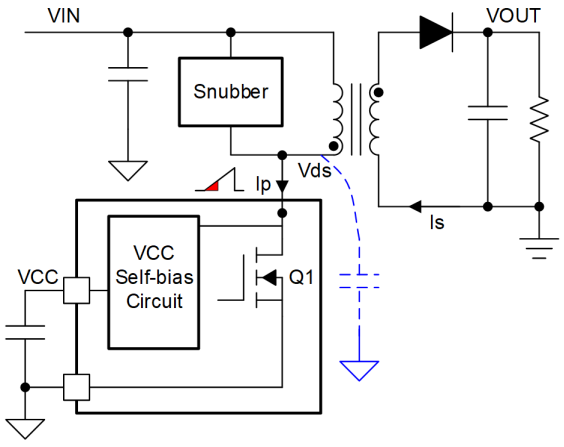

Figure 1-2. VCC Self-Bias

2 VCC Self-Bias at Different AC Line and Load Conditions

The VCC self-biasing circuit is designed to perform energy harvesting based on both input and output conditions. As shown in Figure 2-1, the circuit achieves energy harvesting from the switching node capacitor during QR flyback operation. Under specific conditions, such as low AC line input, when the reflected output voltage equals or exceeds the VBUS input voltage, and no energy stored in the Coss capacitor, energy harvesting from the inductor occurs, as shown in Figure 2-1. A small portion of the primary switching current is directed to the VCC capacitor through an internal path. Consequently, the UCG28826 seamlessly enables energy harvesting from both the capacitor and inductor under varying operational conditions.

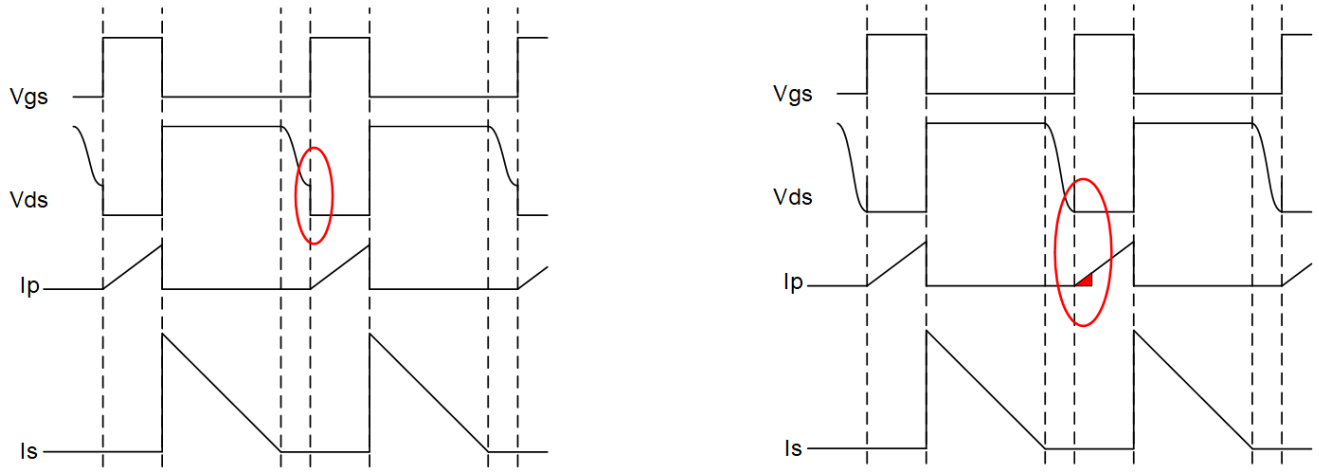

Figure 2-1. VCC Capacitor Energy Harvest

To verify the VCC voltage is sustained across every switching cycle, a potential challenge arises during extended periods without switching events, such as in open-load conditions or burst mode, where the non-switching interval can extend beyond 40ms. During such prolonged intervals, additional energy is required to maintain the VCC voltage. The UCG28826 addresses this by sourcing VCC bias from the high-voltage (HV) pin when the VCC voltage drops below 5.6V, as shown in Figure 3-1. However, this method can be less efficient, particularly when the HV pin voltage is significantly higher than the VCC voltage. To optimize efficiency, charge the VCC capacitor when the HV pin voltage is close to the VCC level, typically around the zero-crossing points of the AC line cycle. This approach minimizes energy loss and enhances VCC charging efficiency, which improves no-load power consumption performance. Failure to implement this strategy can adversely affect the overall power efficiency of the system under light or no-load conditions. Because of this, properly configuring the value of the VCC capacitor is important.

3 VCC Capacitor Configuration

Assume the condition that VCC voltage is slightly above the 5.6V threshold for triggering VCC charging (Assume VCC = 5.61V for example), and right after a zero-crossing event on the HV pin. In this case, calculate the capacitance required to make sure the VCC voltage does not drop below a survival level of 5.3V, which activates the HV charging path, before the next half-line cycle zero-crossing. As the quiescent current of UCG28826 in burst mode equals 250mA, the voltage drops from 5.6V to 5.3V in 10.6ms (half of 47Hz AC period), the VCC capacitance must be 8.83μF according to Equation 1

$$I = C \times dV/dt \tag{1}$$

Accounting for DC voltage derating, temperature effects, and tolerance, a 10μF capacitor is the least capacitance to maintain VCC voltage regulation with the self-bias feature, or the VCC voltage drops below 5.3V in half AC line cycle and trigger random charging event when the HV pin goes high which can cause extra no load power consumption. As shown in Figure 3-1, when VCC capacitor is 4.7μF, the VCC charging frequency is random, and no load power consumption is 86mW in this case.

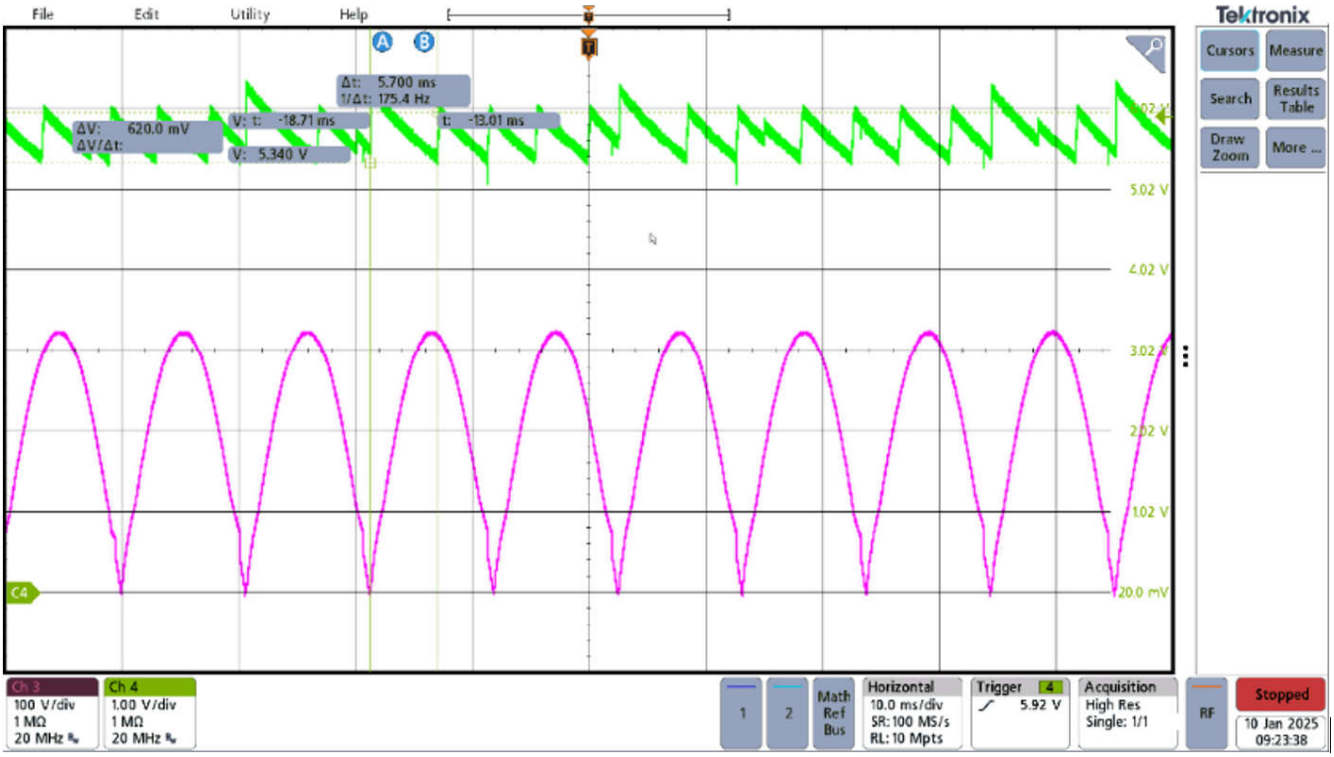

Figure 3-1. 230VAC,47Hz, VCC=4.7uF, Open Load, 89mW Standby Power, CH3: HV CH4: VCC

VCC capacitance can increase to extend the time holding above the 5.3V in half AC cycle, so that the capacitance is less likely to charge VCC at AC zero-crossing. As shown in Figure 3-2, when VCC capacitor is 20μF, VCC charging frequency is 47Hz, and no load power consumption is 28mW.

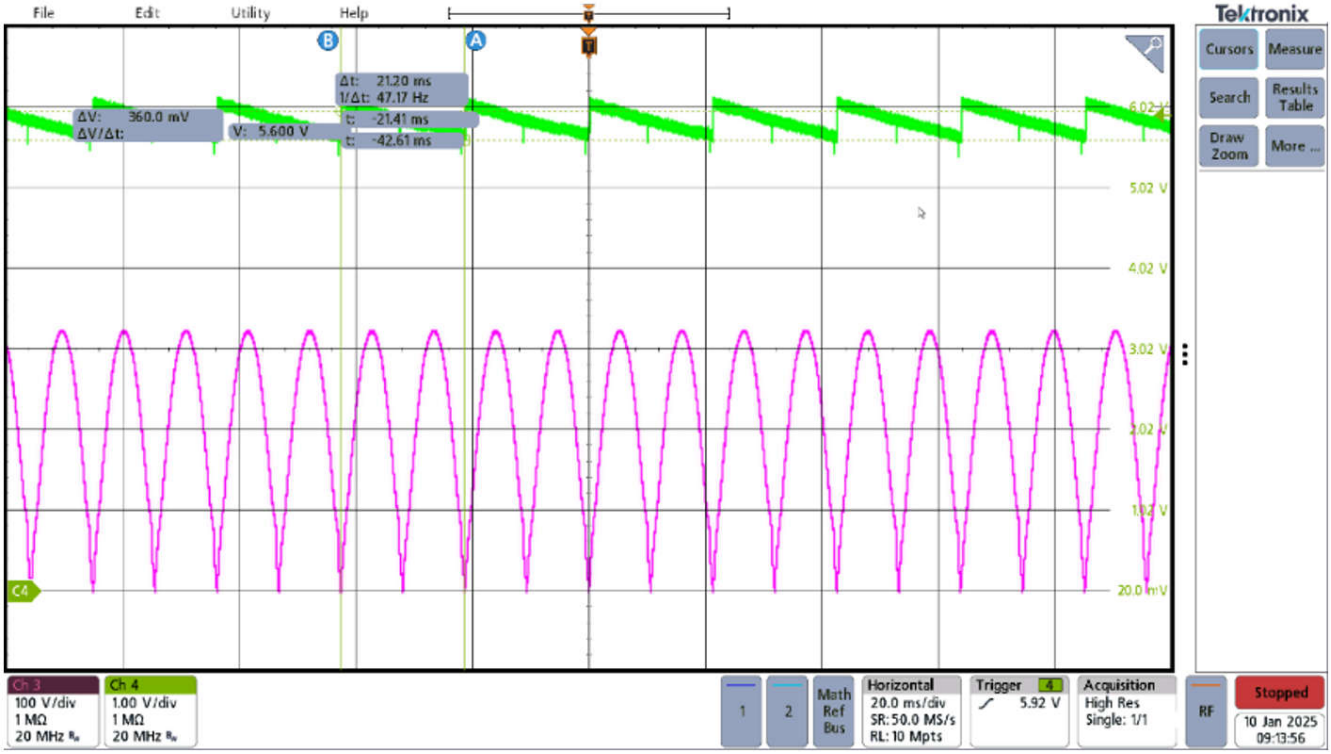

Figure 3-2. 230VAC, 47Hz, VCC=20uF, Open Load, 28mW Standby Power, CH3: HV CH4: VCC

Table 3-1 lists the performance conclusion table with different VCC capacitors.

Table 3-1. Performance Conclusion Under Different C_{VCC}

Test Condition	C_{VCC}	VCC Charging Frequency	No Load Power Consumption
230VAC, 47Hz, open load	4.7μF	Random	86mW
230VAC, 47Hz, open load	20μF	47Hz	28mW
230VAC, 47Hz, open load	44μF	47/2=23.5Hz	27.2mW

To verify the accuracy of the test results, do not use a high capacitance probe on the HV pin or assert any larger resistor in series of the HV pin. In terms of the first case, given that the HV pin is characterized by high impedance, the presence of additional capacitance on this pin can impede the ability to discharge to approximately 0V during each half-cycle of the AC line. This interference can cause the IC to fail in synchronizing with the line frequency at the zero-crossing point. Consequently, the VCC charging process can occur irregularly at the HV pin voltage, leading to an increase in no-load power consumption. In terms of the second case, connecting a high-value resistor in series with the HV pin restricts the charging current to VCC during the AC zero-crossing phase. As a result, the charging of VCC can occur irregularly at higher input voltages once VCC falls below the 5.3V threshold required for survival mode, and can also lead to an increase in no-load power consumption.

4 65W AC-DC USB PD Charger Based on VCC Self-Biasing GaN Flyback

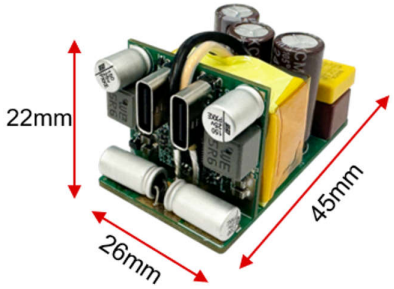

Figure 4-1. PMP41117 Design

Table 4-1. PMP41117 Design Parameter

Parameter	Value
AC Input voltage	90-264VAC
Output voltage	5-20V/3.25A
Transformer	ATQ23-14
Turn ratio	7:1
Transformer Inductance	200uH
Switching frequency	90-140kHz
Efficiency	93.2% at 90VAC
Power density	2.3W/CC

Figure 4-1 and Table 4-1 show a 65W dual USB port AC-DC USB PD charger design. Leveraging the simplified VCC self-bias circuit and the advanced high-level integration of the GaN-based design which uses the UCG28826, this design achieves a power density of 2.3W/cc and an efficiency of 93.2% for the AC-DC conversion stage.

5 Summary

The traditional VCC bias circuit of the controller, along with the associated auxiliary winding in the transformer and rectifier can be entirely eliminated by introducing a VCC self-bias circuit, which enhances the efficiency of the VCC bias circuit across a wide range of output voltages. This document provides design guidelines on sizing the VCC capacitor to verify proper operation. With this feature, engineers can achieve a more streamlined and optimized USB PD charger design.

6 References

1. Texas Instruments, *Universal AC Input 65W Dual USB Type-C® Port USB PD Charger Reference Design With Integrated GaN*, test report.
2. Texas Instruments, *UCG28826 Self-biased High Frequency QR Flyback Converter with Integrated GaN*, data sheet.

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