Application Note

Synchronization to a Clock Signal Using AC Coupling

Cyril Alinsub, Britton Jones

ABSTRACT

DC/DC converters can be synchronized to a clock signal to improve system performance. Typically, if the device starts up before an external clock signal is applied, then the internal PWM oscillator frequency is set by the R_{FSEL} resistor. In this scenario, a high impedance buffer can be used to isolate the clock to maintain the proper R_{FSEL} detection when the clock is unused. This application note introduces how to provide this isolation using a simple AC coupled circuit instead of a buffer, and how to choose the corresponding component values to stay within the absolute voltage ratings of the TPS543620 device used in testing this implementation.

Table of Contents

List of Figures

List of Tables

Trademarks

HotRod™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

1 Introduction

Slight variations in switching frequency when using multiple DC/DC converters can introduce additional challenges to the system design that can be mitigated by synchronizing the switching frequency to a common clock generator. For example, switching frequency synchronization allows users to filter out a predictable frequency band to eliminate potential adverse effects to other components in the system. Users can also have multiple DC/DC converters in a design switch at the same frequency but in different phases, minimizing input voltage, current ripple and EMI effects.

The TPS543620 family of devices are high-performance synchronous DC/DC converters that utilize the internally-compensated, fixed-frequency Advanced Current Control mode control topology and deliver high efficiency in a small 2.5mm x 3mm HotRod™ VQFN package. These devices are available in a 3A, 6A and 8A version, and can operate from 500kHz to 2.2MHz. The devices can also be synchronized to an external clock directly connected to the SYNC/FSEL pin.

To enable external clock synchronization, apply a square wave clock signal to the SYNC/FSEL pin with a duty cycle from 20% to 80%. The clock can either be applied before the device starts up or during operation. If the clock is to be applied before the device starts, then a resistor between SYNC/FSEL and AGND is not needed. In the case that the device starts up before an external clock signal is applied, then the internal PWM oscillator frequency is set by the R_{FSEL} resistor. There are five possible frequency options for the TPS543620 and the corresponding programming resistor values are listed in Table 1-1.

Table 1-1. TPS543620 Switching Frequency Selection

R_{FSEL} ALLOWED NOMINAL RANGE (1%) (kΩ)	RECOMMENDED E96 STANDARD VALUE (1%) (kΩ)	RECOMMENDED E12 STANDARD VALUE (1%) (kΩ)	Fsw (kHz)
>=24.0	24.3	27	500
17.4-18.0	17.4	18	750
11.8-12.1	11.8	12	1000
8.06-8.25	8.06	8.2	1500
<=5.11	4.99	4.7	2200

The device maintains this switching frequency until the clock signal is applied, at which point the device begins synchronizing to this clock after counting four consecutive switching cycles. This application note assumes that the clock is not present before the device starts, necessitating the need for a high impedance design to verify proper detection of the R_{FSEL} resistor.

AC coupling refers to a method used in electronics circuits where a capacitor is added in series on the signal line, functioning as a high-pass filter that allows AC signals to pass through while blocking DC signals. In a DC/DC converter clock synchronization application, a clock signal functions as a DC signal that oscillates between a high and low state at a constant frequency. Utilizing an AC coupled circuit effectively isolates the clock generator from the rest of the components down the path to verify proper detection of the R_{FSEL} value and regulates the clock signal to be within the necessary voltage values of the SYNC/FSEL pin. The clock synchronization high-level input voltage threshold of the device is 1.8V and the absolute minimum input voltage on the SYNC/FSEL pin is -0.3V.

2 Choosing Component Values

There are three additional passive components needed to realize effective clock synchronization of a DC/DC converter using an AC coupled circuit: a capacitor, resistor, and Schottky diode. The schematic for the setup used in the validation of this application note is shown in Figure 2-1. Users must also consider the amplitude and frequency of the applied clock signal.

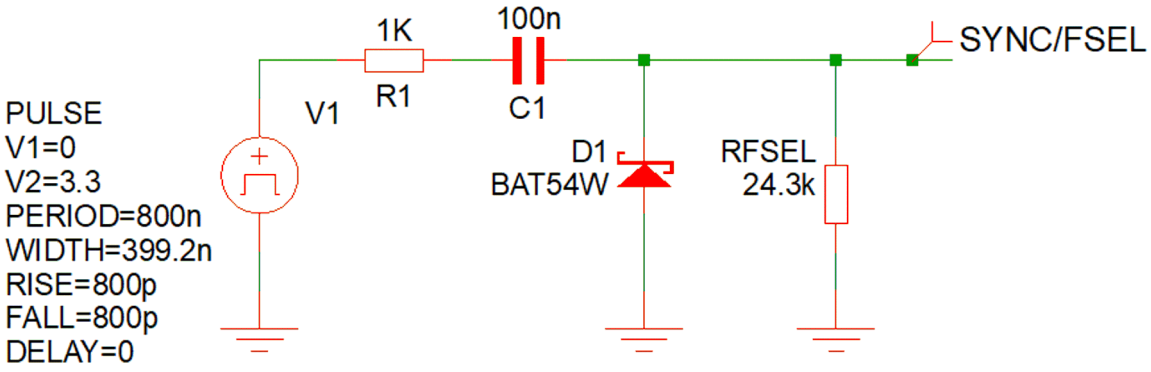

Figure 2-1. AC Coupled Circuit Schematic

2.1 Capacitor

A small capacitor is used for this application, referred to as C1 in Figure 2-1. In this application note, a minimum of 1nF and a maximum of 100nF capacitor is validated and was found to have no significant difference in performance. Note that a 100nF capacitor is the typical value of the bootstrap capacitor needed for the BOOT pin, which can lead to simpler procurement.

2.2 Resistor

In addition to R_{FSEL} used to select the internal PWM oscillator frequency, there is a single resistor in series between the clock generator and capacitor, referred to as R1 in Figure 2-1. A requirement is to use a 1% tolerance resistor or better.

The acceptable values for R1 depend on the chosen clock signal amplitude and switching frequency. At lower switching frequencies, there is less voltage drop across this circuit, resulting in a higher voltage applied to the SYNC/FSEL pin, but still lower than the clock signal amplitude. In this case, a higher value for R1 can be used as long as the SYNC/FSEL pin receives at least 1.8V. When a high switching frequency is selected, there is a greater amount of voltage drop across this circuit, thus a lower R1 value must be used for 1.8V to reach the SYNC/FSEL pin. The results of all the tested R1 and switching frequency values are tabulated in Table 3-1.

When using a 3.3V clock signal, the recommended value for R1 is 1.1kΩ, as this keeps the voltage applied to the SYNC/FSEL pin above the necessary 1.8V threshold while keeping the negative voltage element above -300 mV across all selectable switching frequencies.

2.3 Clock Signal

A minimum voltage of 1.8V is needed to be applied to the SYNC/FSEL pin of the TPS543620 to enable clock synchronization. The clock signal frequency needs to also be within ±20% of the frequency set by R_{FSEL}. The chosen switching frequency setting also has an effect on the voltage applied to the SYNC/FSEL pin. At lower switching frequencies, there is less voltage drop across this circuit, resulting in a higher voltage applied to the SYNC/FSEL pin. Common clock signal amplitudes include 1.8V, 2.5V, 3.3V, and 4.5V.

A clock signal of at least 3.3V is recommended to reach the minimum high-level input voltage of 1.8V across all possible selectable switching frequencies of the device, assuming that a 1.1kΩ R1 is used. Using a clock signal greater than 3.3V is possible and can allow for greater possible R1 values. Using a lower clock voltage than 3.3V is also possible, but there is a limitation to the switching frequency options possible and a lower R1 value can be needed to verify at least 1.8V is applied to the SYNC/FSEL pin.

2.4 Schottky Diode

A Schottky diode is chosen to remove the negative voltage from the clock signal after passing through the capacitor and also due to the functionality at higher switching frequencies. There are numerous possible Schottky diode packages with different voltage and current ratings. The Schottky diode used in this application is a BAT54W with a 30V V_{RRM} rating and 200mA I_F rating. When selecting a Schottky diode for this application, the main consideration is that the diode is rated for voltages higher than the maximum amplitude of the clock signal, has some potential overshoot, and has a similar current rating.

3 Results

For this application note, different combinations of R1, R_{FSEL}, and C1 were analyzed and the high voltage and low voltage applied to the SYNC/FSEL pin were recorded. A function generator was used to emulate a clock generator signal, with the output configured to a square wave with an amplitude of 3.3V and the frequency changing depending on the chosen R_{FSEL}. For the sake of evaluation, this circuit was built using through-hole components, however surface-mount versions of these components are easy to find for a traditional application. All results were taken with three EVMs running in parallel. A summary of the results of the various test configurations is shown in Table 3-1.

Table 3-1. AC Coupled Circuit Test Results

R_{FSEL} (kΩ)	F_{SW} (kHz)	R_1 (kΩ)	C_1 (nF)	Clock Signal Frequency (kHz)	SYNC/FSEL High Voltage (V)	SYNC/FSEL Low Voltage (V)
24.3	500	1.1	100	600	2.64	-0.160
24.3	500	1.1	1	600	2.56	-0.120
4.99	2200	1.1	100	2000	1.8	-0.180
4.99	2200	1.1	1	1900	1.8	-0.200
11.7	1000	1.1	1	1200	2.28	-0.200
11.7	1000	0.5	1	1200	2.56	-0.160
11.7	1000	2	1	1200	2	-0.160

The oscilloscope shots measuring the switching frequency of the TPS543620, the voltage at the SYNC/FSEL pin, and the voltage of the clock signal when the clock is turned off and on are shown in Figure 3-1 through Figure 3-11. For example, The switching frequency of the device when the signal generator is off is shown in Figure 3-1. Channel 1 is the voltage applied to the SYNC/FSEL pin, channel 2 is the switching frequency of the device, and channel 3 is the function generator signal. The device is switching at 514.2kHz, which corresponds to the selected frequency value of the 24.3kΩ R_{FSEL}. The dynamic change of the switching frequency once the signal generator is turned on is shown in Figure 3-2. The switching frequency of the device is recorded to be 599.6kHz, lining up with the values selected for the clock signal, which is set to an amplitude of 3.3V with a frequency of 600kHz. The SYNC/FSEL pin is receiving a signal with a high of 2.66V and a low of -140mV, which is within the specs of the device pin.

3.1 Waveforms

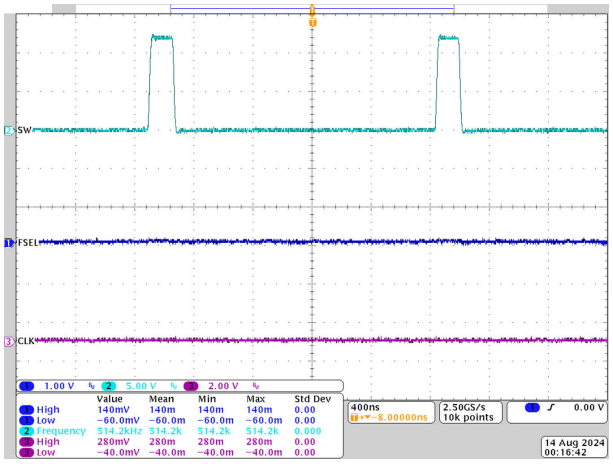

Figure 3-1. Clock Off, Rfsel = 24.3kΩ, R1 = 1.1kΩ, C1 = 100nF

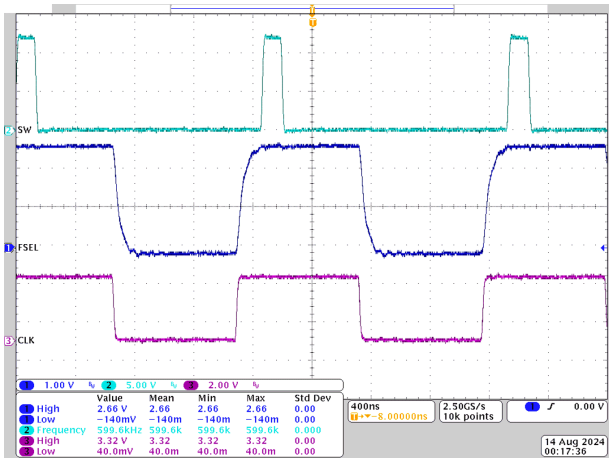

Figure 3-2. Clock Frequency = 600kHz, Clock Amplitude = 3.3V, Rfsel = 24.3kΩ, R1 = 1.1kΩ, C1 = 100nF

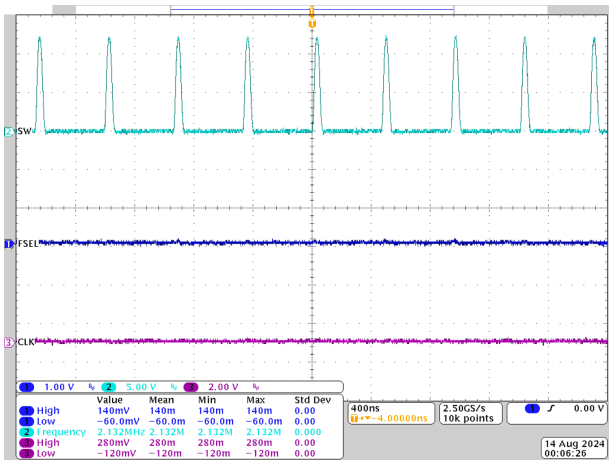

Figure 3-3. Clock Off, R1 = 1kΩ, Rfsel = 4.99kΩ, C1 = 100nF

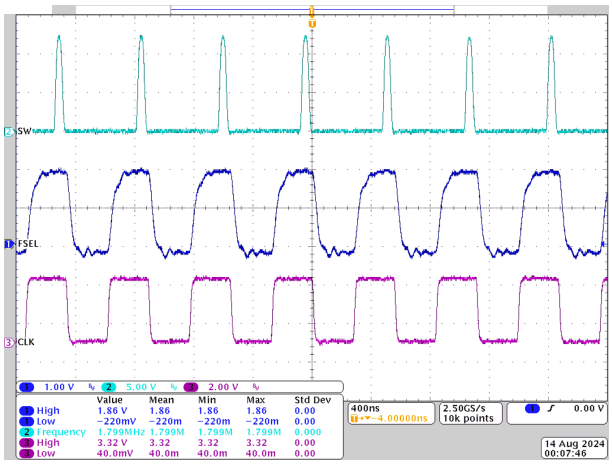

Figure 3-4. Clock On, Clock Frequency = 1.8MHz, Clock Amplitude = 3.3V, R1 = 1kΩ, Rfsel = 4.99kΩ, C1 = 100nF

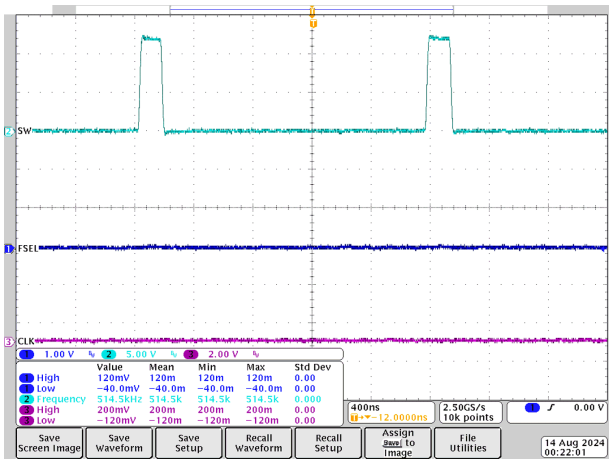

Figure 3-5. Clock Off, R1 = 1kΩ, Rfsel = 24.3kΩ, C1 = 1nF

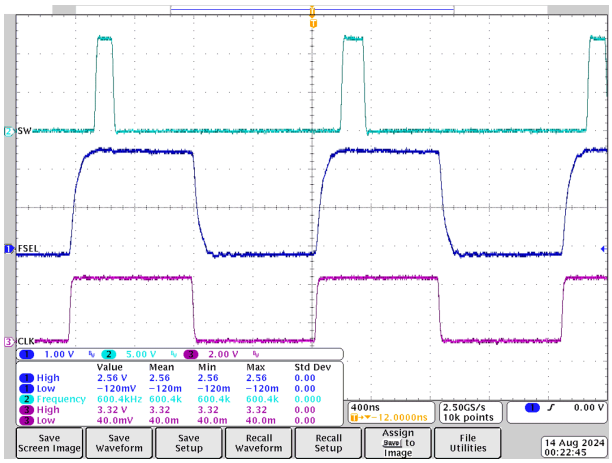

Figure 3-6. Clock On, Clock Frequency = 600kHz, Clock Amplitude = 3.3V, R1 = 1kΩ, Rfsel = 24.3kΩ, C1 = 1nF

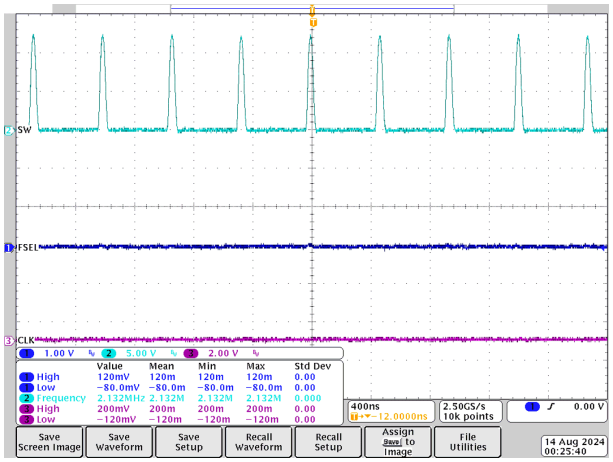

Figure 3-7. Clock Off, R1 = 1kΩ, Rfsel = 4.99kΩ, C1 = 1nF

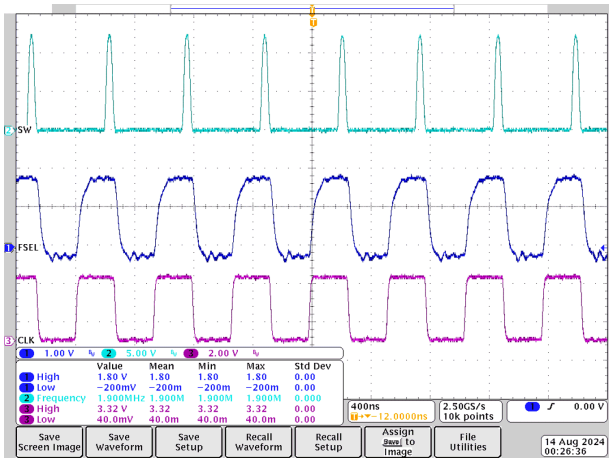

Figure 3-8. Clock On, Clock Frequency = 1.9MHz, Clock Amplitude = 3.3V, R1 = 1kΩ, Rfsel = 4.99kΩ, C1 = 1nF

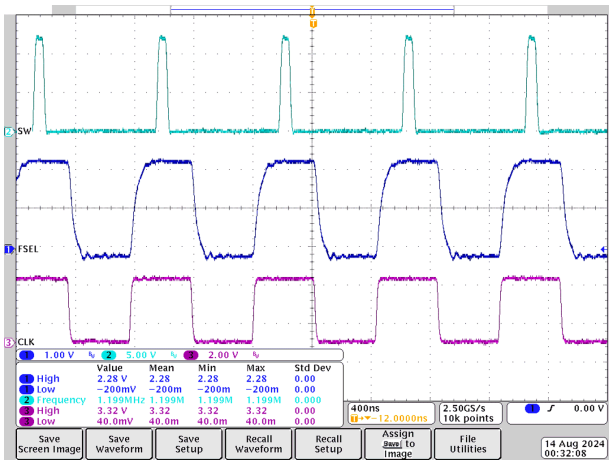

Figure 3-9. Clock On, Clock Frequency = 1.2MHz, Clock Amplitude = 3.3V, R1 = 1kΩ, Rfsel = 11.7kΩ, C1 = 1nF

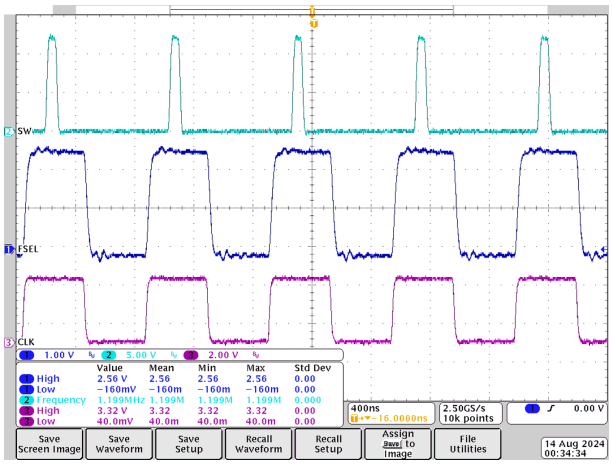

Figure 3-10. Clock On, Clock Frequency = 1.2MHz, Clock Amplitude = 3.3V, R1 = 500kΩ, Rfsel = 11.7kΩ, C1 = 1nF

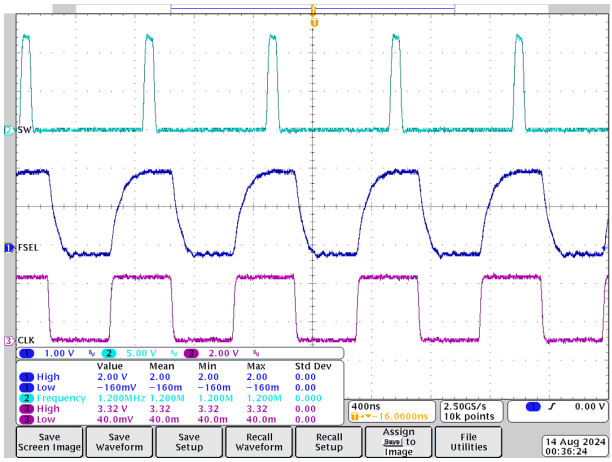

Figure 3-11. Clock On, Clock Frequency = 1.2MHz, Clock Amplitude = 3.3V, R1 = 500kΩ, Rfsel = 11.7kΩ, C1 = 1nF

3.2 Bill of Materials

The bill of materials used in the testing of this application is shown in Table 3-2.

Table 3-2. Bill of Materials

Component	Value	Quantity	Description
Capacitor	1nF	3	CAP, CERM, 1nF, 50V, X7R
Capacitor	100nF	3	CAP, CERM, 100nF, 50V, X7R
Resistor	24.3kΩ	3	RES, 24.3kΩ, ±1%, 0.25W, Axial
Resistor	4.99kΩ	1	RES, 4.99kΩ, ±1%, 0.25W, Axial
Resistor	11.7kΩ	1	RES, 11.7kΩ, ±1%, 0.25W, Axial
Resistor	1.1kΩ	1	RES, 1.1kΩ, ±1%, 0.25W, Axial
Resistor	0.5kΩ	1	RES, 0.5kΩ, ±1%, 0.25W, Axial
Resistor	2kΩ	1	RES, 2kΩ, ±1%, 0.25W, Axial
Diode	BAT54W	3	BAT54W

4 Summary

This application note introduces how to utilize an AC coupled circuit to keep the signal from a clock generator within the absolute voltage ratings for the SYNC/FSEL pin to avoid damaging the DC/DC converter. This circuit is designed to adhere to the synchronization high-level input voltage threshold of 1.8V for the device and the absolute minimum input voltage on the SYNC/FSEL pin of -0.3V. Acceptable component values are discussed and results of a typical application circuit are shown. For a standard clock voltage of 3.3V, we found that an R1 value of 1.1kΩ, C1 value from 1nF to 100nF and a BAT54W satisfied the SYNC/FSEL pin requirements for the TPS543620.

5 References

- Texas Instruments, *TPS543620 4V to 18V Input, 6A Synchronous SWIFT™ Step-Down Converter with Internally Compensated Advanced Current Mode Control* data sheet.
- Texas Instruments, *TPS543620 SWIFT™ Step-Down Converter Evaluation Module User's Guide*
- Texas Instruments, *Synchronizing DC/DC Converters in a Power Tree*, application note.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265