Application Note

Choosing Appropriate Protection Approach for IGBT and SiC Power Modules

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ABSTRACT

Identifying and protecting short circuit (SC) and over current (OC) scenarios are critical for high power systems like HEV-EV traction inverters and EV charging and solar inverters system. In high-power systems, SiC FETs or IGBTs are generally used depending upon the power level and switching frequency. This application note discusses the key considerations and design approaches to implement the right protection circuit based on SiC FETs and IGBTs. It walks through the timings involved from detecting the SC/OC event to safe shut-down, the circuit implementation criteria and experiment data for both IGBT and SiC FETs. It summarizes the right protection driver for IGBTs and SiCs based on the released isolated gate drivers from TI.

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1 Introduction

Isolated gate drivers are commonly used in automotive and industrial high-power systems such as HEV/EV traction inverters, solar inverters, and motor drives. In these applications, silicon carbide (SiC) MOSFETs and Si IGBTs are usually ideal candidates; their abilities to handle high voltage, high current are beneficial in high power systems in the hundreds of kW range. All the high-power applications use power modules with increased voltage and current capability.

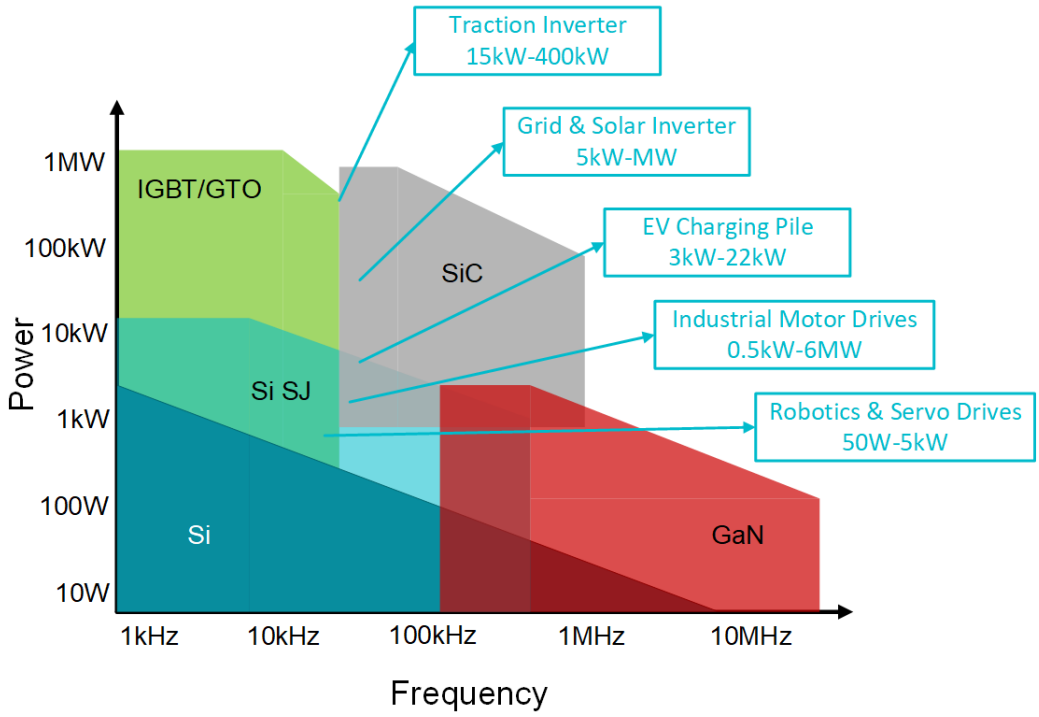

Figure 1-1. Power Switch Types With Different System Power Levels

This application note talks about some of the common failure modes of the SiC and IGBT power switches, characteristics, the best suitable protection approach based on the power module type and the protection circuit component design aspects.

2 SiC and IGBT Characteristics

Though both used in high-voltage, high-power systems, IGBT and SiC FETs are intrinsically different in their voltage-current characteristics, resulting in difference in their overvoltage and short-circuit protection timing and shutdown energy.

Both Si IGBT's and SiC FET's regions of operation are shown in Figure 2-1. For IGBTs, at low collector-emitter voltage (V_{CE}), the device is in its linear region, and the collector current (I_C) increases as V_{CE} increases. IGBT has a saturation V_{CE} voltage, and beyond the V_{CE} saturation point, it operates in the active region, meaning the current is relatively flat as V_{CE} increases. This saturation V_{CE} voltage is usually used to determine when the short-circuit protection starts to engage, with the corresponding I_C being the short circuit threshold current (I_{SC}). Since only V_{CE} increases and Ic stays stable during IGBT short circuit, the power dissipation increases relatively slowly, so IGBTs usually can tolerate longer duration of short-circuit event (around 10µs).

SiC, on the other hand, usually operates in the linear region. As a short-circuit event happens, the drain-source voltage (V_{DS}) and the drain current (I_D) increase simultaneously, resulting in faster-rising power dissipation. Because of this operating mode, the timing is more critical. SiC can usually only tolerate a short duration of short-circuit event (typically 2-3µs) before the power switch starts breaking down.

Thus, it is crucial to select the right short-circuit protection mechanism as well as suitable protection voltage (V_{CE}/V_{DS}) and load current (I_C/I_D) threshold to safely and efficiently turn off the device when a short-circuit event happens.

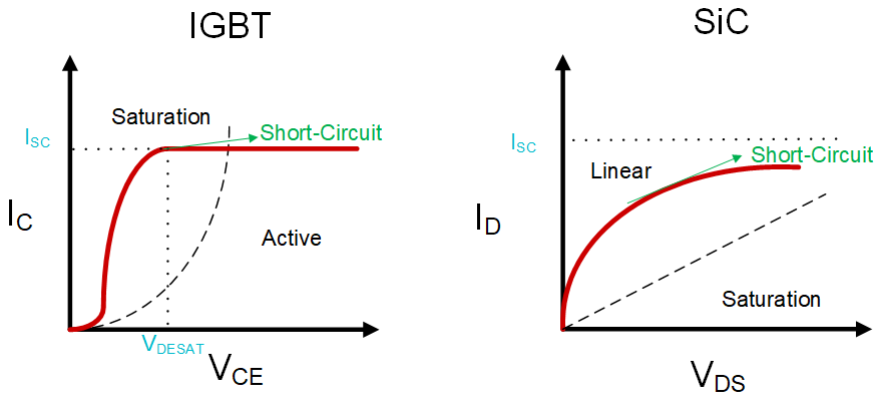

Figure 2-1. SiC and IGBT Characteristics

3 Failure Modes

In case of the IGBTs and SiC power modules, the common failure reasons are:

- **Dielectric break down failure**
  - Both IGBTs and SiC have voltage limits at the Gate pin and the Drain/Collector pin with respect to the Source/Emitter, respectively. If the applied voltage to the power module exceeds the max supported voltage, it causes the power module to fail. So, the applied voltage and also system noise have to be controlled so that the voltage does not exceed the maximum supported Gate, Drain/Collector voltage of the power module.
- **Thermal runaway failure**
  - Another common failure reason for the power module is thermal runaway. During high current operations, due to the internal resistance of the power module, the power module temperature increases. If the power module is placed in an extreme temperature environment or exceeds its maximum current limit continuously, thermal runaway failure may occur. So, the power module temperature needs to be controlled with an effective cooling mechanism and the operating current needs to be controlled to not exceed its rated operating current.

- **Over-current /short-circuit failure (SC)**
  - Over-current and short-circuit failures are the common reasons for power module failure. In a multiphase system, there can be different types of Short-circuit failures and it can happen due to the reasons provided in Table 3-1.

Table 3-1. OC/SC Failure Conditions and the Failure Reasons

Failure Condition	Reason for the Failure
Shoot-through on a phase	Controller malfunction /noise interference
Phase to phase short circuit	Insulation breakdown between the phases
Phase to earth short circuit	Insulation breakdown between phase to casing

For the scope of the gate driver protection approach, focus on the following power module failure possibilities and how the gate driver can protect the power modules effectively.

- Short-circuit/Over-current failure: due to noise/controller malfunction
- Di-electric Over-voltage failure: during switching at high di/dt condition (mostly post SC Event)

4 Short-Circuit Protection Approaches

There are two major protection approaches applicable in terms of detecting short-circuit (SC) and over-current (OC) events.

1. Current threshold (I_{SC})-based protection
2. Voltage threshold (V_{SC})-based protection

- **Current threshold (I_{SC})-based protection**
  - During both SC and OC events, the current is increased at least 10x or more, so detecting the increased I_{CE}/I_D accurately is one of the approaches to detect the OC/SC event. The detection logic needs to be defined so that the detection current threshold is at least 1.5 to 2 times higher than the maximum operating current. Providing enough margin helps to avoid false detection during the maximum operating current.
- **Voltage threshold (V_{SC})-based protection**
  - Based on IGBT and SiC power module IV characteristics, another approach to detect the OC/SC event is by measuring the voltage across the power module effectively to detect the faulty condition. During the OC/SC event, the voltage across the power module (both V_{CE} and V_{DS}) increases to a much higher value than the normal operating condition. The current saturation characteristic in an IGBT gives us a very clear V_{CE} voltage at which point you can decisively say the IGBT is leaving the saturation region, or “De-saturating". In case of SiC, it is recommended to define 2x the normal operating voltage to detect the OC/SC threshold.

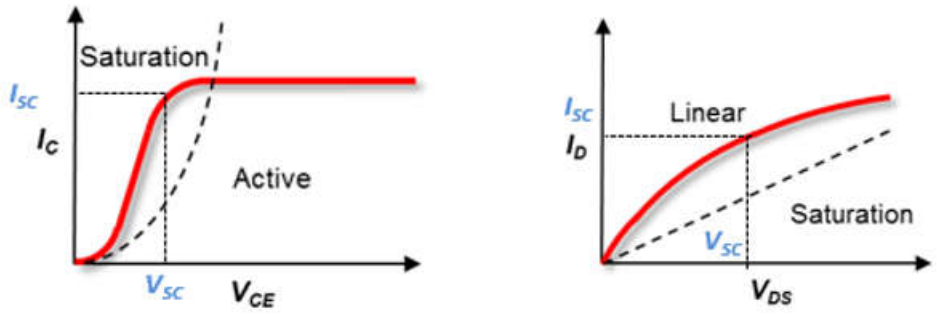

Figure 4-1. V_{SC} and I_{SC} Thresholds on IGBT and SiC IV Curves

4.1 Short-Circuit Current-Based Protection Implementation

There are two implementation options for current detection approach:

- Shunt resistor based approach
- R-sense resistor based approach

Option1: Shunt resistor-based approach

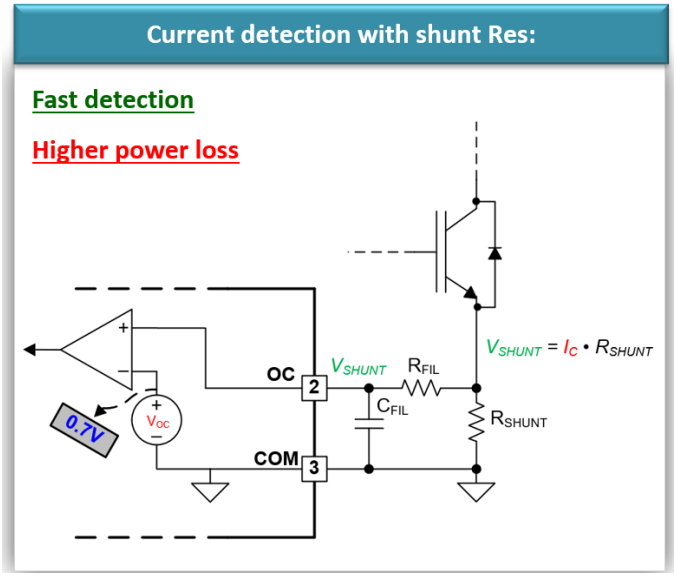

Figure 4-2. Shunt Resistor Implementation Circuit

In Figure 4-2, the current detection implementation approach is shown with an R_{shunt} resistor. The R_{shunt} is added in the high current path, the voltage across the resistor is measured using the RC filter by the OC detection pin. When the voltage across the resistor is higher than the OC detection threshold, the gate driver triggers a fault event and turns off the gate driver output to protect the system.

This implementation approach is very simple and fast. However, as the resistor is in the high current path, this method causes high-power loss. Due to that, this approach is not recommended for systems with high operating current, to minimize the power loss.

Option2: R_{sense} resistor-based approach:

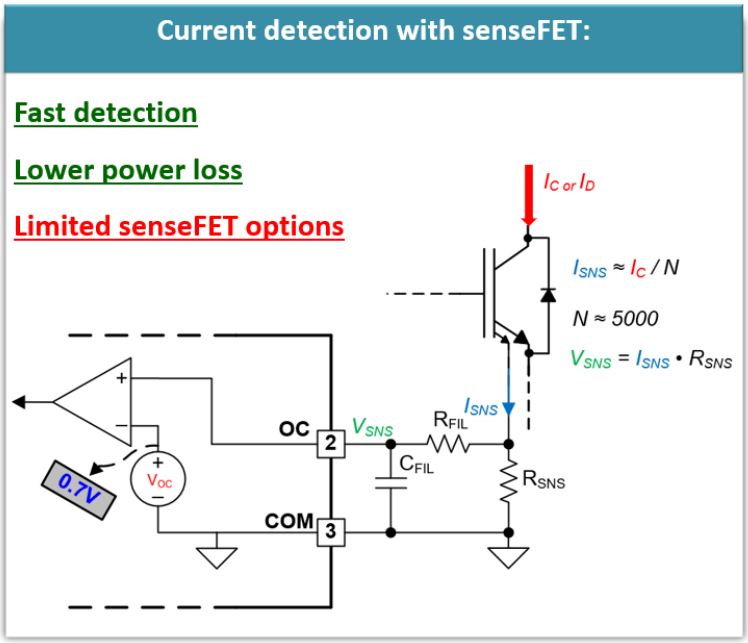

Figure 4-3. R_{sense} Resistor Implementation Circuit

This approach is similar to the R_{shunt}-based approach. However, in the case of the R_{sense}-based approach, the sense resistor is added in the sense path, not on the high current path. Some power modules have a separate terminal that has around 5000x lower current sense path apart from the high current path. The sense resistor is added in the lower current sense path and hence the power loss is minimal. This approach is faster and has lower power loss as well. However, it can be implemented only with the power modules with the sense option.

4.2 Short Circuit Voltage-Based Protection Implementation

Short-circuit voltage-based protection is typically done using the DESAT function in a gate driver. OC-detection approach is also sometimes used for voltage-based protection. So the two options are:

- V_{SC} voltage detection across FET using DESAT pin
- V_{SC} voltage detection across FET using OC pin

Option1: V_{SC} voltage detection across FET using DESAT pin:

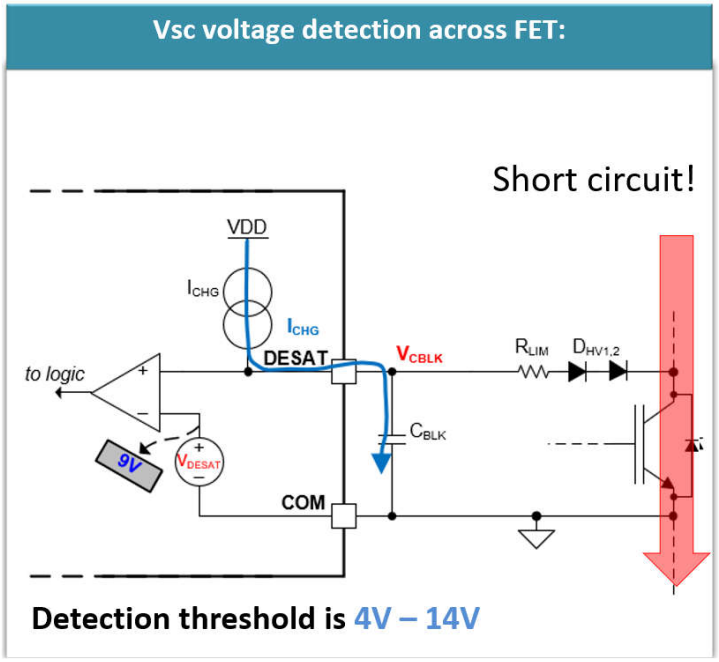

Figure 4-4. DESAT Circuit Implementation for V_{SC} Voltage Detection

The typical voltage detection approach across the power module is using the DESAT node as shown in Figure 4-4. The high voltage drain node is connected through 1 or 2 high voltage diodes and a current limiting resistor (R_{LIM}) to the DESAT pin. A blanking capacitor (C_{BLK}) is connected in the DESAT pin as well. DESAT node has an internal current source, internally connected to the VDD bias (secondary isolated bias). When INP is high, the internal current source will supply the (I_{CHG}) current through the DESAT pin. The current source path is not active when INP is low.

During normal operation, the voltage across the power module is low, hence the high-voltage diodes ($D_{HV\ 1,\ 2}$) are forward biased and the current flows through the diode and power module. However, during short-circuit events, the voltage across the power module is high, which causes the $D_{HV1,\ 2}$ to be reverse biased; hence the DESAT current path is disconnected. So, the I_{CHG} charges the C_{BLK} capacitor. When the voltage on the DESAT pin exceeds the detection threshold, it triggers the DESAT fault and turns the gate driver output off to protect the system. The turn-off operation is discussed in a separate section as the turn off operation needs special consideration due to high di/dt involved during the SC/OC event.

The gate driver's internal current source is typically around 500µA-2mA. To enable faster protection, an external current source path can be planned by connecting the DESAT node to VDD/OUTH with a resistor. The same concept can be used for OC pin as well.

Option2: V_{SC} voltage detection across FET using OC pin

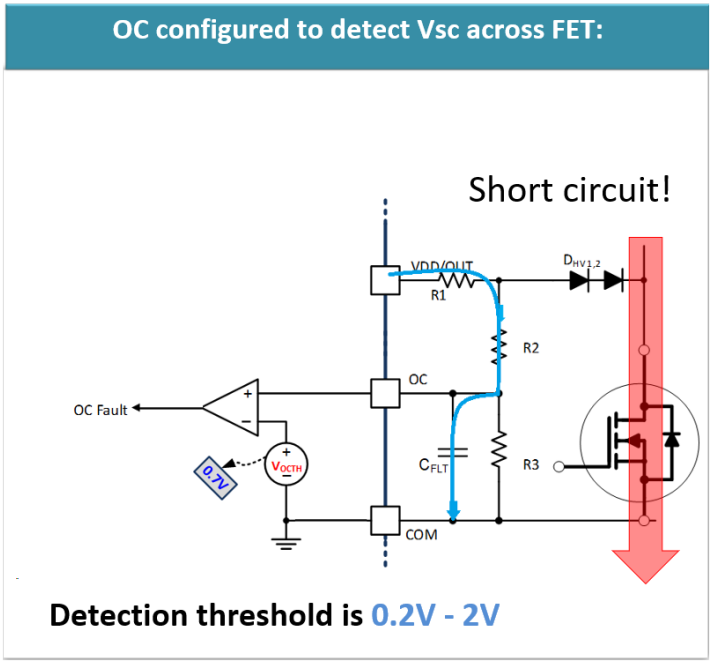

Figure 4-5. OC Pin Circuit Implementation for V_{SC} Voltage Detection

OC pin is typically used to sense current as explained in the current-based protection section. However, the OC pin can be used for V_{SC}-based voltage detection as well by planning the current source from VDD/OUT as shown in Figure 4-5. Similar to the DESAT concept, during normal operation, the VDD/OUT charge current path is through the power module, and during the OC/SC event, the current path is through the C_{FLT} capacitor and triggers the OC event.

V_{SC}- and I_{SC}-based protection approaches explained using the DESAT or OC pin. The I_{SC}-based protection approach is faster, however, causes increased power loss in the case of the R_{shunt} approach or needed power module with sense pin for the R_{sense} approach. Due to these reasons, it is very common practice to use DESAT-based approach for both of the SiC and IGBT modules. In this application note, data has been collected based on the V_{SC} approach for both DESAT and OC pin.

5 DESAT Circuitry Design

5.1 DESAT Circuit Component Selection

To achieve proper short circuit and overcurrent detection, it is crucial to choose the right components for the DESAT circuitry. The DESAT circuitry usually includes a blanking capacitor (C_{BLK}), a current-limiting resistor (R_{LIM}), and high-voltage diode(s) ($D_{HV(1,2..)}$). Depending on system conditions, usually protection diodes (D_{D1}, D_{D2}) and a zener diode in the DESAT path (D_Z) are also used.

During normal operation of the power switch, the V_{DS} or V_{CE} is lower than the desired V_{DS}/V_{CE} threshold. Under this condition, the high-voltage diodes are forward biased, and the DESAT pin internal charging current (I_{CHG}) flows through the high-voltage diodes into the collector or drain of the power switch. Thus, voltage on the DESAT pin is lower than the DESAT detection threshold, and DESAT is not triggered.

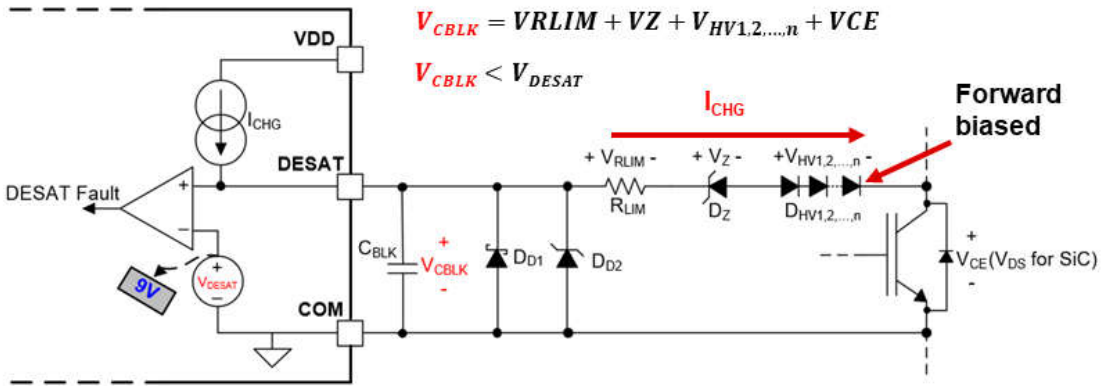

Figure 5-1. DESAT Normal Operation

During a short-circuit or overcurrent event, the V_{DS} or V_{CE} is higher than the desired V_{DS}/V_{CE} threshold. Under this condition, the high-voltage diodes become reverse biased, and the DESAT pin internal charging current cannot flow through the diodes. As a result, I_{CHG} starts charging the blanking capacitor, causing the voltage on the DESAT pin to rapidly rise up to above the DESAT detection threshold. After a deglitch period, DESAT is triggered in this case.

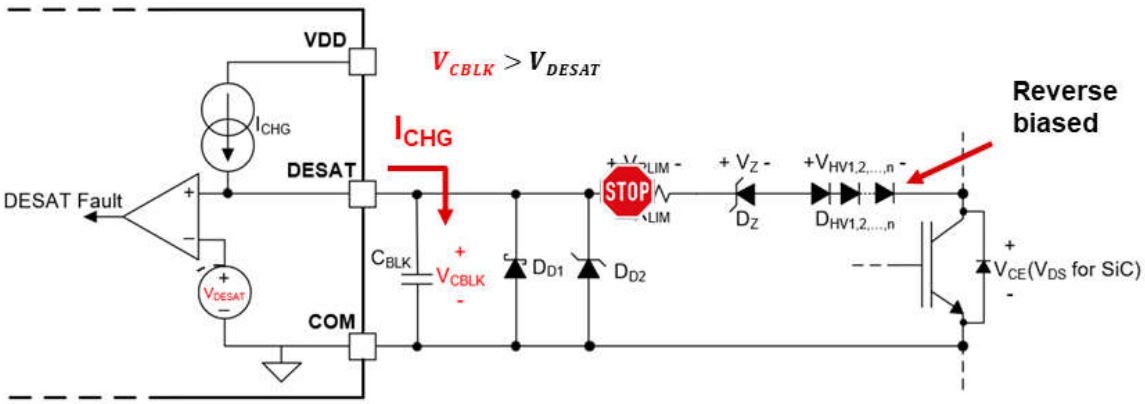

Figure 5-2. DESAT Short-Circuit Operation

To correctly select the external circuitry values, first determine the V_{DS}/V_{CE} threshold above, which the system is considered short-circuited or overcurrent. Then, design the external circuitry values using Equation 1:

During normal operation:

$$V_{CBLK} = \left(V_{RLIM} + V_Z + V_{HV\ 1,2,\ldots n} + V_{CE}\ \text{or}\ V_{DS}\right) < V_{DESAT} \quad (1)$$

During short-circuit or overcurrent operation:

$$V_{CE} \text{ or } V_{DS} > V_{DESAT} - (V_{RLIM} + V_Z + V_{HV\,1,2,\ldots n}) \quad (2)$$

Besides the voltage detection threshold, also pay attention to the blanking capacitor charging time (t_{BLK}), since it contributes to the total DESAT detection and shutdown time. t_{BLK} can be estimated using Equation 3:

$$t_{BLK} = \frac{C_{BLK} \times V_{DESAT}}{I_{CHG}} \quad (3)$$

Where Cblk is the size of the blanking capacitor, V_{desat} is the DESAT detection threshold, and I_{CHG} is the DESAT charging current.

After taking all elements into consideration, the total DESAT detection time can be calculated by using Equation 4:

$$t_{total\_detection} = t_{DESATLEB} + t_{BLK} + t_{DESATFIL} \quad (4)$$

Where $t_{DESATLEB}$ is the leading edge blanking time, t_{BLK} is the blanking capacitor charging time, and $t_{DESATFIL}$ is the DESAT filter time.

5.2 Effect of Parasitic Elements

Besides the values of DESAT external circuitry (capacitance, resistance, forward voltage drop, and so forth), it is also important to pay attention to the parasitics introduced by the external circuitry and the effects. Two parasitic elements that can affect DESAT detection time are discussed here: the junction capacitance of the high-voltage diode and the parasitic capacitance on the DESAT node.

The junction capacitance of the high-voltage diode can affect DESAT detection time, because it can couple dV/dt from the drain/collector and causing current flow. When there is a negative dV/dt on the drain/collector, current is pulled from the DESAT pin; when there is a positive dV/dt on the drain/collector, current is injected into the DESAT pin. The delta current can either increase or decrease DESAT detection time.Figure 5-3 shows how larger high-voltage diode junction capacitance can result in larger DESAT pin voltage dip, resulting in longer blanking capacitor charging time.

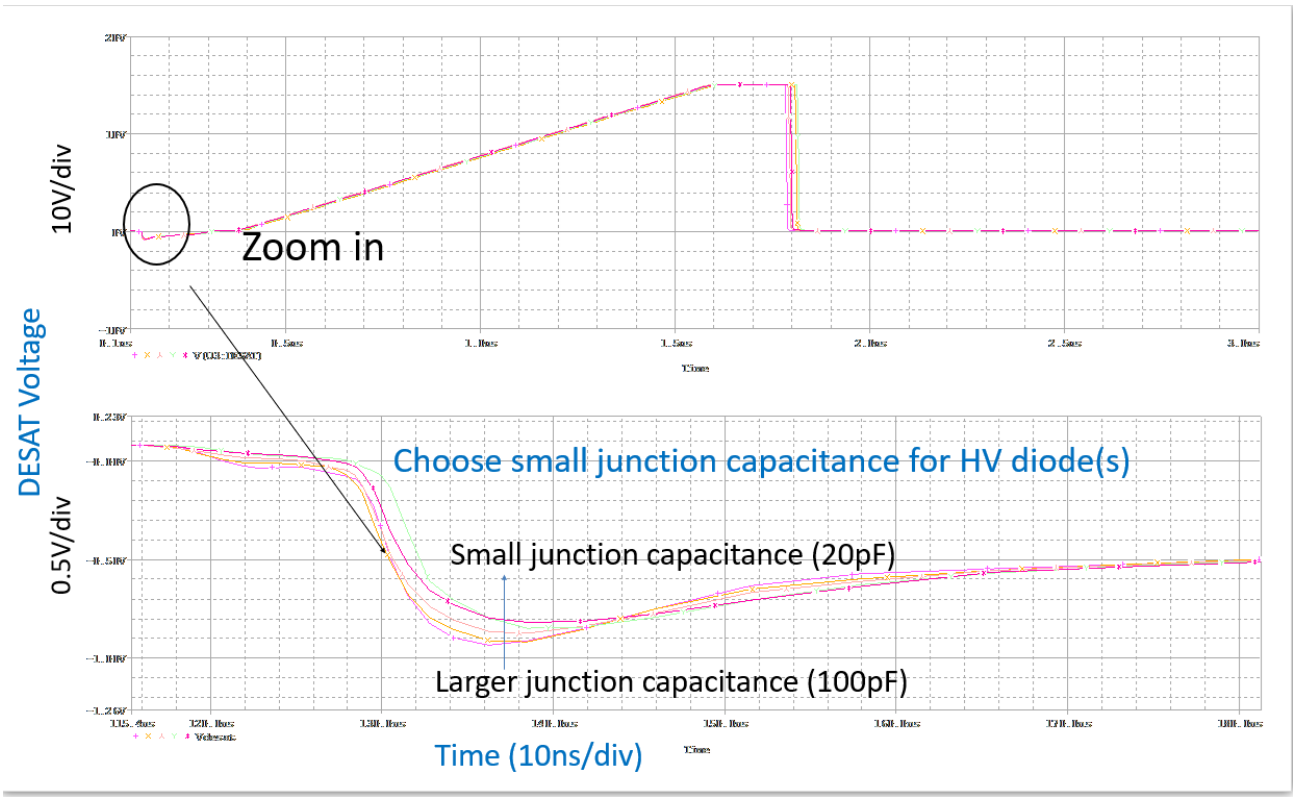

Figure 5-3. Junction Capacitance Simulation Result

Additional parasitic capacitance on the DESAT node can also affect DESAT detection time. These parasitic capacitance can come from either the clamping diodes on DESAT (Schottky diode and/or Zener diode) or the PCB trace capacitance. The clamping diode's junction capacitance is usually around 5pF, while the PCB trace parasitic capacitance varies by the system, usually in the 5pF-20pF range. Take the extra capacitance value into consideration when calculating DESAT blanking capacitor charge time.

5.3 Effect of Rlim on DESAT Noise

The current-limiting resistor in the DESAT circuitry serves two purposes: it can help to adjust the DESAT detection threshold, and it can also help to limit the current injected into DESAT node or drawn out of DESAT node when dV/dt from the drain/collector causes a current flow. Figure 5-4 shows how a smaller current-limiting resistor value can result in larger DESAT pin voltage dip, resulting in longer blanking capacitor charging time. TI recommends selecting a current-limiting resistor of 1kOhm or above to improve DESAT detection robustness.

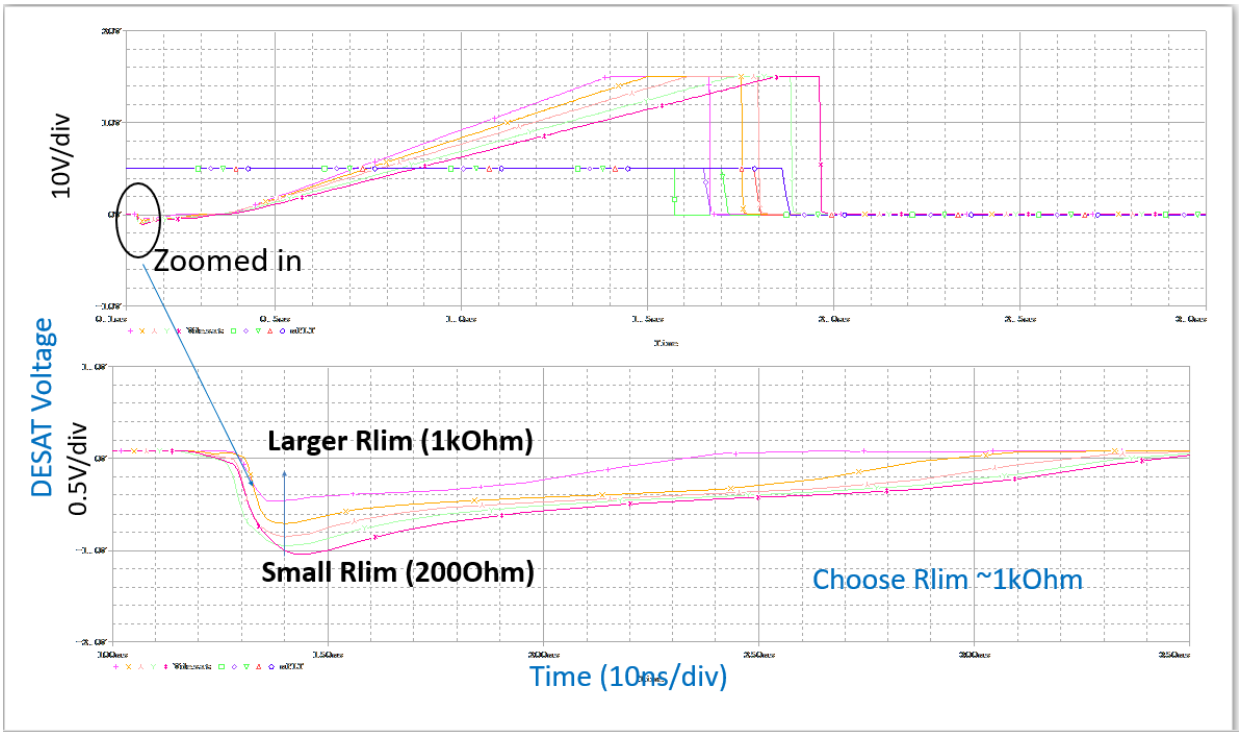

Figure 5-4. Rlimit Resistor Simulation Result

6 Safe Shutdown

6.1 Safe Shutdown Mechanisms

After detecting the short-circuit or overcurrent event with either voltage-based or current-based detection methods, the power switch needs to be shut down safely and efficiently to prevent power switch damage and system failure.

If the switch is turned off quickly with a high sink current (several or tens of amps), there will be a very large, negative di/dt through the switch. This di/dt, coupling with the parasitic inductances in the power loop, can cause the voltage across the switch to rise up. This V_{CE}/V_{DS} overshoot can be hundreds of volts, and has the potential to overvoltage the power switch and cause power switch failure.

Thus, after detecting short circuit or overcurrent, it is preferable to use either soft turn-off (STO) or two-level turn-off (2LTO) to turn off the power switch. During soft turn-off, shown in Figure 6-1, a smaller, constant sink current is used to switch off the device. The turn-off time is increased, turn-off speed is reduced, and the gate is slowly discharged. During two-level turn-off, shown in Figure 6-2, the gate is first pulled down to a mid-voltage level and stays for a fixed amount of time. After the fixed time expires, the driver continues to pull down the gate voltage with a smaller, constant sink current. Both of these methods can reduce the turn-off speed, reduce the di/dt, and reduce V_{CE}/V_{DS} overshoot to protect the device.

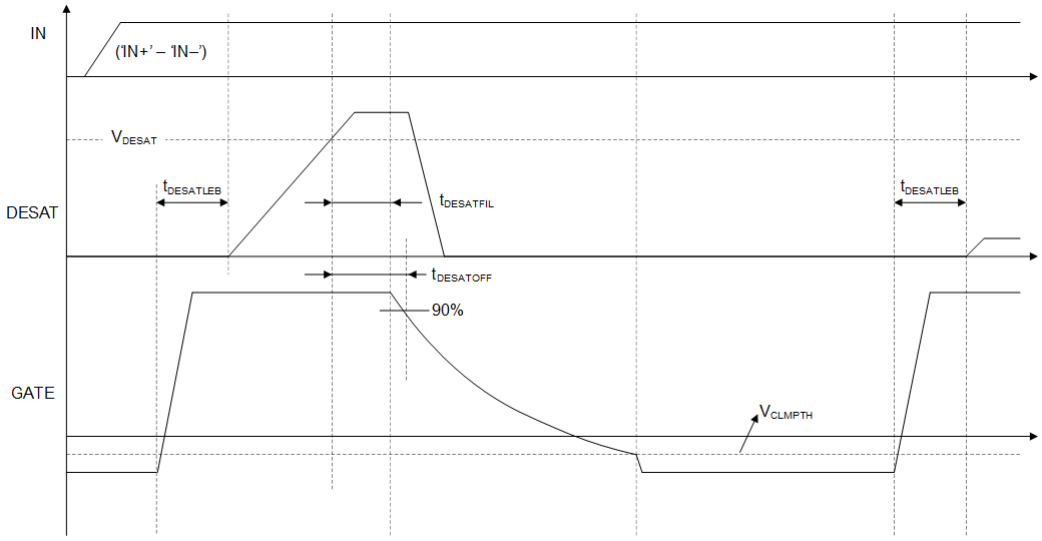

Figure 6-1. Soft Turn-Off

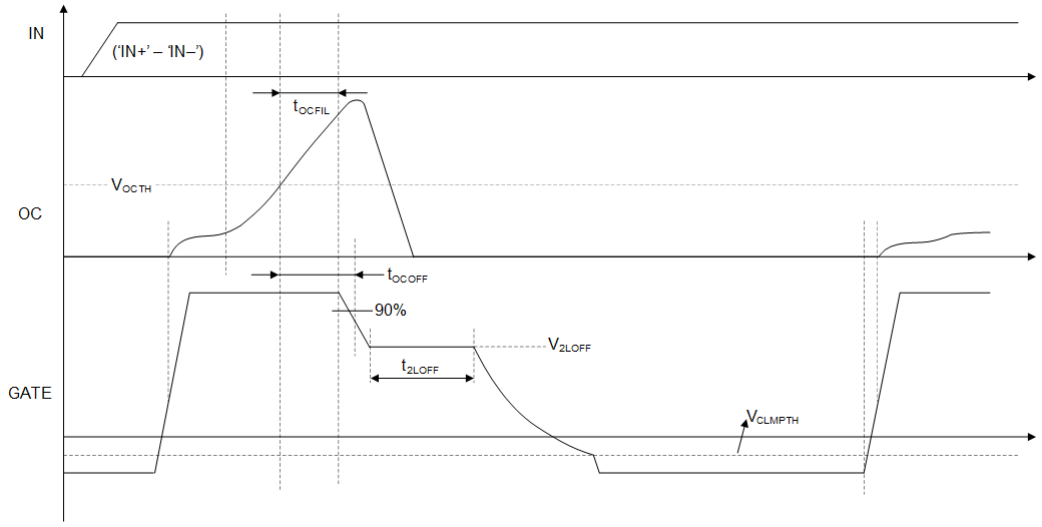

Figure 6-2. Two-Level Turn-Off

6.2 Safe Shutdown Considerations

When safe shutdown is implemented, the power loop parasitic inductance plays a large role in the V_{CE}/V_{DS} overshoot profile and the shutdown time. Larger power loop parasitic inductance would increase the V_{CE}/V_{DS} overshoot with the same power switch di/dt, which is also why STO/2LTO are more desirable under this condition. Also, shutdown time can be reduced if parasitic inductance in the power loop is reduced. This includes power module stray inductance.

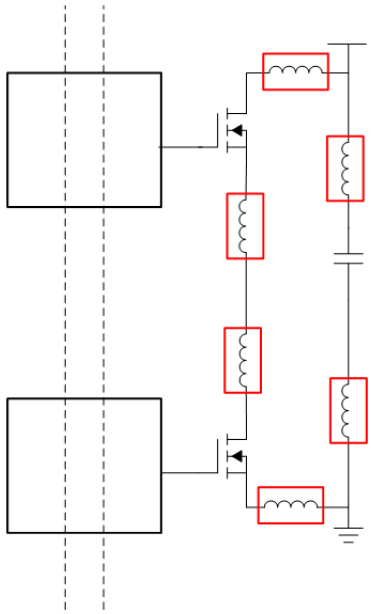

Figure 6-3. Power Loop Inductance

7 Short-Circuit Test Setup and Data

7.1 Short-Circuit Bench Measurement Setup

To exercise short-circuit event, a half-bridge gate driver board UCC21710QDWEVM-054 is used. This half-bridge board is capable of doing double pulse or SC testing. To exercise SC, the high side driver input is permanently set to high and the low side gate driver is turned on while the high sides switch is on.

High voltage power supply + bulk capacitance used as HV source. The schematic representation of the SC testing is shown in Figure 7-1.

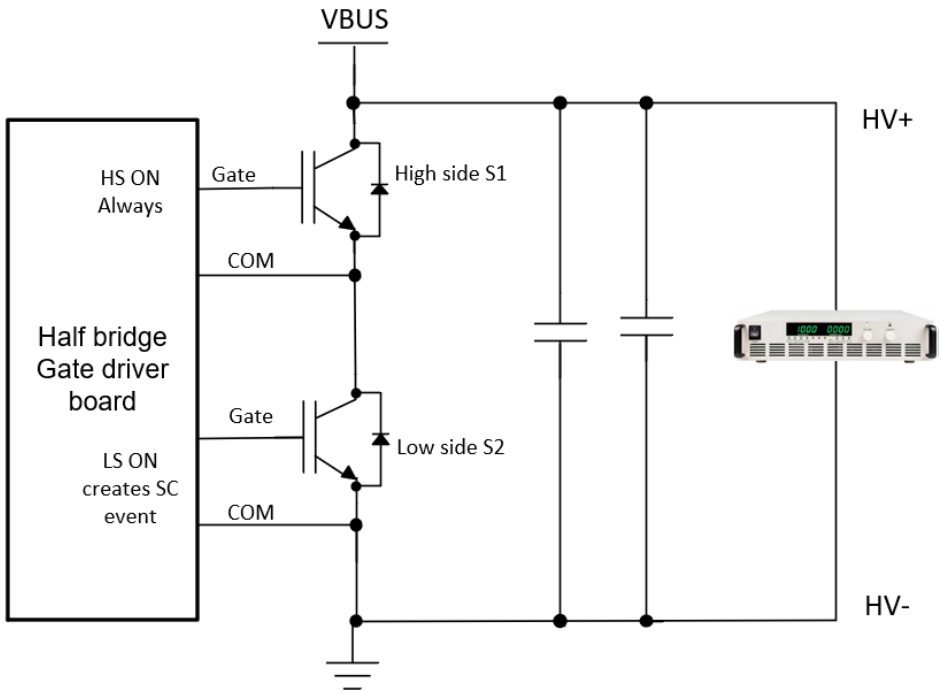

Figure 7-1. Half Bridge SC Schematic Representation

IGBT (FF800R12KE7) and SiC (CAB450M12XM3) power modules are used to collect data for the SC event. V_{SC}-based protection approach used to capture SC event for both DESAT and OC capable gate drivers.

The power modules key parameters are shown in Table 7-1.

Table 7-1. Power Modules Key Parameters

	SiC CAB450M12XM3	**IGBT FF800R12KE7**
V_{CE}/V_{DS} (V) I_C/I_D (A)	1200V 450A	1200V 800A
Qg	1330 nC (Vds=800V)	12.8 uC (Vcc=600V) **(10x)**
Cies / Ciss, Cres/ Crss	38 nF, 90 pF	122 nF **(3x),** 0.6 nF **(6x)**

7.2 SC Board Setup for Data Collection

The following lab setup is used to collect data for both DESAT and OC-based implementation for both IGBT and SiC power modules, as shown in Figure 7-2.

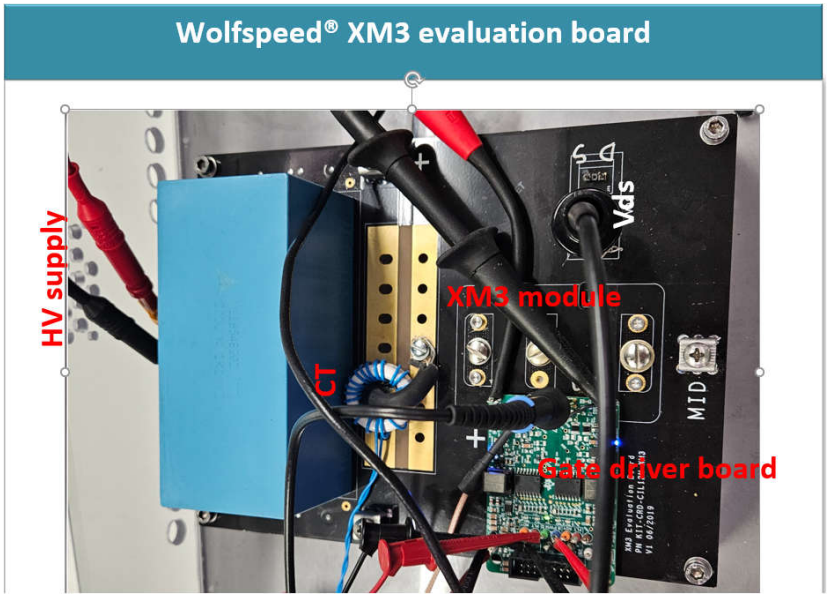

Figure 7-2. XM3® Evaluation Board With Half Bridge Driver EVM Connected

The **HVP054 EVM** directly plugs into the XM3® evaluation board from Wolfspeed® as shown in Figure 7-2 to exercise SC event for the SiC power module.

BM3® evaluation board was used to test for the IGBT power module SC event. As the gate driver board is not compatible with the power module evaluation board, an interface board is used to convert the EVM to be compatible with the 62mm power module connection as shown in Figure 7-3.

Figure 7-3. Interface Board to Connect Gate Driver EVM to BM3 Power Module

7.3 Different Circuit Configurations for SC Testing

Two different DESAT circuit implementations and “OC as DESAT” circuit implementation are used with two different turn-off approaches to compare the SC performance for IGBT and SiC power modules.

- **Circuit Implementation for DESAT without external charge:**
  - **Charge current:** 0.5mA typical
  - **DESAT detection Threshold:** 9V
  - **Capacitor updated to 50pF**

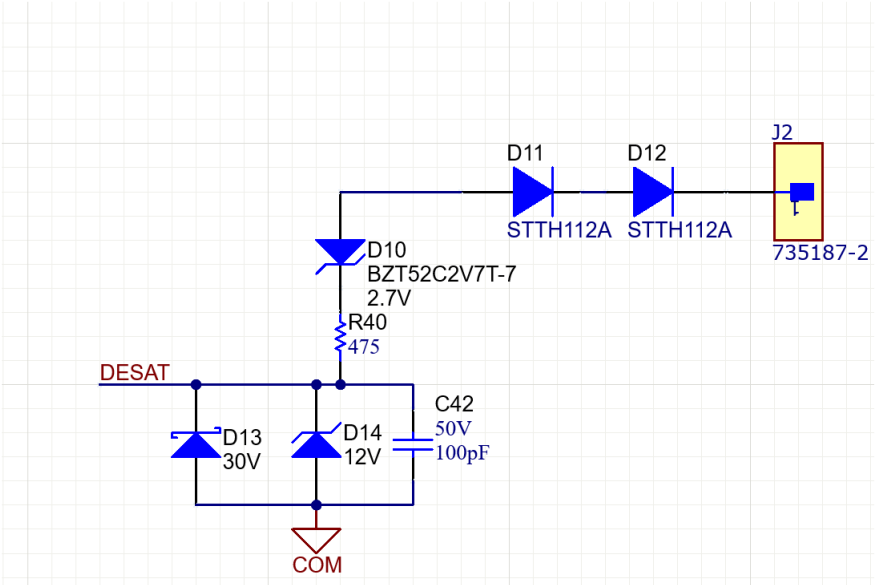

Figure 7-4. DESAT Without External Charge Implementation

- **Circuit Implementation for DESAT with external charge from OUTH:**
  - **Charge current:** 0.5mA +10mA typical
  - **DESAT detection Threshold**: 9V
  - **Capacitor updated** to 50pF

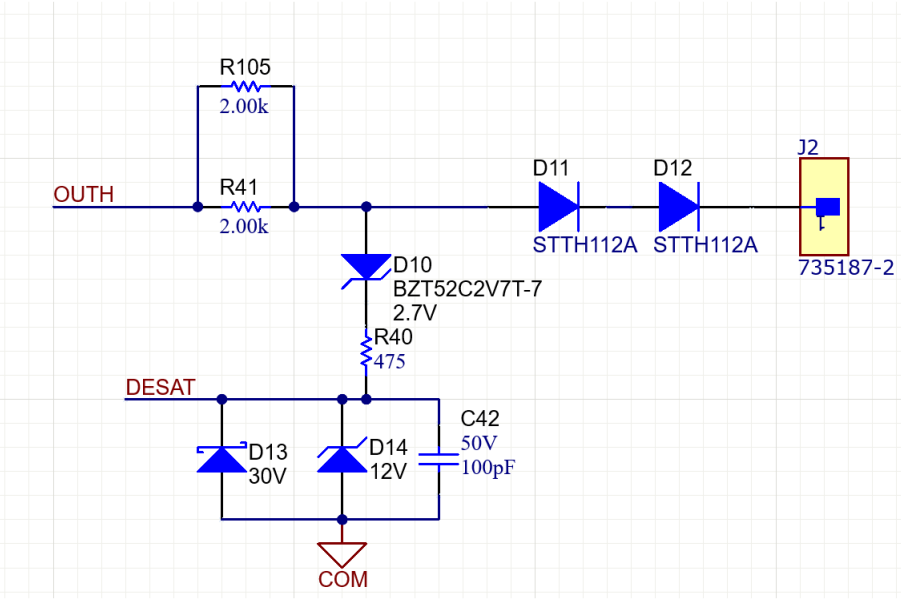

Figure 7-5. DESAT With External Charge Implementation

- **Circuit Implementation for OC as DESAT with external charge from OUTH:**
  - **Charge current:** <10mA Typical
  - **OC detection Threshold:** 0.7V
  - **Capacitor updated to 50pF**

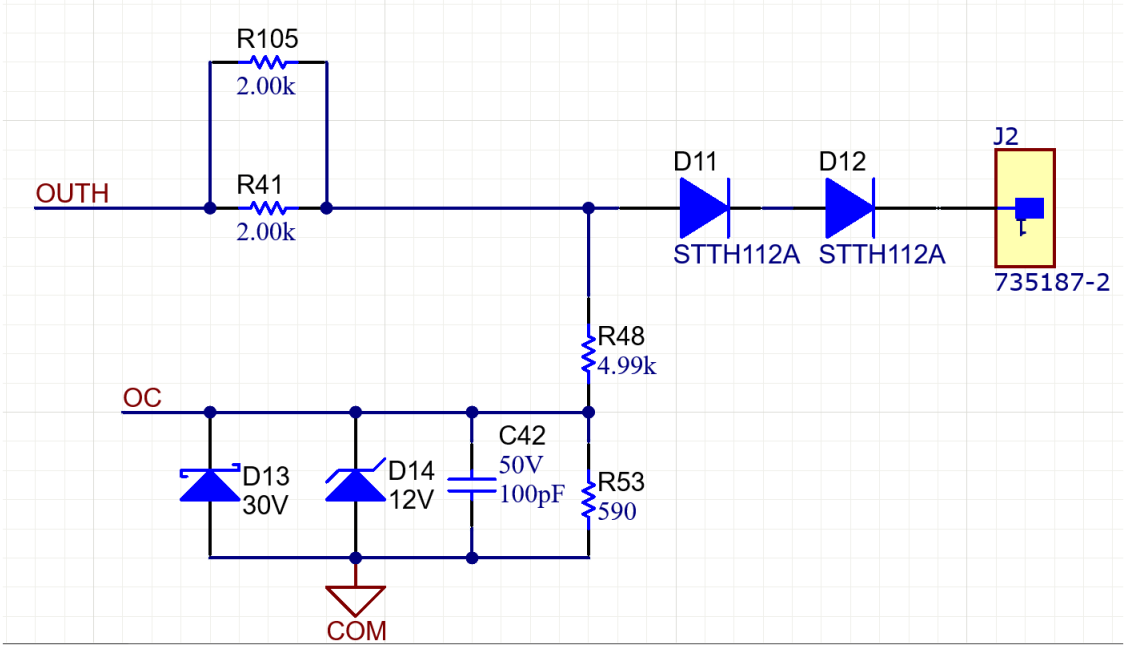

Figure 7-6. OC as DESAT Implementation

7.4 Bench Measurement Results

There are four different SC tests conducted with different detection approaches. 9V DESAT threshold gate driver UCC21750-Q1 is used to capture SC data for both without external charge current and with external charge current. Also, 0.7V OC threshold gate drivers UCC21710-Q1 and UCC21732-Q1 are used to capture SC data for STO and 2LTO, different turn-off approaches.

- **Case1:** 9V DESAT without external charge current, with STO
- **Case2:** 9V DESAT with external charge current, with STO
- **Case3:** 0.7V OC threshold, with STO
- **case4:** 0.7V OC threshold, with 2LTO

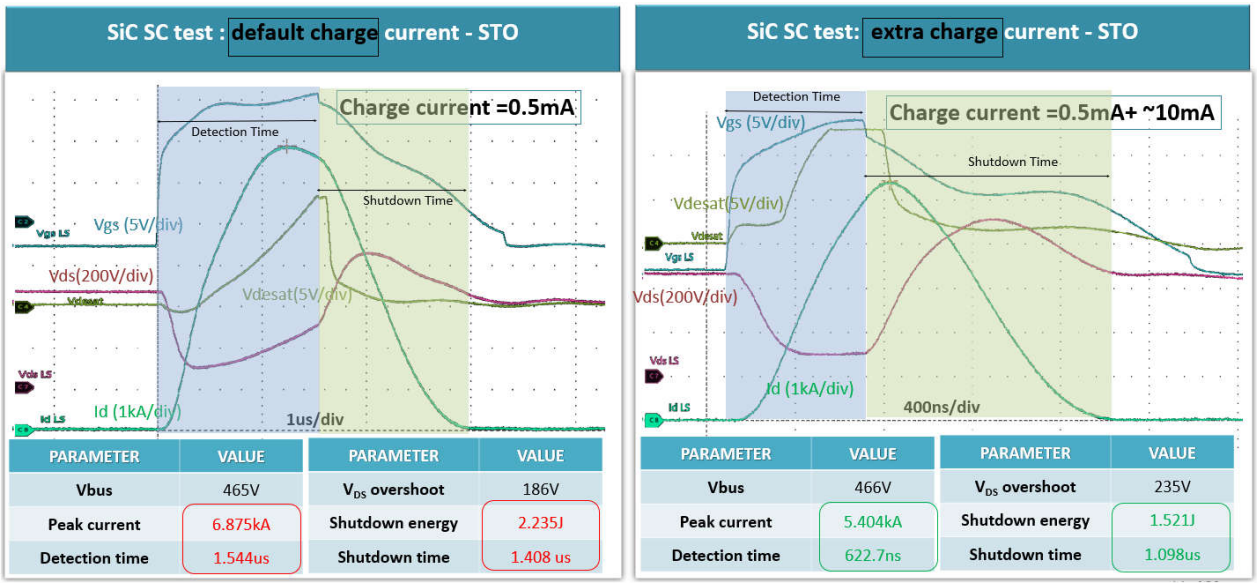

Figure 7-7. Case1 and Case2 SiC SC Event Screen Captures

As shown in Figure 7-7, with a default charge current of 0.5mA, the detection time, peak SC current, shutdown energy, and shutdown time are all high compared to external charge circuitry to enable faster detection.

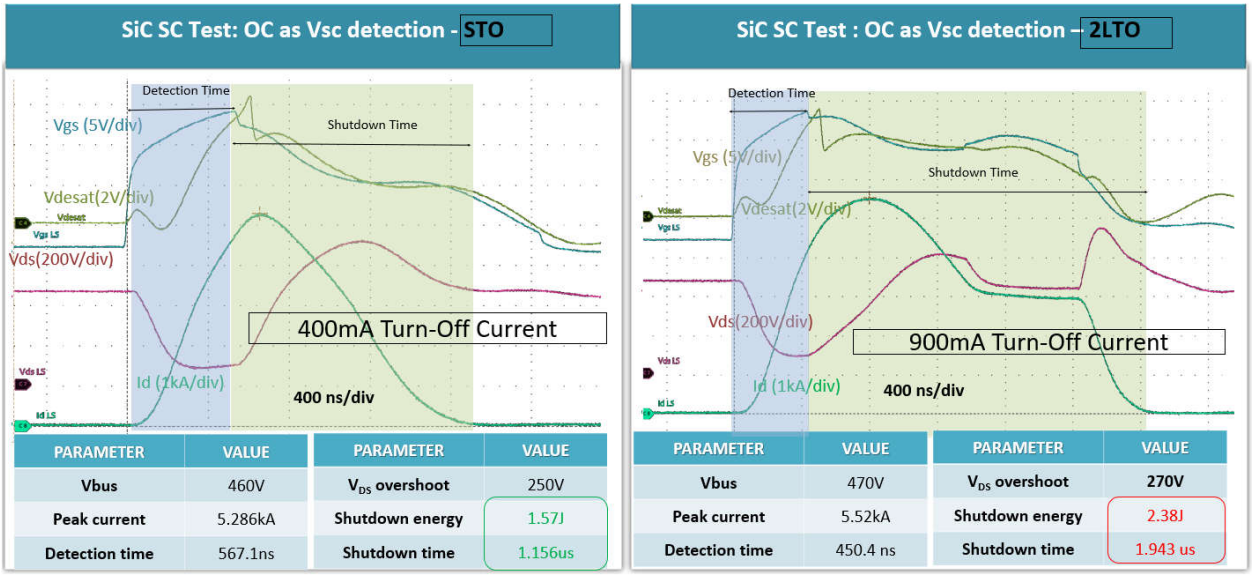

Figure 7-8. Case3 and Case4 SiC SC Event Screen Captures

As shown in Figure 7-8, the “OC as DESAT” peak current and detection time (Case3 and 4) are comparable to the “DESAT” detection time with external charge current (Case2).

In case of shutdown energy, 400mA STO performance Case3 matched Case2, however, 2LTO performance of Case4 showed higher shutdown energy and shutdown time as the Gate was held approximately 9V for approximately 1µsec and the peak current did not reduce and kept It the same. This is because the gate holding voltage of 9V threshold is keeping the SiC module conducting and the peak current was not reduced. If the power module “turn on threshold” is just below 9V, then it would reduce the SC current and the 2LTO would be effective in such case only.

The four cases shown above are repeated for IGBT power module as well.

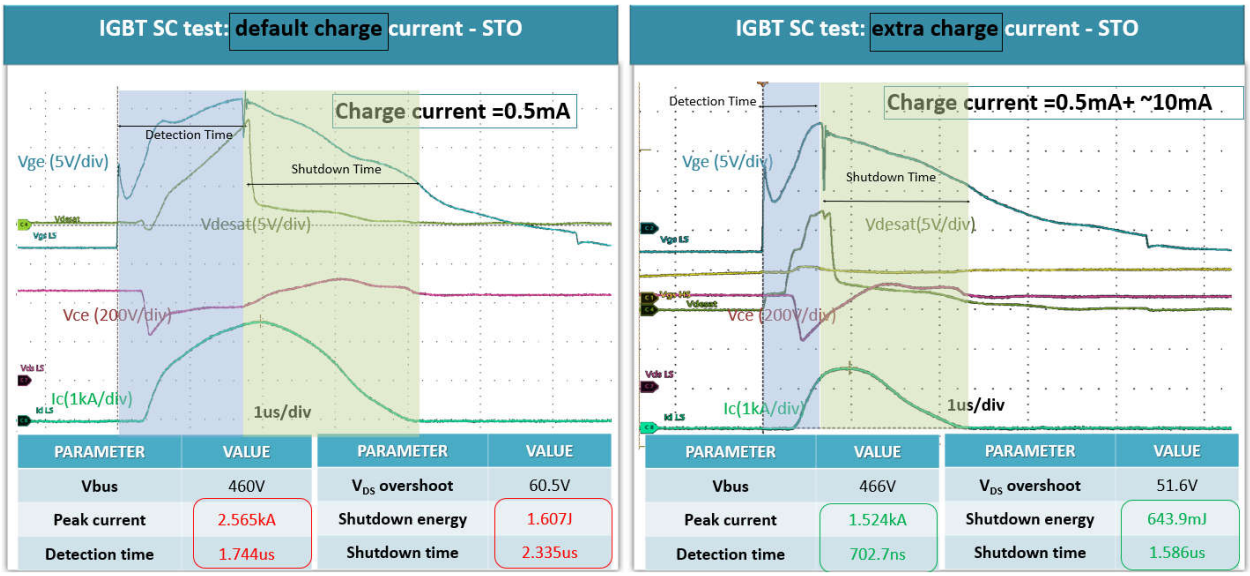

Figure 7-9. Case1 and Case2 IGBT SC Event Screen Captures

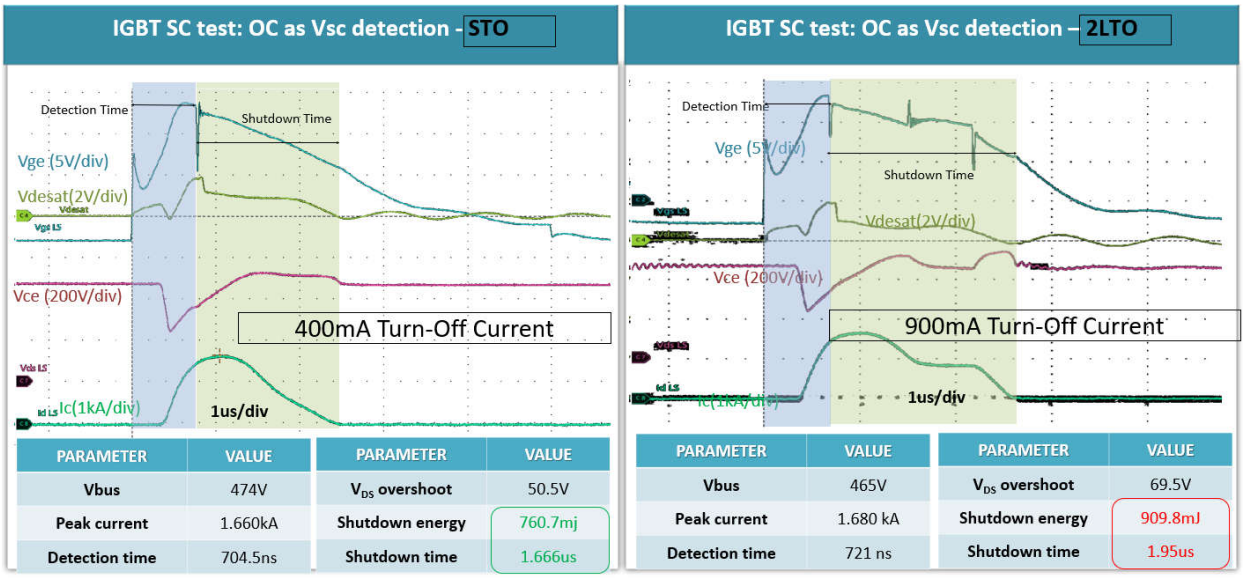

Figure 7-10. Case3 and Case4 IGBT SC Event Screen Captures

The performance of the IGBT was comparable to SiC power module in terms of how DESAT/OC circuit behavior.

However, as the overall peak current observed in the IGBT module was much lower compared to SiC. Because of this, the shutdown energy and shutdown time are all much lower for IGBT module.

7.5 Overall Summary of SiC vs IGBT Power Module SC Observation

SiC	IGBT
SC current increases **~66ns** after gate on (As SiC has lower gate threshold and lower gate capacitance)	SC current increases **~350ns** after gate on (As IGBT has higher gate threshold and higher gate capacitance)
Peak current **6.87kA** (at ~1.5µs delay)	Peak current **2.565kA** (at ~1.7µs delay)
Ideal to detect + initiate gate turn-off within < 1µs	Ideal to detect + initiate gate turn-off within < 2µs
Faster turn off is needed, however balance between overshoot and turn off time	As IGBT can withstand SC current little longer, prioritize in reducing the overshoot

8 Key Consideration in Designing SC Protection Circuit

- **Reduce peak short circuit current**
  - Peak current depends on multiple factors: time to detect the SC event, module type, and the system voltage. As the module type and system voltage are fixed, the only way to optimize is to implement a faster detection circuit to identify the failure event faster.

Some of the key considerations to detect the failure faster:

- Optimum smaller blanking capacitor ~30-100pF (balance between false triggering to right protection)
- Higher blanking cap charge current (0.5mA-2mA)
- Optimum low V_{SC} detection threshold based on the power module
- **Reduce shutdown time and energy**
  - Reducing shutdown energy depends on the peak current during the SC event and turn-off di/dt. Reducing peak current was explained in the previous passage and the only other parameter to tweak is turn-off di/dt. Though faster turn-off will help to reduce the shutdown time, it is not recommended due to possible overshoot across the power module due to very high di/dt during the SC event. So it is ideal to balance the turn-off di/dt and overshoot specific to the power module.
    - Faster turn-off (higher overshoot, but less shutdown energy), slower turn-off (lower overshoot, but higher shutdown energy)
    - Need to balance between overshoot vs shutdown energy

Table 8-1. TI Isolated Gate Drivers Selection for SiC and IGBT Power Module Protection

	IGBT	SiC
Smart Isolated Gate Driver UCC217xx family (ICHG = 0.5mA)		
Desaturation protection	(9V threshold) UCC21750 **(STO-400mA)**	(5V threshold) UCC21755 **(STO-400mA)** UCC21756 **(STO-900mA)**
OC protection	(0.7V threshold) UCC21710, UCC21737 **(STO- 400mA)**	
	(0.7V threshold) UCC21732 **(2LTO – 900mA)**	
Programmable Isolated Gate Driver – UCC588x (ICHG=0.5-2mA)		
Desaturation protection	4-14V threshold	
OC/SC protection	0.25V – 2V threshold	
STO /2STO current	300mA -1200mA	

9 Summary

The following topics are discussed in this application note: different OC/SC protection approaches, the protection circuit working principle, key considerations in designing the protection circuit, bench measurement setup, SC data, and the gate driver selection guide for IGBT and SiC power module.

10 References

“Failure modes and mechanism analysis of SiC MOSFET under short-circuit conditions” by Xi Jiang, Jun Wang, Jiwu Lu, Jianjun Chen, Xin Yang, Zongjian Li, Chunming Tu, Z. John Shen

“IGBT Failure mechanism and boundary analysis under large current and high temperature turn-off” by Xiao Ma, Yongle Huang and Yifei Luo

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