Technical White Paper

Optimizing a Synchronous Rectification Scheme in CLLLC

ABSTRACT

This paper analyzes the problem with a synchronous rectification scheme, that is, when the secondary rectifier switch and the primary active switch are turned on at the same time, the problem of turning on rectifier switch in advance occurs when the switching frequency is greater than the resonant frequency.

This paper proposes that the formula for time domain analysis can be used to calculate the delay of the turn-on time of the rectifier switch relative to the turn-on time of the switch in primary side, so as to confirm the normal opening of the rectifier switch.

Table of Contents

Trademarks

1 Background

In energy storage systems (ESS), bidirectional isolated DC/DC is usually used to charge and discharge batteries.

Among the different isolated bidirectional DC/DC topologies, LLC resonant converters can easily implement soft switching over the full-load range, offering significant advantages in high-efficiency applications. The CLLLC topology is the basis of the LLC topology, which adds a resonant tank on the secondary side to enable symmetric gain in both forward and reverse mode.

In traditional bidirectional CLLLC resonant converters, as shown in Figure 1-1, the body diodes of the MOSFET form an uncontrolled rectification network. Compared to fast recovery diodes, body diodes can seriously reduce efficiency due to the larger reverse recovery current, longer reverse recovery time, higher voltage drop, and lower rated on-current.

The most effective way to solve this problem is to use synchronous rectification (SR) technology. By replacing the body diode with a MOSFET in a rectified network, the current now flows through the MOSFET channel. The MOSFET has a small on-resistance which effectively reduces rectified conduction losses.

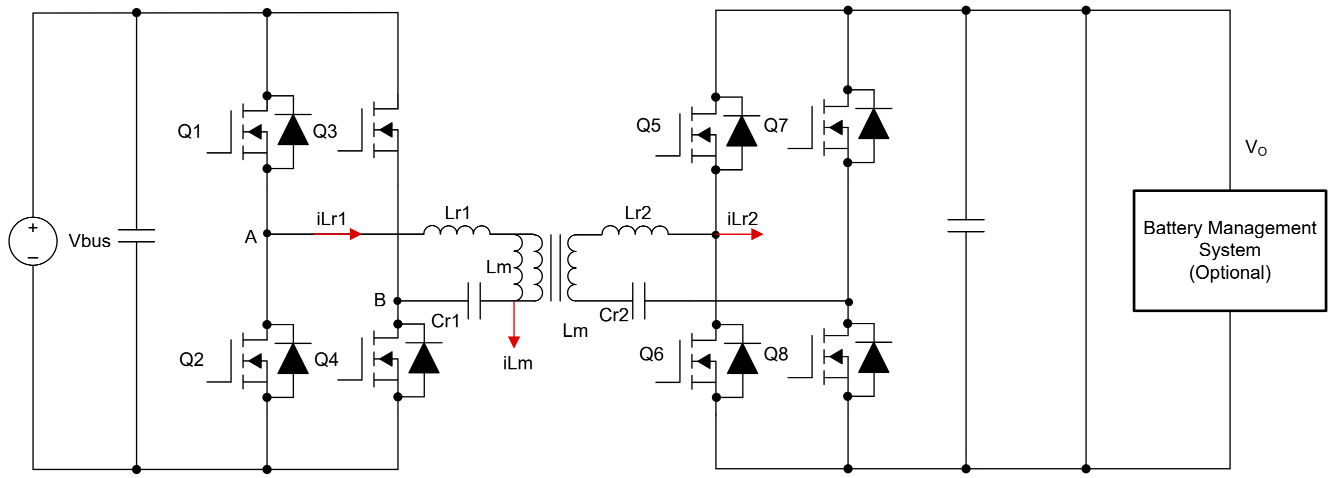

Figure 1-1. CLLLC Topology in ESS

Traditional synchronous rectification strategies can be divided into the following categories:

1. *Current type.* Current sensors use current type to obtain a voltage in phase with the rectifier current as the synchronous rectification driving signal. The current-type synchronous rectification strategy can be used in most topologies and is simple to implement, but requires one or more current sensors, increasing the cost and volume.
2. *Voltage type.* By detecting the drain-source voltage of the rectifier switch tube as a reference signal for synchronous rectification drive switches, this strategy has been applied to many commercial synchronous rectification chips, such as UCC24624. The voltage-based synchronous rectification strategy does not require an additional current sensor, but the detection of the drain-source voltage signal is affected by the parasitic inductance of the switch package and the inductance on the sensing path.

2 Problems with a Synchronous Rectification Strategy

To reduce the number of sensors, a synchronous rectification strategy based on secondary-side current sampling combined with a primary-side drive signal is proposed. Taking the forward operation of the CLLLC resonant converter as an example, assume that the converter operates in boost mode ($f_s < f_r$), as shown in Figure 2-1.

The synchronous rectifier switches Q_5 and Q_8 are turned on at the same time as Q_2 and Q_3, and the switch turns off when i_{Lr2} is detected at 0. While these actions are not a problem in this mode as shown, problems can occur if the converter works in over-resonant mode ($f_s > f_r$).

As shown in the top-right graph of Figure 2-2, in the dead time from t_1 to t_3, $i_{Lr1} = i_{Lm}$ at the t_2 moment, causing the secondary current to begin to commutate, and the t_3 moment Q_2/Q_3 is now on. At this time there is no problem with turning on the secondary-side rectifier switch, but such situations do exist, as shown in the bottom-right graph of Figure 2-2. The dead time is relatively short, as until the end of the dead zone, i_{Lr1} is still greater than i_{Lm}. At this time Q_2/Q_3 is turned on (t_2), and i_{Lr1} is still higher than i_{Lm} until equal to i_{Lm} (t3). At this time, the secondary side begins to commutate if the original logic is still used. When the synchronous rectifier switch is turned on together with Q_2/Q_3, the switch is turned on in advance, causing the current waveform to oscillate.

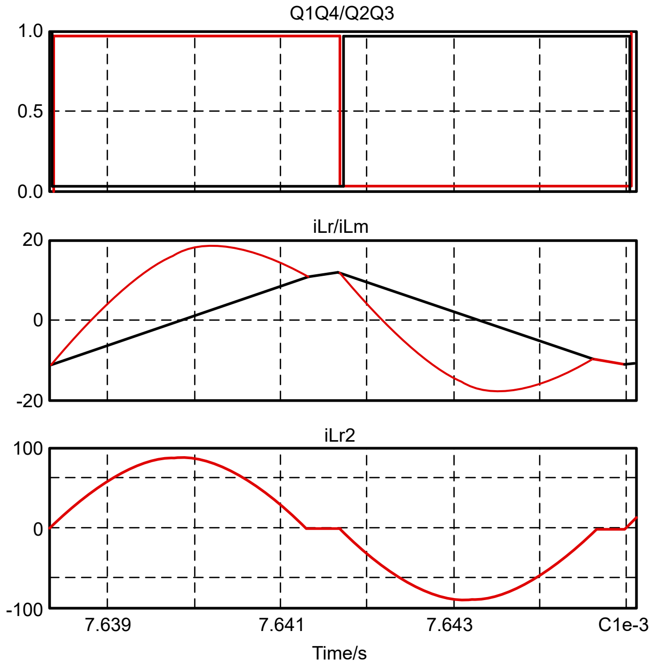

Figure 2-1. Current Waveforms When $f_s < f_r$

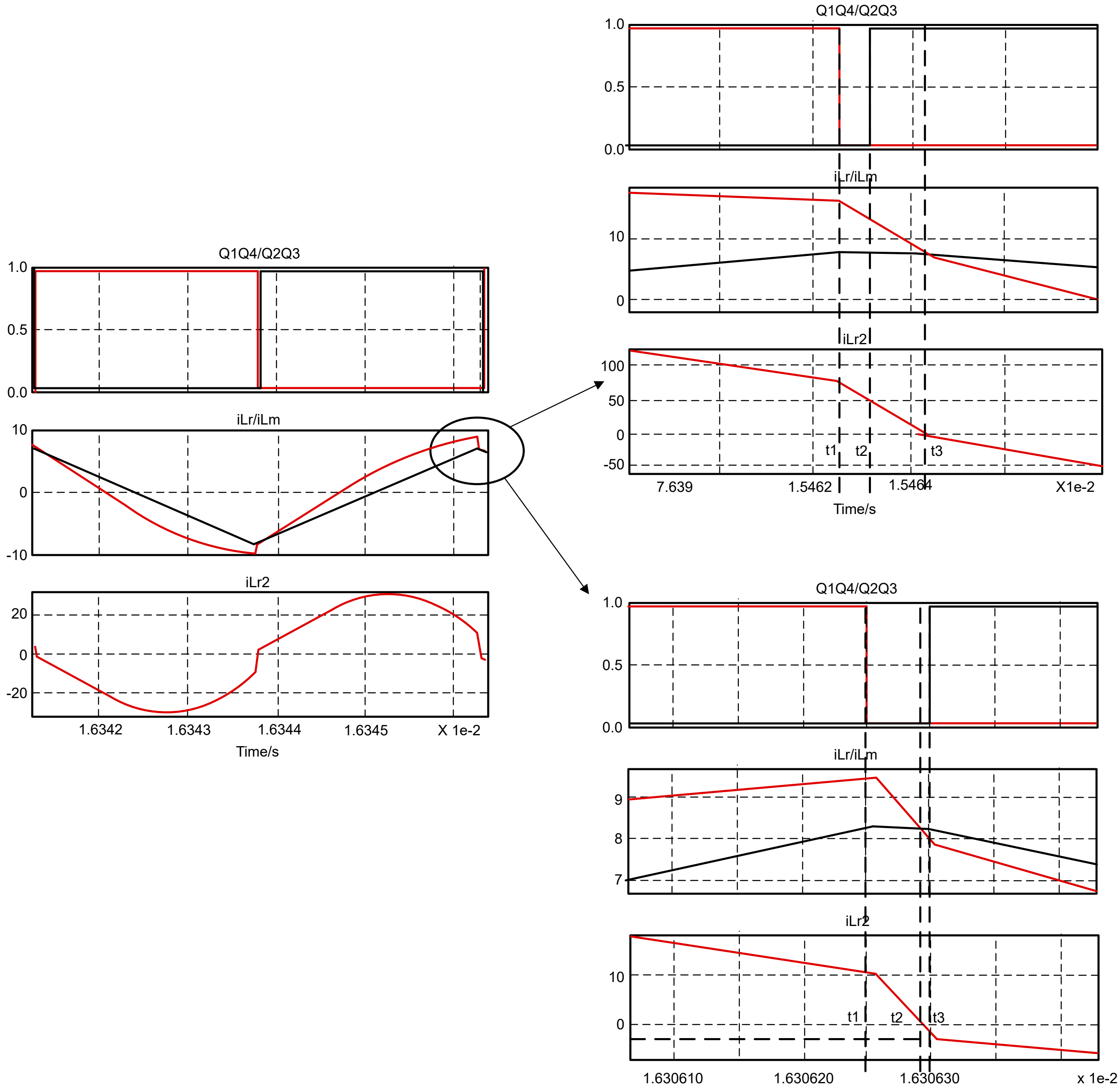

Figure 2-2. Current Waveforms When $f_s > f_r$

So, under situations like this, providing an acceptable delay is necessary to make sure that SR is not turned on in advance.

3 Solution

Much literature in the analysis of the LLC converter uses the First Harmonic Approximation (FHA) method, which has a certain guiding role in design but cannot accurately analyze the modality. To directly calculate the length of $0 - t_1$ in Figure 3-1, use the time domain analysis method. The specific analysis process is very complicated, and you can refer to process in the *Steady-state analysis of the LLC series resonant converter* article[1]. The calculation formula for time domain analysis is as follows:

$$\alpha_1 = \gamma - \phi, \quad \alpha_3 = \gamma + \phi \\ \sin(\phi) = \gamma l M \cos(y) + M \sin(y) \\ M = \frac{v0}{v_{in}}, \gamma = 2\omega_0 \frac{Ts}{2} = \frac{2\pi}{F}, F = \frac{f_s}{f_0}, l = \frac{L_r}{L_m} \tag{1}$$

where:

- V_o is the output voltage
- V_{in} is the input voltage
- f_s is the switching frequency
- f_0 is the resonant frequency
- L_r is the resonant inductor
- L_m is the magnetizing inductor.

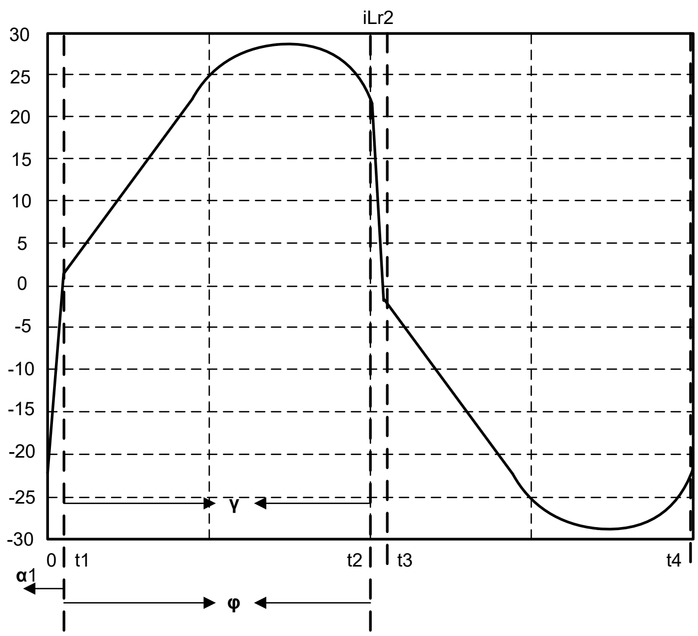

Figure 3-1. Detailed Waveforms When $f_s > f_r$

4 Simulation Verification

To verify the accuracy of the calculation results, Table 4-1 shows three sets of parameters in the simulation to observe the actual length of time, as shown in Figure 4-1, Figure 4-2, and Figure 4-3.

Table 4-1. Parameters Under Different Conditions

V_{in}	400V	400V	400V
V_o	40V	42V	40V
f_s / f_r	212khz/170khz	235khz/170khz	265khz/170khz
L_r / L_m	10uH/56uH	10uH/56uH	10uH/56uH
α_1 (simulated/calculated)	2.22e-7/2.25e-7s	7.76e-8s/7.79e-8s	9.77e-8s/9.81e-8s

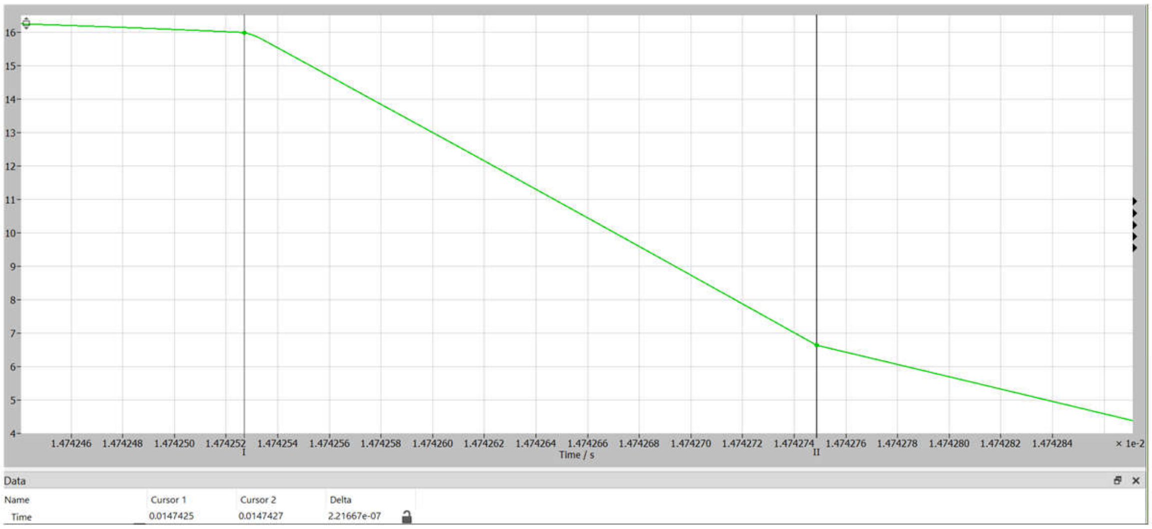

Figure 4-1. The Waveform of the First Set of Parameters

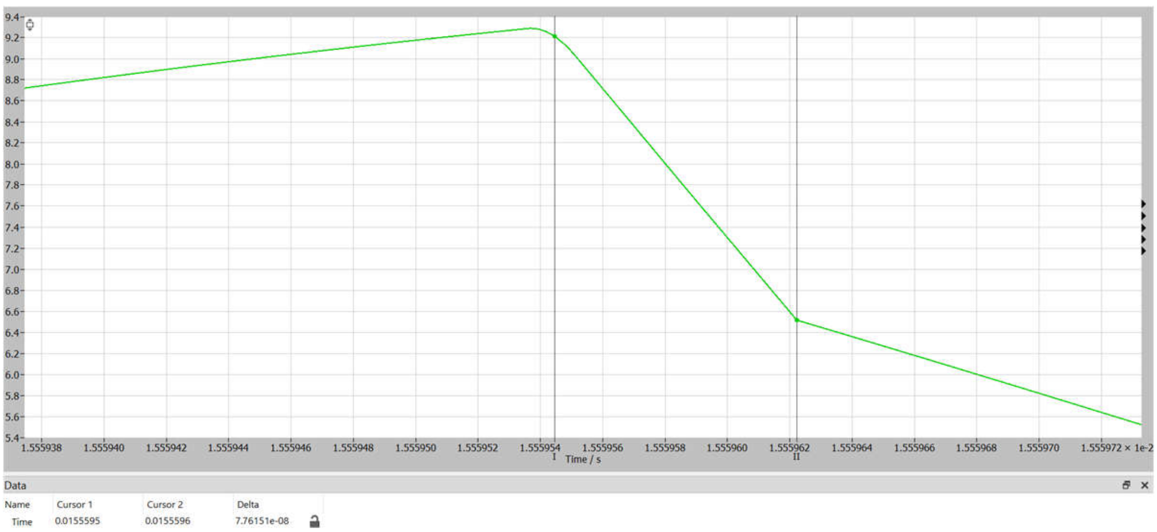

Figure 4-2. The Waveform of the Second Set of Parameters

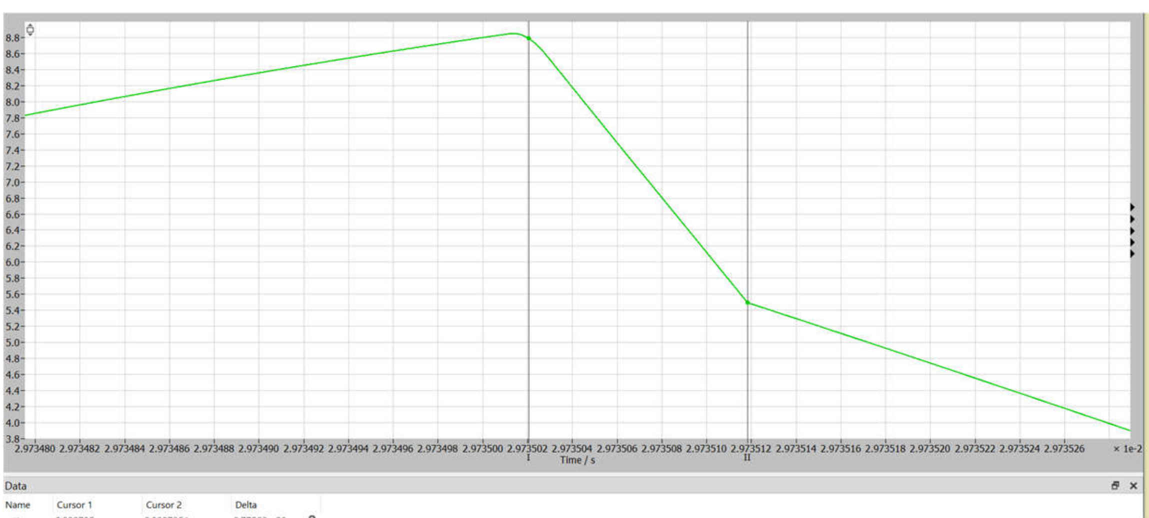

Figure 4-3. The Waveform of the Third Set of Parameters

The calculations from the simulation result are relatively accurate, meaning you can set up a delay based on these calculated results.

If the dead time is set to 100ns, then set a delay for the SR start-up time when α_1 is greater than 100ns, where delay time is α_1 minus the dead time. Figure 4-4 shows time curves α_1 for different output voltages and loads, which shows that the worst case occurs in the case of the lowest output voltage, the heaviest load.

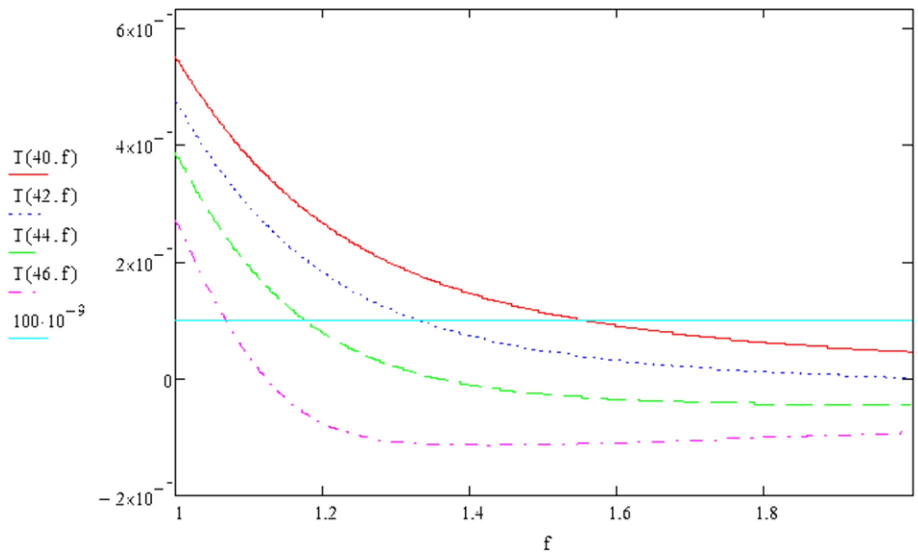

Figure 4-4. Time Curves For Different Output Voltages and Frequency

5 Conclusion

This paper analyzes the problem with a synchronous rectification scheme, that is, when the secondary rectifier switch and the primary active switch are turned on at the same time, the problem of turning on rectifier switch in advance occurs when the switching frequency is greater than the resonant frequency.

This paper proposes that the formula for time domain analysis can be used to calculate the delay of the turn-on time of the rectifier switch relative to the turn-on time of the switch in primary side, so as to confirm the normal opening of the rectifier switch.

6 References

1. J. F. Lazar and R. Martinelli, "Steady-state analysis of the LLC series resonant converter," *in APEC 2001. Sixteenth Annual IEEE Applied Power Electronics Conference and Exposition (Cat. No.01CH37181)*, vol. 2, March 2001, pp. 728–735 vol.2.

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