Application Note

Discrete Power Solution for AM62x

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ABSTRACT

AM62x is an extension of the Sitara™ Industrial grade family of heterogeneous Arm® processors with embedded 3D graphics acceleration, dual display interfaces and extensive peripheral and networking options. The low-cost AM62x Sitara processors help customers reduce system design complexity and cost. AM62x is suitable for a broad set of industrial applications that include Industrial HMI (Human Machine Interface), EV charging stations, Touchless building access and Driver monitoring systems.

This document describes the power tree for the AM62x processor using low cost discrete voltage regulators and details the specific power up/down sequencing requirement of the different voltage rails of the AM62x

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Trademarks

1 Power Requirements

AM62x requires four to eight power supply groups, depending on the system requirements. The power supply groups include the core supply (VDD_CORE), RAM supply (VDDR_CORE), DDR PHY IO supply (VDDS_DDR), 3.3 V digital supply (VDDSHVx), SD Card interface supply (VDDSHV5), 1.8 V digital supply (VDDSHVy), 1.8 V analog supply (VDDA_1P8) and a 1.8 V eFuse programming supply (VPP).

Figure 1-1 shows a block diagram of the power tree of the AM62x with DDR4. The different voltage regulators for these rails were chosen based on cost, good efficiency, load transient performance, and power up/down sequencing requirements.

The LM61460-Q1, buck converter is used to supply the 3.3V, VDDSHVx rail as well as act as the input supply for the rest of the voltage regulators, except the TLV7103318 in the power tree. VDDSHVy, VDDS_DDR, VDD_CORE and VDDR_CORE are supplied by the TPS6282x family of buck converters. These are high efficiency small solution size buck converters having controlled turn on and turn off times. The VDDA_1P8 and VPP are supplied by 2 LDOs - TPS74518 and TLV75518 respectively. The VDDSHV5 (SD Card IO power supply) rail can be configured to run either at 3.3 V or 1.8 V and is powered using a TLV7103318 LDO. A couple of logic gates along with an RC delay is also required for proper sequencing of the VDD_CORE and VDDR_CORE rails. A detailed circuit schematic detailing the power solution and sequencing is shown in Figure 1-1.

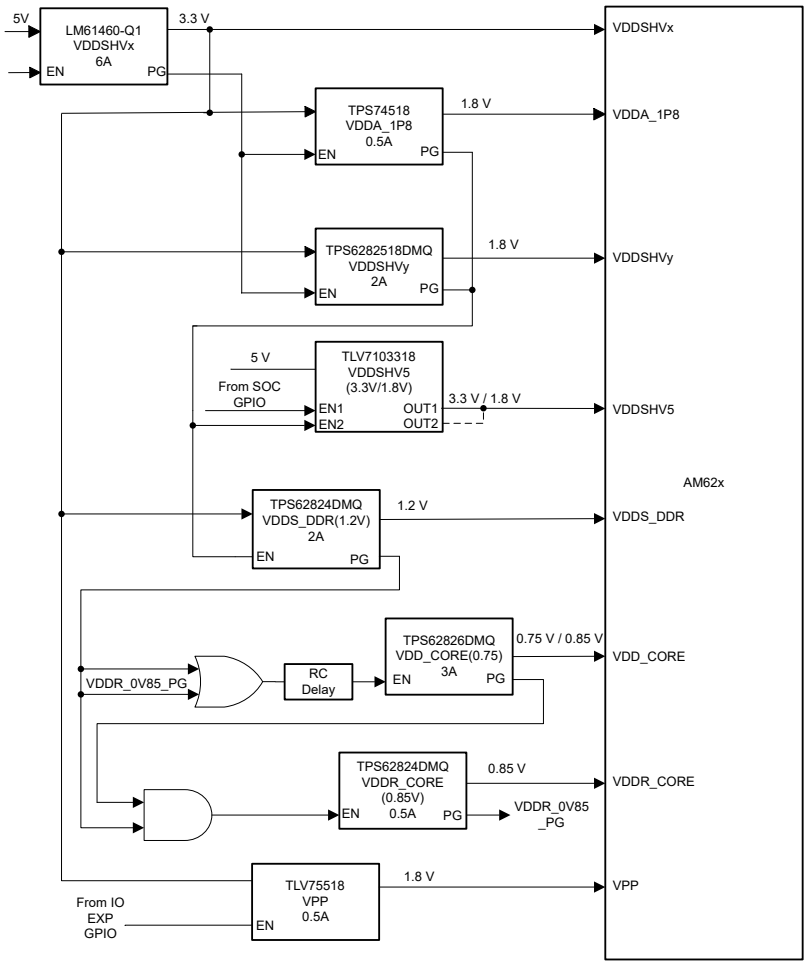

Figure 1-1. Functional Block Diagram of AM62x Power Tree with DDR4 (1.2 V)

The AM62x power requirements are listed in Table 1-1.

Table 1-1. AM62x Power Requirements

Power Supply	V_{OUT} (V)	I_{OUT} (mA)	Output Voltage (V)	Power Supply	Nominal Rating	Grouping
LM61460-Q1	Adjustable	6000	3.3	VDDSHV_MCU, VDDSHV0, VDDSHV2, VDDSHV3, VDDSHV_CANUART, VDDA_3P3_USB, VMON_3P3_SOC	3.3 V ±5%	VDDSHVx
TLV7103318	3.3, 1.8	200	3.3 / 1.8	VDDSHV5	3.3 V ±5% 1.8 V ±5%	VDDSHV5
TPS74518	1.8	500	1.8	VDDA_MCU, VDDA_PLL0, VDDA_PLL1, VDDA_PLL2, VDDA_1P8_CSIRX0, VDDA_1P8_OLDI0, VDDA_1P8_USB, VMON_1P8_SOC, VDDA_TEMP0, VDDA_TEMP1	1.8 V ±5%	VDDA_1P8
TPS6282518	1.8	2000	1.8	VDDSHV1, VDDSHV4, VDDSHV6, VMON_1P8_SOC,	1.8 V ±5%	VDDSHVy
TPS62824	Adjustable	2000	1.2	VDDS_DDR, VDDS_DDR_C	1.2 V ±5%	VDDS_DDR
TPS62826	Adjustable	3000	0.75	VDD_CORE, VDD_CANUART, VDDA_CORE_CSIRX0, VDDA_CORE_USB, VDDA_DDR_PLL0	0.75 V ±5%	VDD_CORE
TPS62824	Adjustable	2000	0.85	VDDR_CORE	0.85 V ±5%	VDDR_CORE
TLV75518	1.8	500	1.8	VPP	1.8 V ±5%	VPP

1.1 Power on Sequence

AM62x requires the different power rails to be ramped up in a certain sequence to ensure a reliable and fault free operation. Figure 1-2 shows the power-on sequence of the power rails. Shaded regions in Figure 1-2 indicate, that particular rail is allowed to ramp up at any time within this region. The 3V3, VDDSHVx and VDDSHV5 rails are the first rails to be powered on. Next, the 1.8V analog and digital rails are ramped up. This is followed by the 1.2 V DDR rail. By ramping up the 0.75 V, VDD_CORE before the 0.85 V, VDDR_CORE, it is made sure that the VDDR_CORE voltage never exceeds the VDD_CORE voltage by 180 mV. If VDD_CORE is operating at 0.85 V, both VDD_CORE and VDDR_CORE can be supplied by the same rail and there is no ramp up requirement between them. The 1.8 V, VPP is the eFuse programming supply, which shall be left floating (HiZ) or grounded during power-up/down sequences and during normal device operation. This supply shall only be sourced while programming.

For a detailed description of the power-on sequencing please refer to section 7.10.2.2.1 of the data sheet.

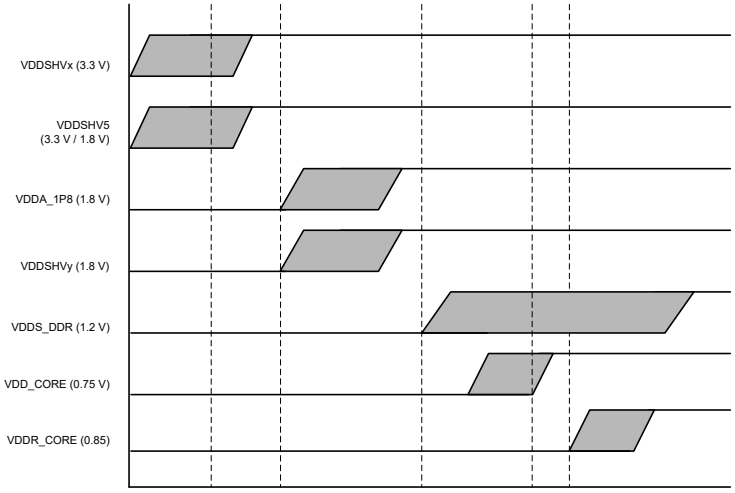

Figure 1-2. Power-On Sequence for AM62x

1.2 Power-Off Sequence

As described in section 7.10.2.2.2 in the data sheet, all power rails except VDD_CORE and VDDR_CORE can be ramped down independent of each other. If VDD_CORE is operating at 0.75 V, it should be ramped down after the 0.85 V VDDR_CORE. For the case where VDD_CORE and VDDR_CORE both run from a common 0.85 V supply, there is no ramp down requirement between them.

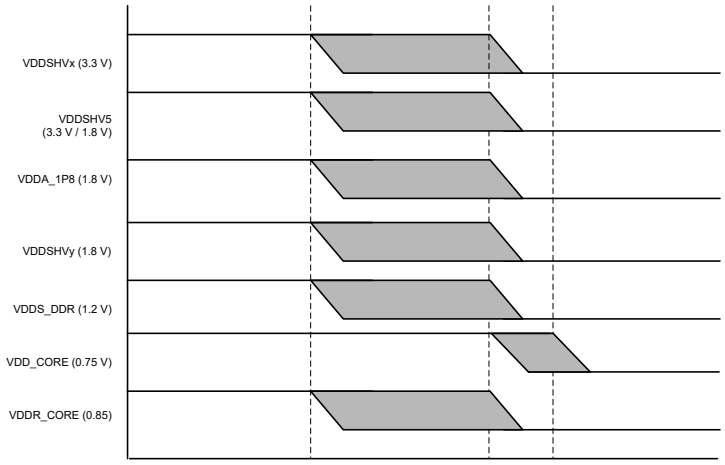

Figure 1-3. Power-Off Sequence for AM62x

2 Schematic

Figure 2-1 shows the circuit schematic detailing the external components required by the optimized discrete solution to achieve the different power rails required by the AM62x. Proper power-on or off sequencing is achieved by connecting the EN pin of a converter to the PG pin of the converter supplying the previous rail in the power-on or off sequence.

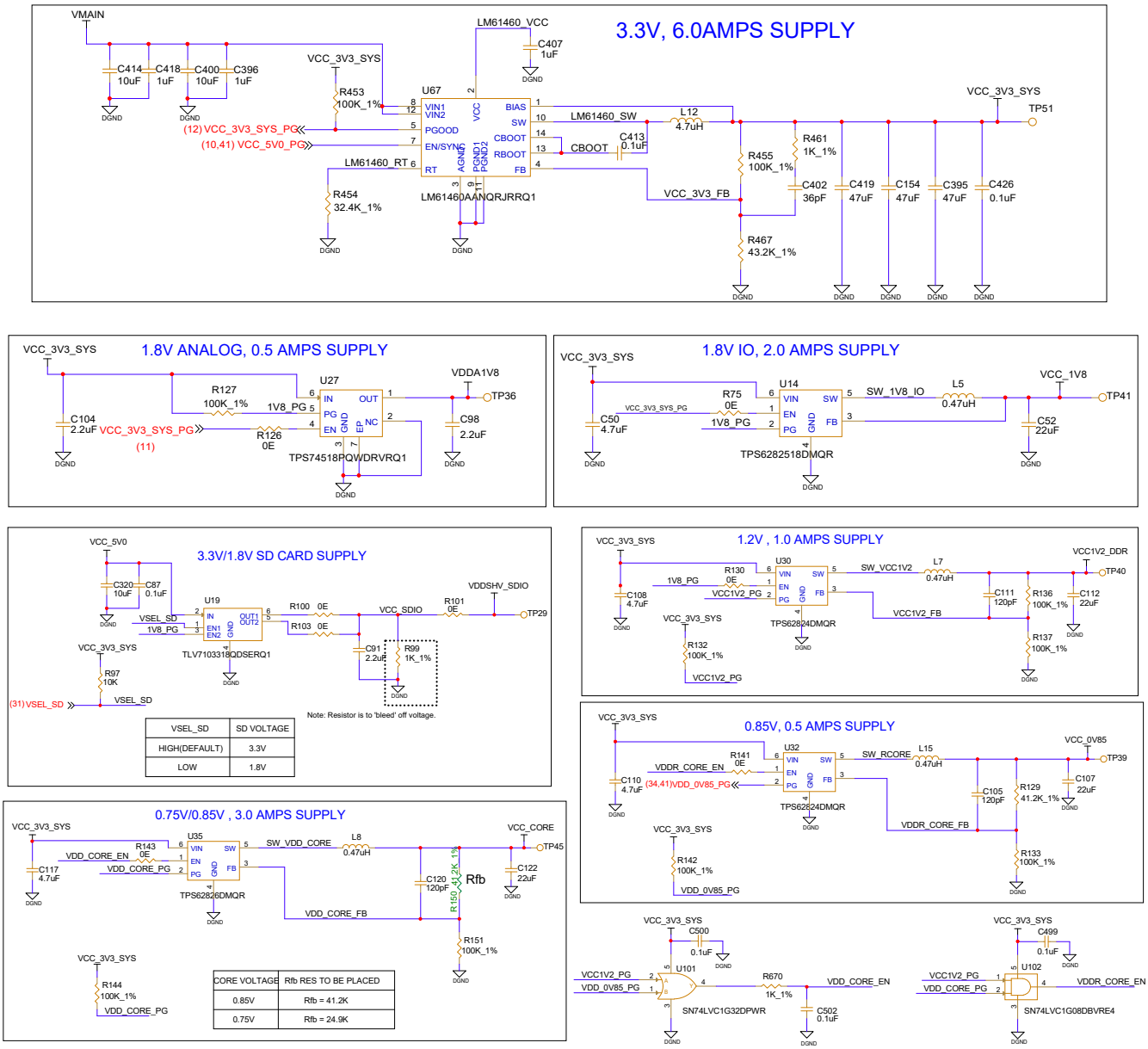

Figure 2-1. AM62x Power Supply Schematics

3 Bill of Materials

The bill of materials for the BOM-optimized discrete power solution is listed in Table 3-1.

Table 3-1. Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR
3	C105, C111, C120	120 pF	CAP CERAMIC 120 pF 25 V 10% X7R	0201	GRM033R71E121KA01D	MURATA
1	C402	36 pF	CAP CERAMIC 36 pF 50 V 2% HI-Q C0G(NP0)	0402	GJM1555C1H360GB01D	MURATA
5	C87, C413, C426, C500, C502	0.1 uF	CAP CERAMIC 0.1 uF 50 V 10% X7R	0402	GRM155R71H104KE14D	MURATA
2	C396, C418	1 uF	CAP CERAMIC 1 uF 100 V 10% X7S	0805	GRM21BC72A105KE01L	MURATA
1	C407	1 uF	CAP CERAMIC 1 uF 16 V 20% X5R	0201	GRM033R61C105ME15D	MURATA
3	C91, C98, C104	2.2 uF	CAP CERAMIC 2.2 uF 25 V 10% X5R	0402	GRM155R61E225KE11D	MURATA
4	C50, C108, C110, C117	4.7 uF	CAP CERAMIC 4.7 uF 35 V 20% X5R	0603	GRM188R6YA475ME15D	MURATA
3	C320, C400, C414	10 uF	CAP CERAMIC 10 uF 35 V 20% X5R	0603	GRM188R6YA106MA73D	MURATA
4	C52, C107, C112, C122	22 uF	CAP CERAMIC 22 uF 10 V 20% X5R	0603	GRM188R61A226ME15D	MURATA
3	C154, C395, C419	47 uF	CAP CERAMIC 47 uF 16 V 10% X6S	1210	GRM32EC81C476KE15L	MURATA
2	L5, L7	470nH	IND CHIP 0.47 uH 4.5 A 20%	0806	DFE201612E-R47M=P2	MURATA
1	L12	4.7uH	IND POWER 4.7 uH 11A 20% SMD		XAL6060-472MEB	COILCRAFT
2	R99, R670	1K	RES 1K 1/10W 1%	0402	Std	Std
1	R97	10K	RES 10K 1/20W 5%	0201	Std	Std
1	R454	32.4K	RES 32.4K 1/16W 1%	0402	Std	Std
2	R129, R150	41.2K	RES 41.2K 1/16W 1%	0402	Std	Std
1	R467	43.2K	RES 43.2K 1/16W 1%	0402	Std	Std
10	R127, R132, R133, R136, R137, R142, R144, R151, R453, R455	100K	RES 100K 1/10W 1%	0402	Std	Std
1	U101	SN74LVC1G32DPWR	IC SINGLE 2-INPUT POSITIVE-OR GATE X2SON5	SON-5	SN74LVC1G32DPWR	TI
1	U102	SN74LVC1G08DBVRE4	IC SINGLE 2-INPUT POSITIVE AND GATE SOT23-5	SOT-23-5	SN74LVC1G08DBVRE4	TI
1	U27	TPS74518PQWDRVRQ1	IC 1.8 V 500 mA LDO WITH POWER-GOOD WSON6	WSON-6	TPS74518PQWDRVRQ1	TI
1	U14	TPS6282518DMQR	IC 2A 1.8 V STEP-DOWN CONVERTER WITH 1% OUTPUT ACCURACY VSON-HR6	VSON-HR-6	TPS6282518DMQR	TI
1	U19	TLV7103318QDSERQ1	IC 200 mA 3.3 V/1.8 V LOW IQ LDO REGULATOR WSON6	WSON-6	TLV7103318QDSERQ1	TI
2	U30, U32	TPS62824DMQR	IC 1A ADJ STEP-DOWN CONVERTER WITH 1% OUTPUT ACCURACY VSON-HR6	VSON-HR-6	TPS62824DMQR	TI
1	U35	TPS62826DMQR	IC 3A ADJ STEP-DOWN CONVERTER WITH 1% OUTPUT ACCURACY VSON-HR6	VSON-HR-6	TPS62826DMQR	TI
1	U67	LM61460AANQRJRRQ1	IC 6A ADJ AUTO LOW EMI SYNCHRONOUS STEP-DOWN DC-DC CONVERTER VQFN-HR14	VQFN-HR-14	LM61460AANQRJRRQ1	TI

4 Waveforms

The waveforms in Figure 4-1 and Figure 4-2 show the power up and down sequence of the different power rails measured on the AM62x discrete power EVM.

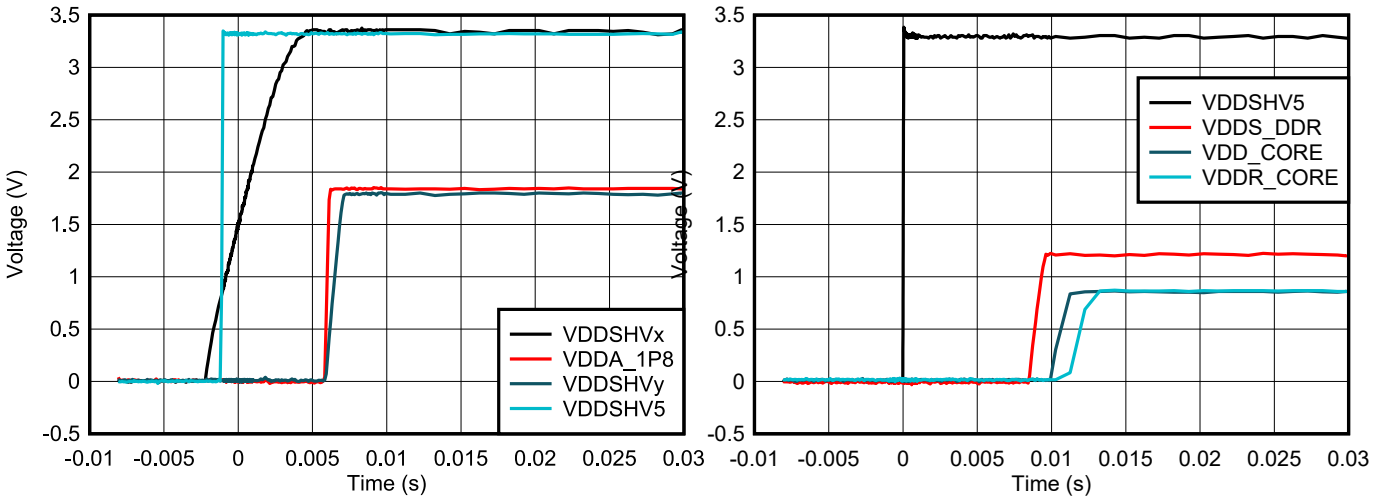

Figure 4-1. Measured Power-On Sequence for AM62x

On the AM62X discrete power EVM, the power-down sequence is triggered by the ramp down of the 3.3 V, VDDSHVx rail as shown in Figure 4-2.

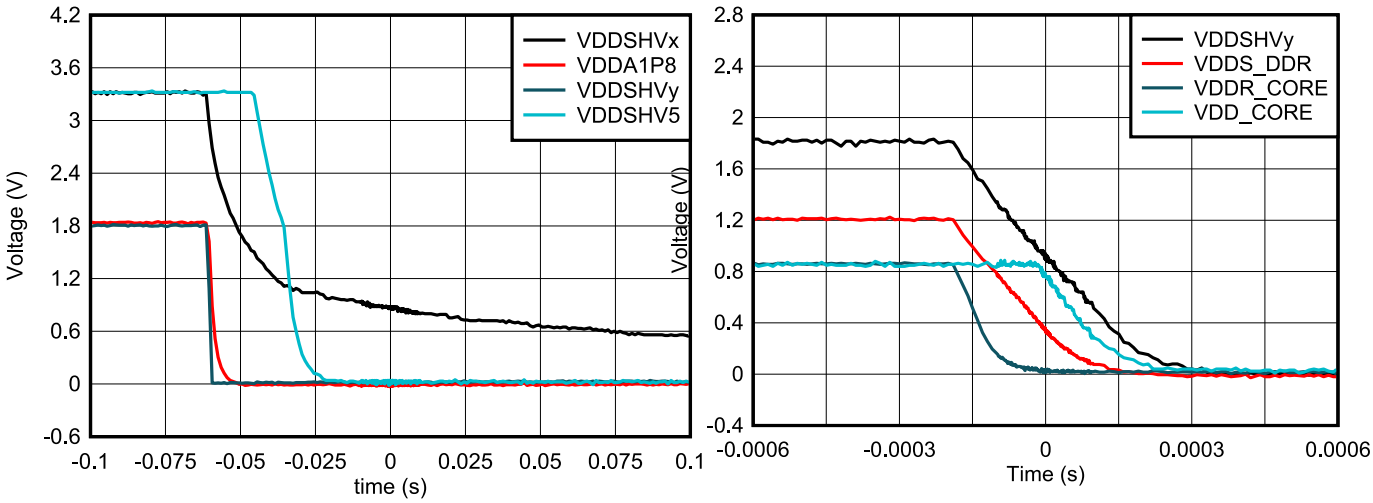

Figure 4-2. Measured Power-Off Sequence for AM62x

5 Sequencing VDD_CORE and VDDR_CORE Rails

When VDD_CORE is supplied at 0.75 V instead of 0.85 V, power on or off sequencing between the VDD_CORE and VDDR_CORE rails become important. The sequencing requirement of ramping up the VDD_CORE rail before the VDDR_CORE rail during power on and ramping down after the VDDR_CORE rail during power off is achieved by using simple AND and OR gates along with an RC delay.

During power on, a logic high on the PG pin of the 1.2 V VDDS_DDR rail enables the VDD_CORE rail. Since the PG of the VDD_CORE rail is also an input to the AND gate driving the EN pin of VDDR_CORE rail, the VDDR_CORE rail will only get enabled after the VDD_CORE rail completes its startup. For the power down sequence, a logic low on the PG pin of the 1.2 V VDDS_DDR rail disables the VDDR_CORE rail. Once the VDDR_CORE rail starts discharging its output, a logic low on the PG pin will cause the output of the OR gate driving the EN pin of the VDD_CORE rail through the RC filter to go low. However, the RC filter adds a delay to the output of the OR gate, thereby delaying the turn off of the VDD_CORE rail.

Figure 5-1 and Figure 5-2 show the power on and off sequencing achieved between the VDD_CORE and VDDR_CORE on the AM62x discrete power EVM. On this EVM, the VDDR_ CORE was configured to run at 0.85 V. The logic for the required sequencing when the VDD_CORE rail runs at 0.75 V was implemented on this EVM to demonstrate functionality. The value of the RC delay depends on the value of the output discharge resistor or current sink of the converters supplying these rails. For the recommended TPS6282x regulators, an RC delay of 0.1 ms made up with a 1 KOhm and a 0.1 µF capacitor is sufficient.

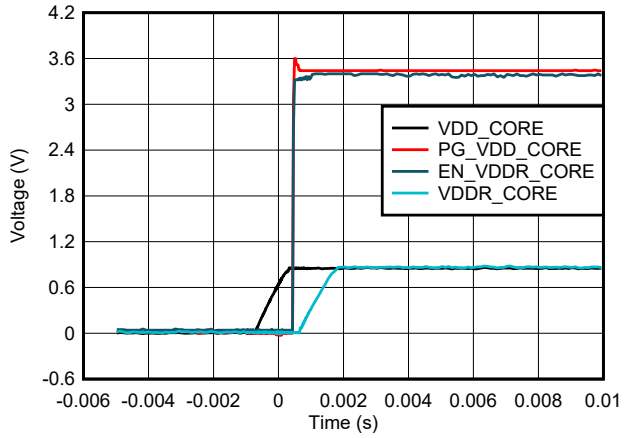

Figure 5-1. Measured Power On Sequence of VDD_CORE and VDDR_CORE

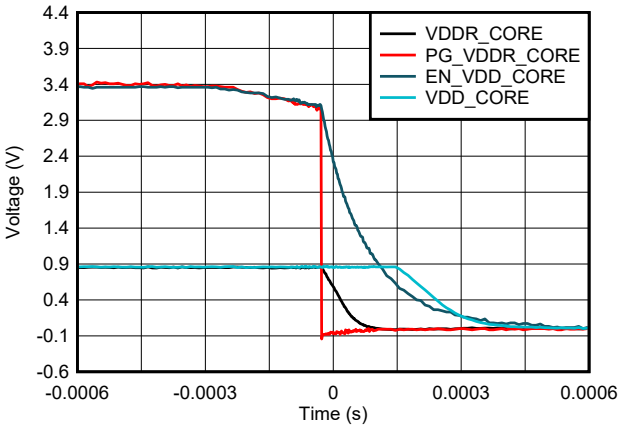

Figure 5-2. Measured Power Off Sequence of VDD_CORE and VDDR_CORE

6 Summary

The TPS6282x and LM61460-Q1 buck converters along with the TPS74518, TLV7103318 and TLV75518 LDOs provide a BOM optimized, discrete power solution for the AM62x. This document details the required external components for the discrete ICs as well as the sequencing connections between them to meet the power on/off requirements of AM62x. Simple logic AND and OR gates along with an RC delay helps to achieve the correct sequencing between the VDD_CORE and VDDR_CORE rails. This document can be used as a reference for choosing a series of discrete devices for powering the AM62x.

7 References

1. Texas Instruments, *TPS6282x 2.4-V to 5.5-V Input, 1-, 2-, 3-, 4-A Step-down Converter with 1% Output Accuracy* data sheet
2. Texas Instruments, *TPS745-Q1 500-mA LDO With Power-Good in Small Wettable Flank WSON Packages* data sheet
3. Texas Instruments, *TLV755P 500-mA, Low IQ, Small Size, Low Dropout Regulator* data sheet
4. Texas Instruments, *TLV7103318 Dual, 200-mA, Low-IQ Low-Dropout Regulator* data sheet
5. Texas Instruments, *LM61460-Q1 3-V to 36-V, 6-A, Low EMI Synchronous Step-Down Converter* data sheet
6. Texas Instruments, *AM62x Sitara™ Processors* data sheet

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