Application Note

UCC25640x LLC Resonant Controller Features Brief Overview and Bring up Guidelines

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ABSTRACT

The UCC25640x is the latest family of LLC controllers from Texas Instruments. The UCC25640x has improved features and optimized performance compared to the previous generation devices UCC25630x. This application note briefly discusses each feature of the controller using block diagrams and typical waveforms. Finally, it goes through power up procedure and debugging tips for each pin of the controller.

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1 UCC25640x Selection Guide

Table 1-1. Device Comparison Table

	UCC256402	UCC256402A	UCC256403	UCC256403A	UCC256404	UCC256404A	UCC256404B
Key Application	Lighting/ Industrial	Lighting/ Industrial	TV OLED Screen/ Telecom/ Industrial	TV OLED Screen/ Telecom/ Industrial	TV - WLLC	TV - WLLC	TV - WLLC
Burst Packet Size	16	16	40	16	40	16	40
Burst Soft On/Off	No	No	Yes	No	Yes	No	Yes
HV Startup	Yes	Yes	No	No	Yes	Yes	Yes
Auxiliary Supply Required	No	No	Yes	Yes	No	No	No
X-Cap Discharge (XCD)	No	No	No	No	Yes	Yes	Yes
BLK/DC Start (1)	3 V/340 V	3 V/340 V	3 V/340 V	3 V/340 V	1 V/113 V	1 V/113 V	1 V/113 V
BLK/DC Stop (1)	2.2 V/249 V	2.2 V/249 V	2.2 V/249 V	2.2 V/249 V	0.9 V/102 V	0.9 V/102 V	0.9 V/102 V
BLK/DC OVP (1)	NA	4 V/453 V	NA	NA	NA	NA	NA
BW OVP Mode	Restart	Restart	Restart	Latch	Restart	Latch	Restart
Other Fault Mode	Restart	Restart	Restart	Restart	Restart	Restart	Restart
PFC Off in Standby Mode	No	No	No	No	Yes	Yes	Yes
VCC startup voltage that will initiate startup process	26 V	26 V	10.9 V	10.9 V	26 V	26 V	26 V

(1) Typical startup, shutdown and overvoltage values assume Bulk Divider ratio 113.33:1

The UCC256404B maximum XCD test current is lower (1.3mA) compared to the maximum XCD test currents of the 404 and 404A (1.7mA). This difference helps to reduce stand-by power loss when using the UCC256404B during very-light-load to no-load conditions.

2 UCC25640x Features Brief Overview

2.1 High Voltage(HV) Startup

2.1.1 HV Startup Procedure

Figure 2-1 shows the startup procedure for UCC256402 and UCC256404 devices. Here we can observe that RVCC will be enabled only when VCC reaches 26 V.

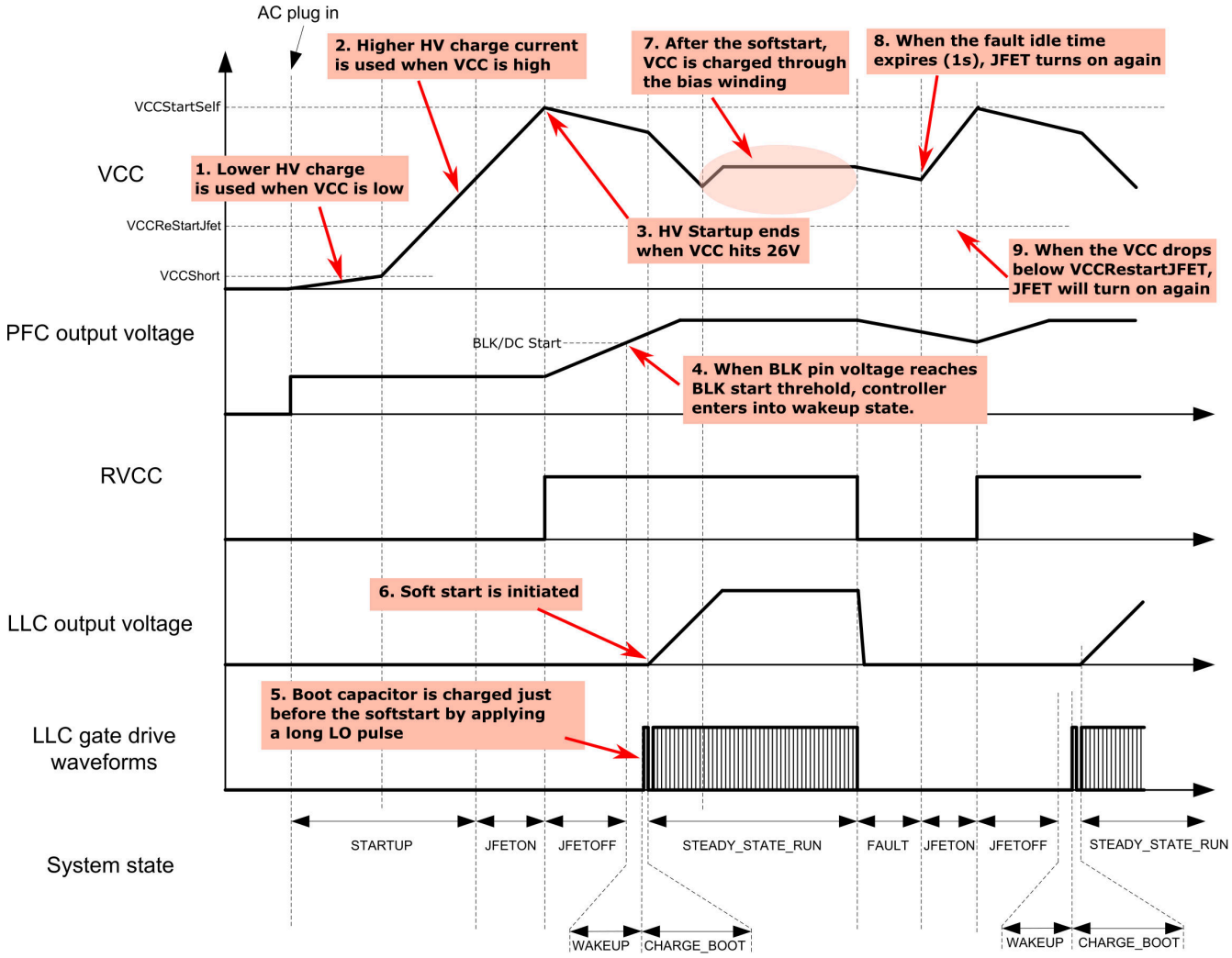

Figure 2-1. HV Startup for 402 and 404 Devices

2.1.2 HV Startup with External Bias

As mentioned in Table 1-1, 403 devices does not have an HV startup. Auxiliary supply is needed to startup these devices. Figure 2-2 shows the startup procedure for UCC256403 devices with auxiliary supply.

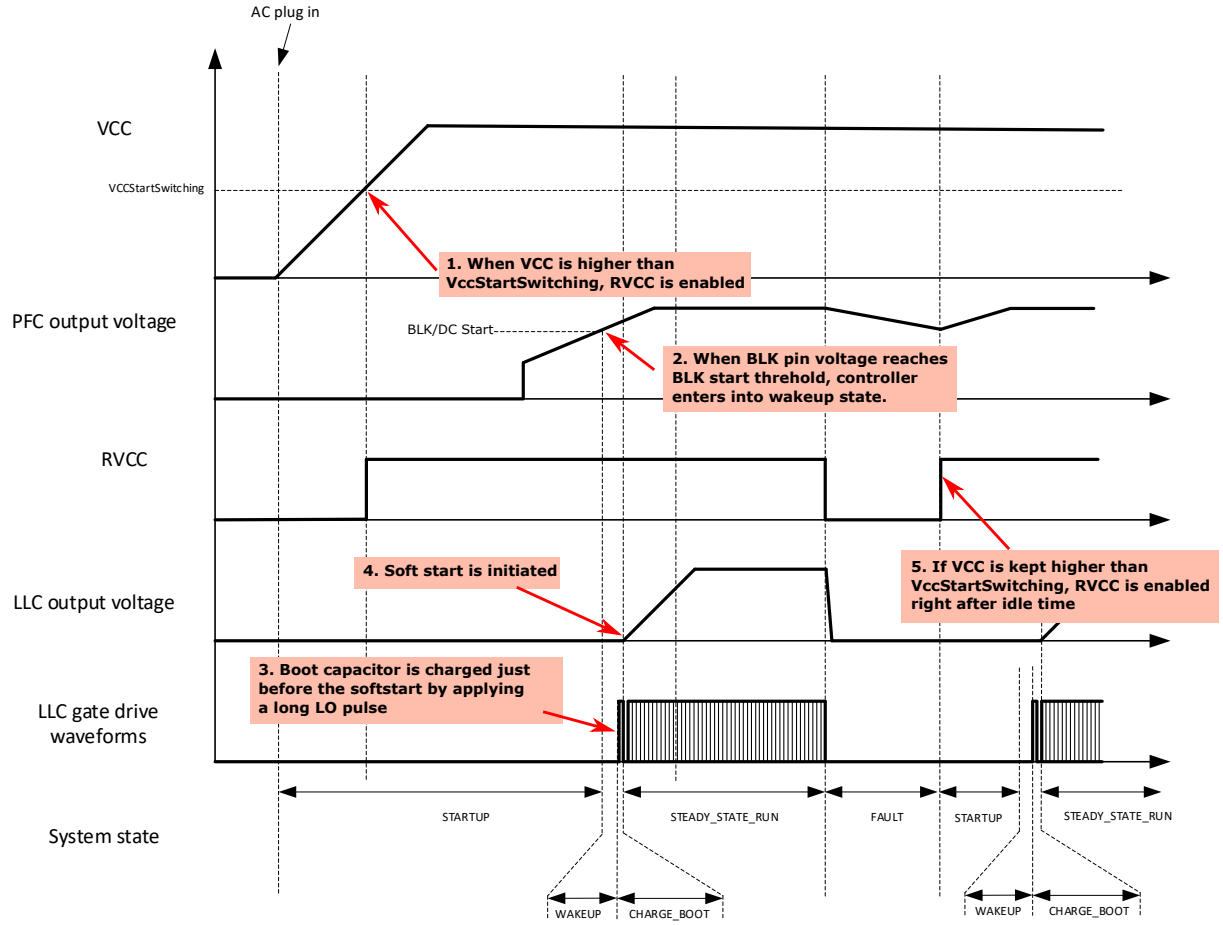

Figure 2-2. HV Startup with External Bias for 403 Devices

2.1.3 HV Start-up, VCC, X-cap Discharge Internal Block Diagram

- Figure 2-3 shows the internal architecture of the HV, VCC, X-cap discharge block.
- The switch S1 shown in Figure 2-3 controls high voltage startup for the device. Once the VCC pin exceeds the VccStartSelf (402 and 404 devices), this switch will be turned off which means HV startup is finished.

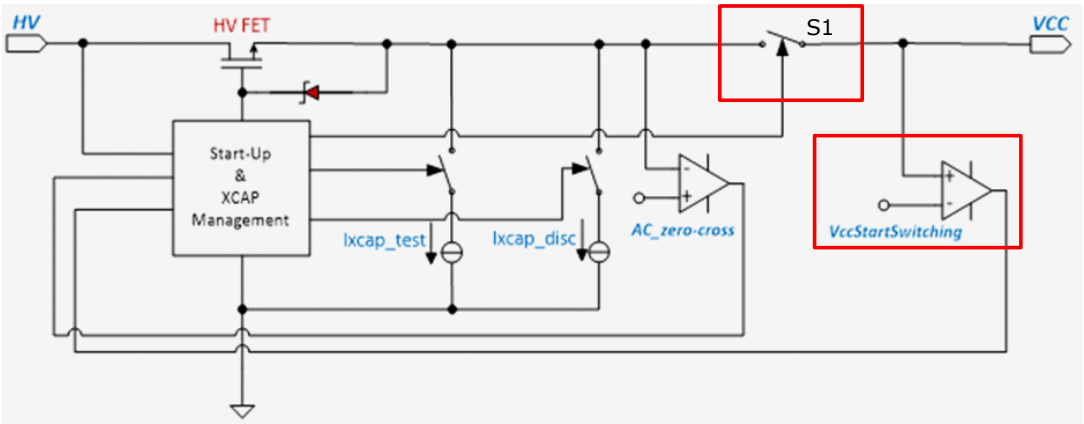

Figure 2-3. HV, VCC, X-cap Discharge Internal Block Architecture

2.1.4 HV Startup External Resistor

The typical recommended resistor value for R_{HV} shown in Figure 2-4 is 5k Ohm.

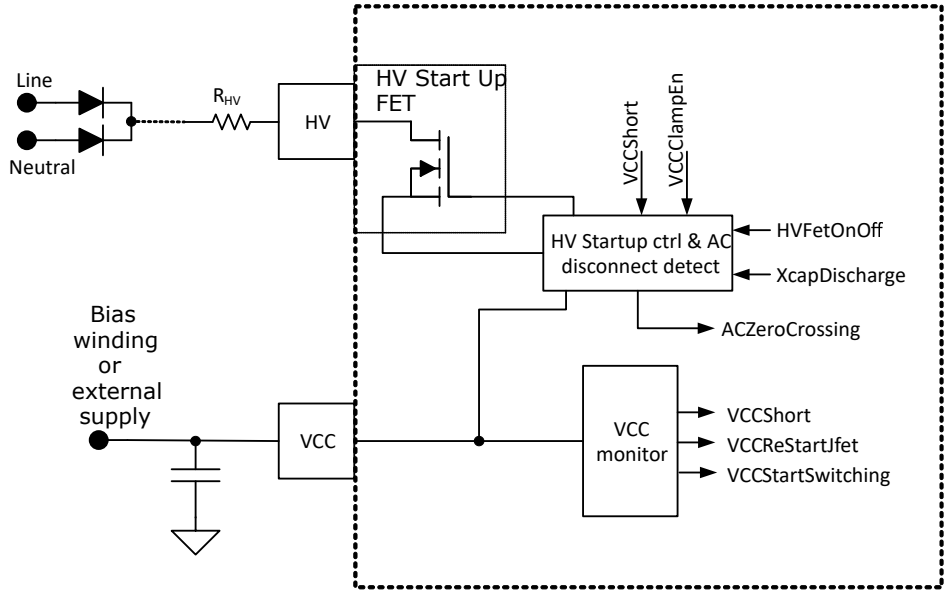

Figure 2-4. HV Startup Block Diagram

2.2 XCAP Discharge

2.2.1 IEC Standards

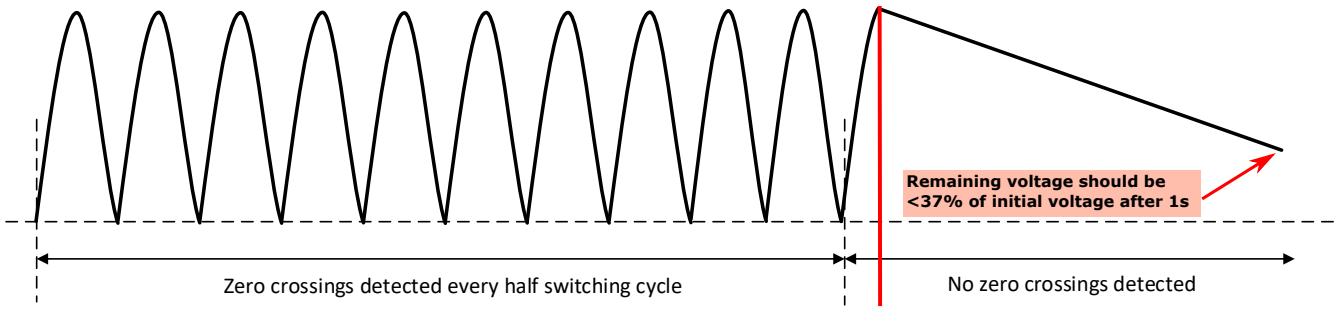

Figure 2-5. Voltage at HV Pin for Zero Crossing Detection

- IEC60950 and IEC60065: 1s after AC disconnect, the remaining voltage on x-capacitor should be less than 37% of the initial voltage.
- IEC62368: 2s after AC disconnect, the remaining voltage on x-capacitor should be less than 60 V.

2.2.2 Detecting AC presence

- HV pin is connected to Line and Neutral through two rectifier diodes as shown in Figure 2-4; This pin's voltage is used to detect if AC is present.
- Under ideal conditions when AC is connected, the HV pin should detect the zero crossing where the voltage between Line and Neutral reaches 0 V twice per cycle. However, due to the parasitic capacitance of the diode bridge, the voltage at HV will not reach zero. To overcome this, current is sinked from HV to GND.

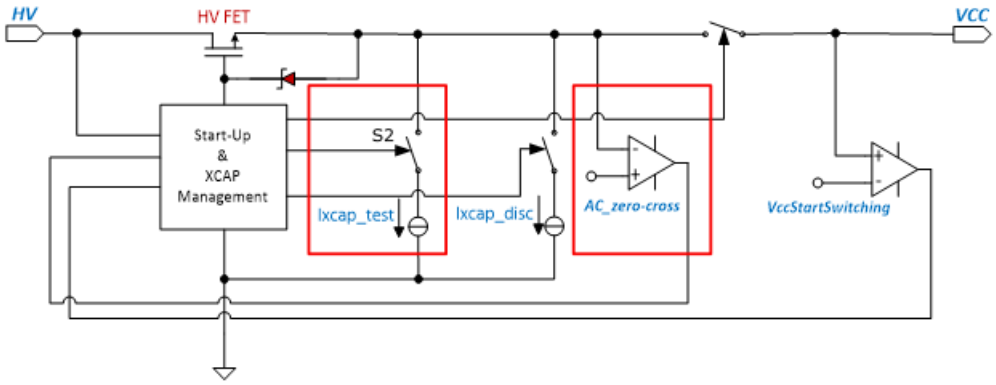

Figure 2-6. X-cap discharge internal block diagram

- The switch S2 highlighted in Figure 2-6 controls the Ixcap test current to determine if AC is still connected. The logic is looking for the HV pin to be pulled below 9V. Note this test current goes to gnd.

2.2.3 Test Current Injection for Zero Crossing Detection

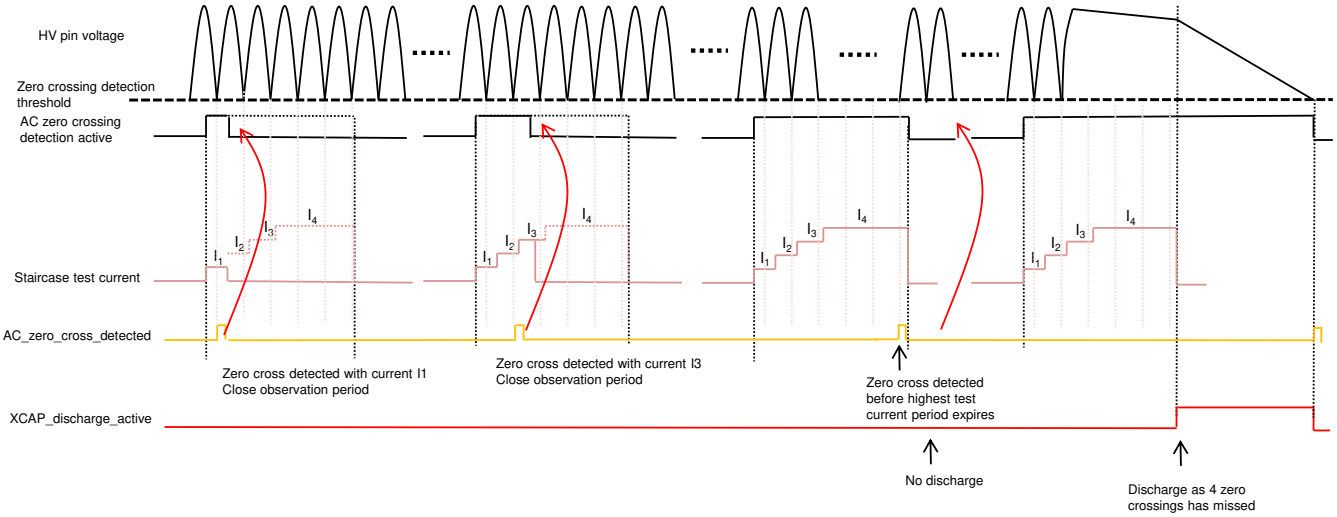

Figure 2-7. Xcap Discharge

- Test current I1 is applied to check if HV pin voltage is <9 V threshold.
- When HV pin voltage falls below 9 V, test current is turned off and controller waits 700 ms before applying I1 again.
- I1 test current is on for maximum of 12 ms. If HV pin does not satisfy <9 V requirement, test current is increased to I2, then I3 and finally, I4.
- I4 test current maximum on time is 48 ms.
- If zero crossing is not detected during the test current period, a discharge current of 11.5 mA (typical value) is applied for 350 ms from HV to GND as shown in Figure 2-7.

2.2.4 Typical Waveforms of HV Startup and XCAP Discharge

Figure 2-8. Test Condition: AC Plugged in, BLK UVLO; Ch1 – LO, Ch2 – VCC, Ch3 – RVCC, Ch4 – HV

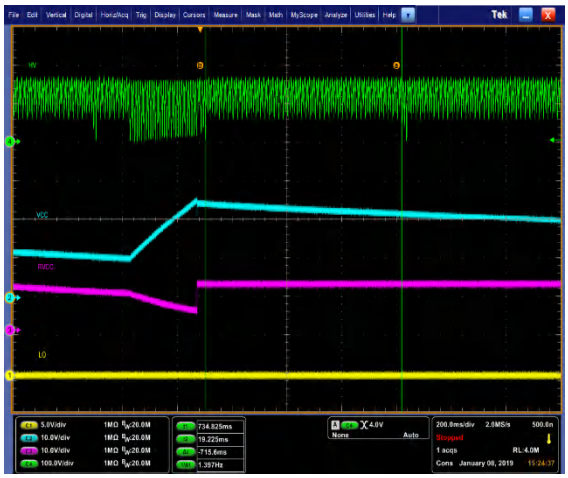

Figure 2-9. Zoomed In: Test Condition: AC Plugged in, BLK UVLO; Ch1 – LO, Ch2 – VCC, Ch3 – RVCC, Ch4 – HV

In Figure 2-8 and Figure 2-9, we can observe that whenever test current being injected (for every 700 ms) HV pin voltage is being pulled down. Also, when VCC is reduced to VCCRestartJFET threshold, VCC charging is initiated.

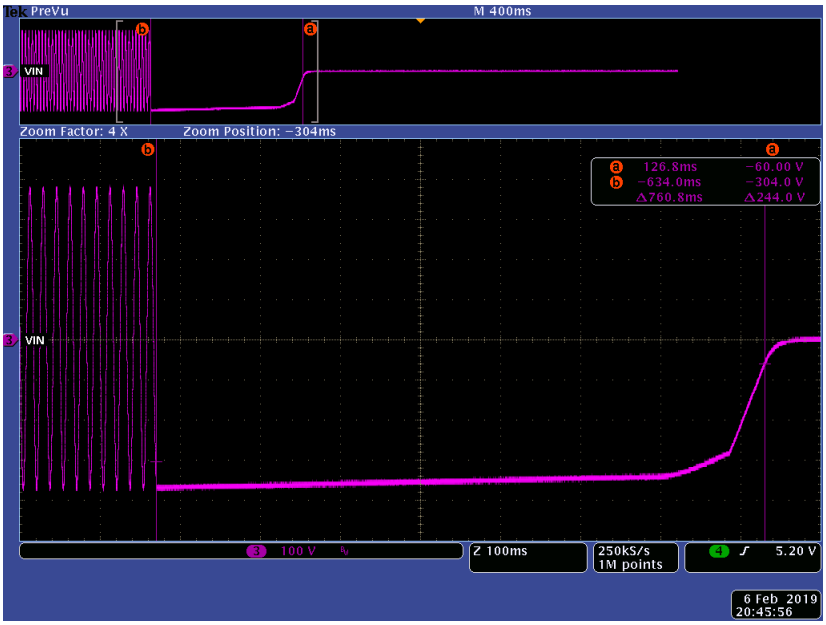

Figure 2-10. Waveform Capture of AC Input Removal and X-cap Discharge

2.3 Feedback Chain

As UCC25640x is a primary side LLC controller, the output voltage/current is regulated by a voltage/current regulator circuit located on the secondary side of the isolation barrier. The demand signal from the secondary side regulator circuit is transferred across the isolation barrier via an opto-coupler (U1) as shown in Figure 2-11.

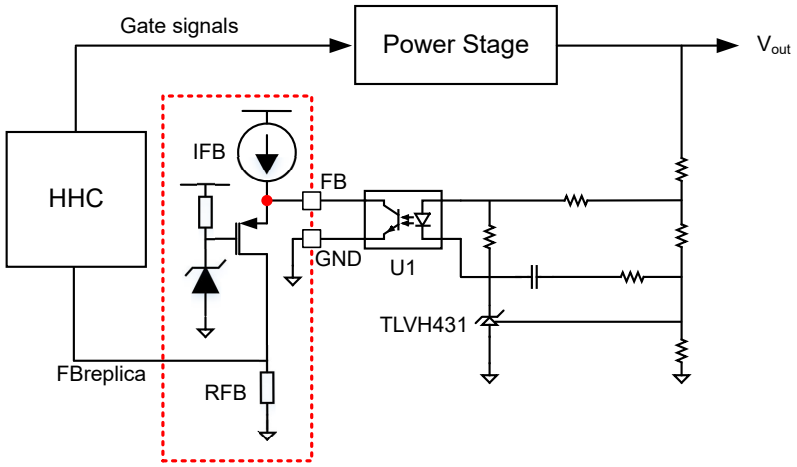

Figure 2-11. Feedback Chain Block Diagram

2.3.1 FBreplica Generation

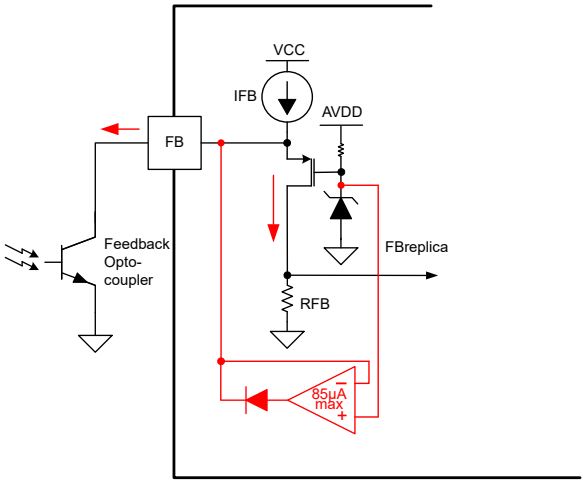

Figure 2-12. FBreplica Generation

- FB pin is supplied with an IFB current source
- The optocoupler collector voltage maintained at approximate constant voltage (~5.6 V) when FB sourcing current is less than IFB. Due to this, no extra pole introduced due to the optocoupler parasitic capacitor
- The FB clamp circuit is to provide extra 82uA current to the FB pin when needed to prevent FB voltage drop and to maintain good transient performance
- The Optocoupler current is reflected as the FBreplica in the IC for control purpose
- Voltage at the RFB is given by FBreplica = (IFB-Ioptocoupler) *RFB where RFB typical value is 100 kohm and IFB typical values are 82 uA (for 402, 404 devices) and 164 uA (403, 403A devices).
- If the current through optocoupler is zero during the heavy output load, FB pin voltage will be clamped to internal whereas FBreplica is clamped to 6 V.

2.3.2 Vcomp Signal and Threshold Voltages

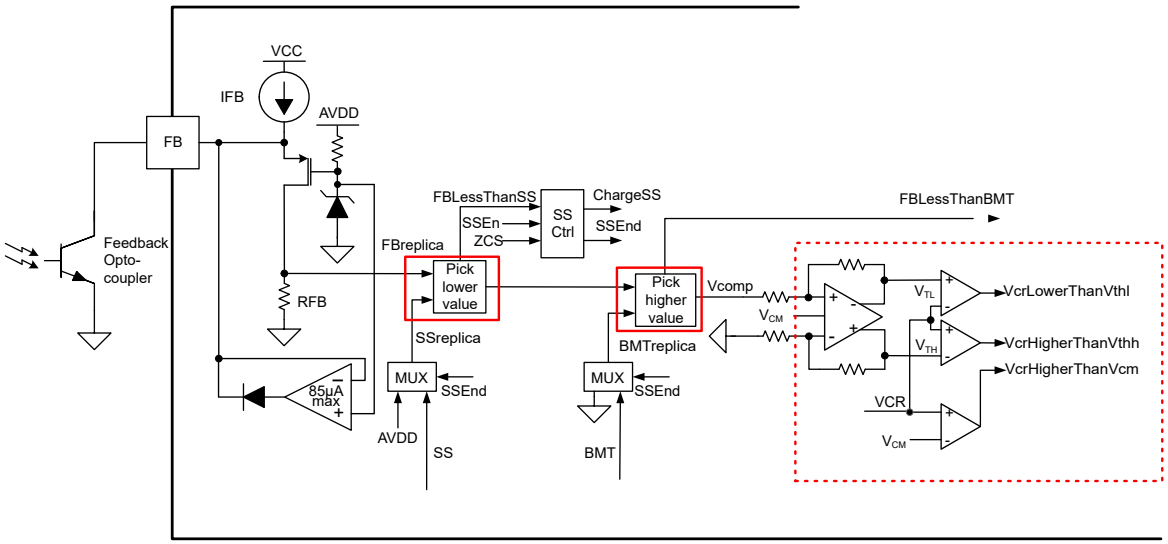

Figure 2-13. Feedback Chain Block Diagram

- Vcomp is the control effort used to determine the switching frequency of the LLC in UCC25640x.
- During soft start, Vcomp is the lower value between FBreplica and Soft start signal.
- During burst mode, Vcomp is the higher value between FBreplica and BMTL (Minimal burst mode entry threshold).
- Threshold voltages for VCR are given as VTH = VCM + Vcomp/2 and VTL= VCM - Vcomp/2 where VCM is 3 V. These can be seen in Figure 2-14.

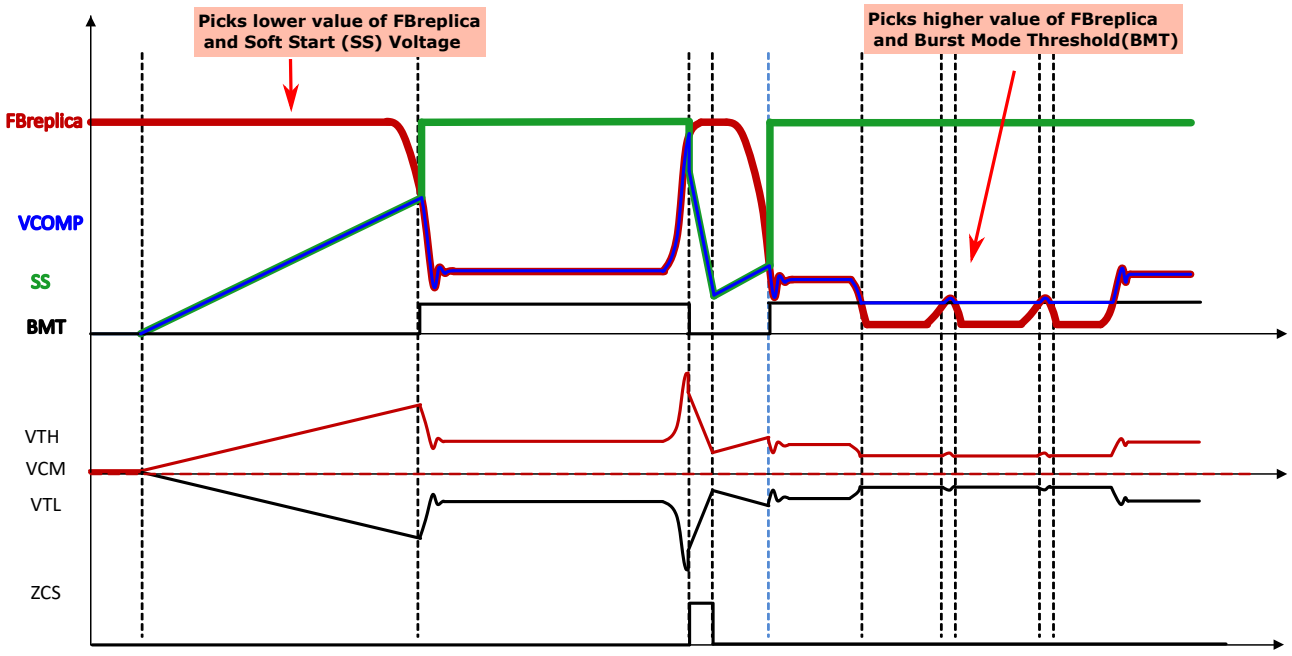

Figure 2-14. VTH and VTL During Startup, Burst Mode, ZCS and Normal Operation

2.3.3 FB Pin Voltage Typical Waveform at no Load

Figure 2-15 shows the FB pin voltage during no load. Here we can see that FB pin voltage is close to 5.6 V whenever FB pin current value is smaller than the sum of IFB current source and the clamp current source. Otherwise it is at zero.

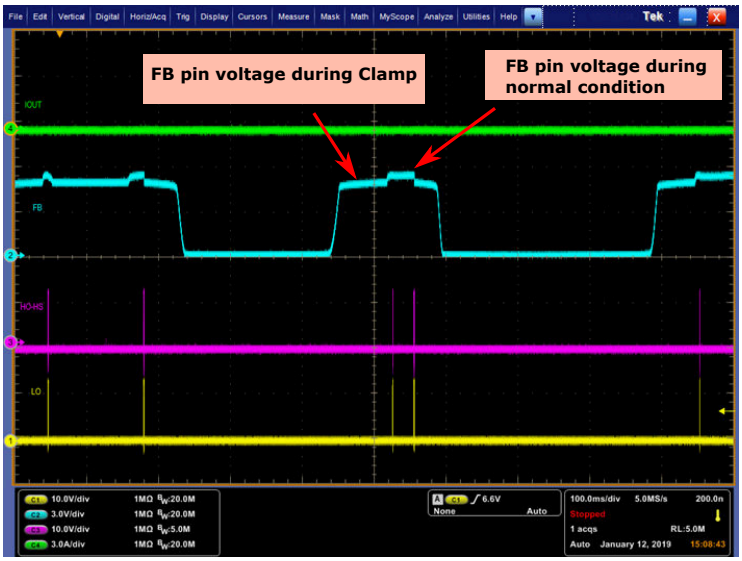

Figure 2-15. Ch1- LO, Ch2-FB, Ch3- (HO-HS), Ch4-Iout

2.4 Hybrid Hysteretic Control and VCR Pin Voltage and Gate Pulse Generation

2.4.1 Hybrid Hysteretic Control

Hybrid Hysteretic Control (HHC) is a charge control with added frequency ramp. It is analogous to current mode control with added slope compensation of a PWM converter. HHC control enables the LLC resonant converter to achieve higher bandwidth and faster transient response.

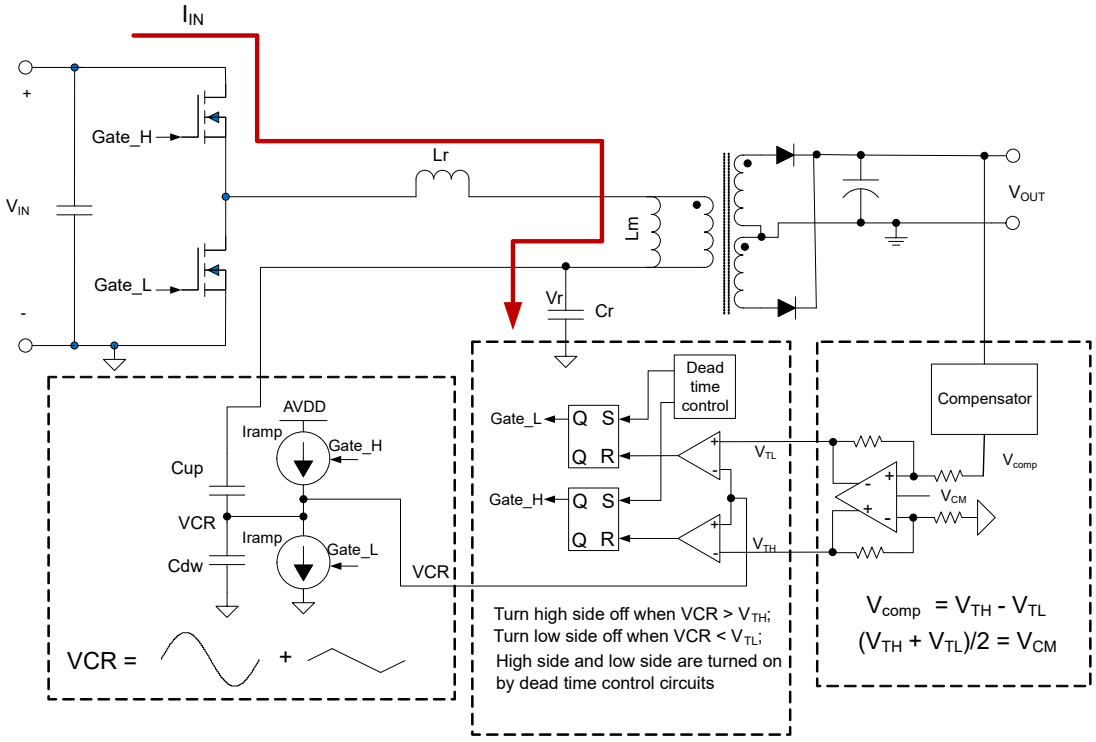

Figure 2-16. HHC Basic Scheme

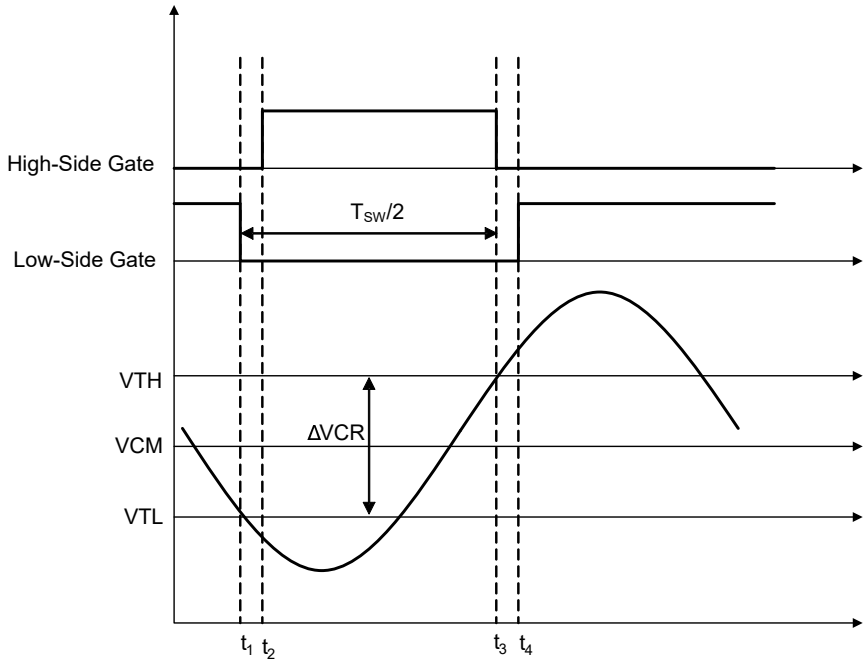

Figure 2-17. HHC Control Basic Waveforms

$$V_{comp} = (I_{FB} - I_{opto}) \cdot R_{FB} \quad (1)$$

$$V_{TH} = V_{CM} + \frac{V_{comp}}{2} \quad (2)$$

$$V_{TL} = V_{CM} - \frac{V_{comp}}{2} \quad (3)$$

$$V_{TH} - V_{TL} = V_{CM} + \frac{V_{comp}}{2} - V_{CM} + \frac{V_{comp}}{2} = V_{comp} \quad (4)$$

$$\Delta V_{CR} = \frac{C_{up}}{C_{up} + C_{dw}} \cdot \Delta V_r + \frac{1}{C_{up} + C_{dw}} \cdot I_{ramp} \cdot \frac{T_{sw}}{2} \quad (5)$$

$$\Delta V_{CR} = V_{TH} - V_{TL} = V_{comp} \quad (6)$$

$$\Delta V_{CR} = V_{comp} \cong \frac{C_{up}}{C_{up} + C_{dw}} \cdot \frac{1}{C_r} \cdot T_{sw} \cdot I_{in_{(avg)}} + \frac{1}{C_{up} + C_{dw}} \cdot I_{ramp} \cdot \frac{T_{sw}}{2} \cong \frac{C_{up}}{C_{dw}} \cdot \frac{1}{C_r} \cdot T_{sw} \cdot I_{in_{(avg)}} + \frac{1}{C_{dw}} \cdot I_{ramp} \cdot \frac{T_{sw}}{2} \quad (7)$$

2.4.2 VCR Pin Voltage

The VCR pin voltage is one of the important signals for this LLC controller as this signal determines turn on instants of the both low side and high side switches.

- The resonant capacitor voltage is sensed using lossless capacitor divider (Cup and Cdw) as shown in Figure 2-16.
- The VCR waveform is composed of two components: the sampled resonant capacitor voltage and the voltage due to internal frequency compensation current. This frequency compensation is added using two well-balanced current sources (Iramp) as shown in Figure 2-16.
- The added compensation will make the VCR signal in the form of a triangle voltage superimposed on the sinusoidal resonant capacitor voltage (Vr). Equation 5 gives the relation between change in VCR pin voltage and the change in resonant capacitor voltage and the frequency compensation current.
- Equation 7 gives the relation between change in VCR pin voltage and the Vcomp signal and average input current and slope compensation current. When the output power is high, converter operates similar to charge control as the input average current component given in Equation 7 dominates the added frequency component. The slope compensation has a small impact on transfer function. The overall transfer function will be approximately first order plant transfer function similar to charge control. When output power is low, converter operates in direct frequency control as the input average current will be very small. These operations will be true assuming we set the proper *mix* between the sampled voltage and the compensation current in the VCR pin signal. This needs proper selection of Cup and Cdw capacitors.
- Figure 2-17 shows that when VCR > VTH, high side gate signal (HO) turns off and when VCR < VTL, high side gate signal (LO) turns off. These thresholds are related to Vcomp signal as given in Equation 2 and Equation 3. The turn on instants of the HO and LO signals depends on the adaptive dead time control given in the Section 2.7.
- VCR pin also has a common mode voltage (VCM) of 3 V and the peak to peak voltage should be less than 6vV at the minimum operating input voltage with maximum load.
- The VCR voltage affects the initial switching frequency profile during startup so it is important to make sure there is sufficient margin to avoid tripping OCP when starting into maximum load. The initial switching frequency also impacts the startup timing. Section 2 of the *UCC25630x Practical Design Guidelines* gives more detail regarding the impact of VCR voltage on startup behavior.

2.4.3 VCR Typical Waveform

Figure 2-18. Ch1 – LO, Ch2 – VCR, Ch3 – ISNS, Ch4 – Resonant Inductor Current

- In Figure 2-18, an obvious transition can be noticed on VCR voltage at gate transition edges.
- Vcomp can be measured as difference between VCR values (VCR1-VCR2) during the switching instants.

2.5 Soft Start

LL/SS (Light Load and Soft start) pin is used for programming soft start ramp rate, burst mode high threshold and the initial frequency at the startup.

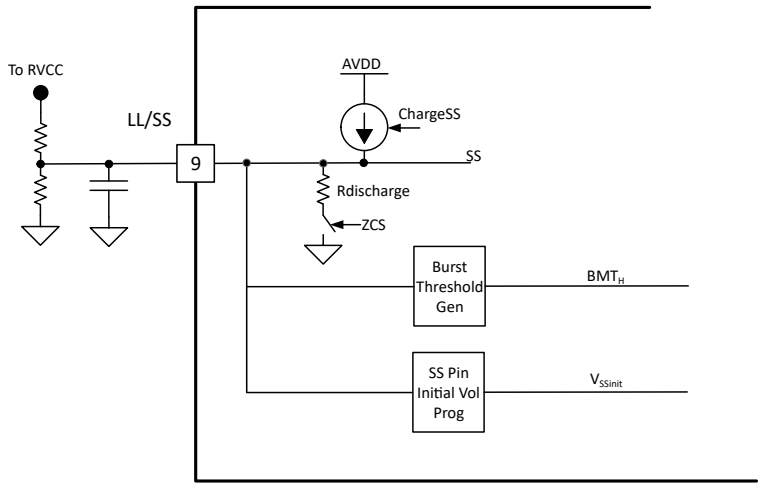

Figure 2-19. LL/SS Pin

2.5.1 Soft Start Timing

- LL/SS pin capacitor determines Soft start control signal ramp rate. This would make sure initial frequency is slowly ramps down until feedback signal takes over as shown in Figure 2-14. This ramp rate helps to avoid the stress in the power stage components during the startup. Note that burst mode is disabled during the soft start which is shown in Figure 2-20
- LL/SS pin resistors and capacitor together programs the initial voltage on the pin for startup
- LL/SS pin resistors programs the burst mode high threshold.

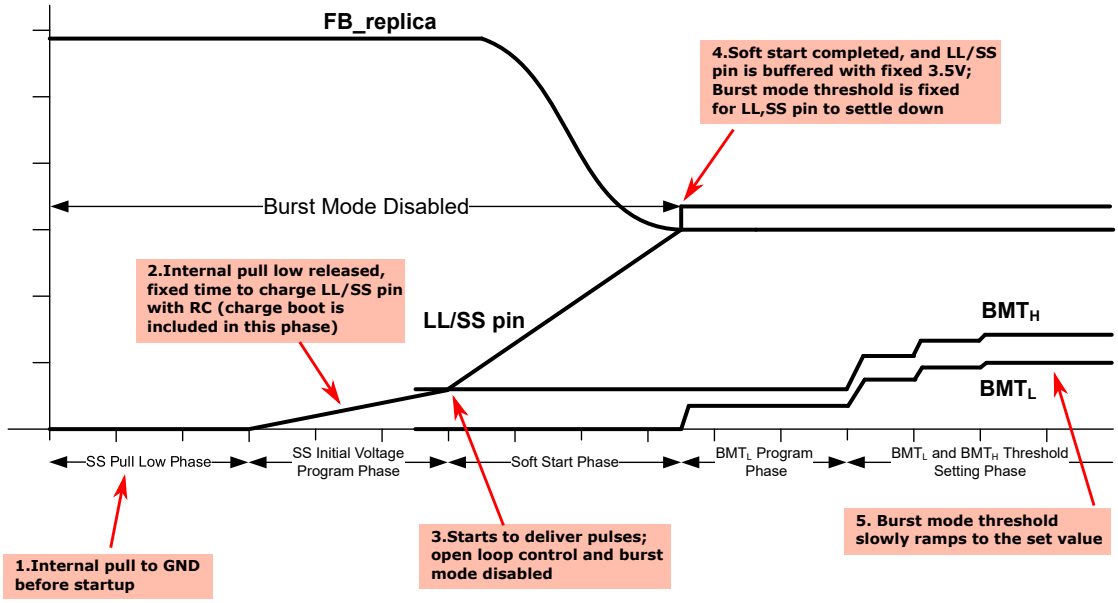

Figure 2-20. Soft Start Timing

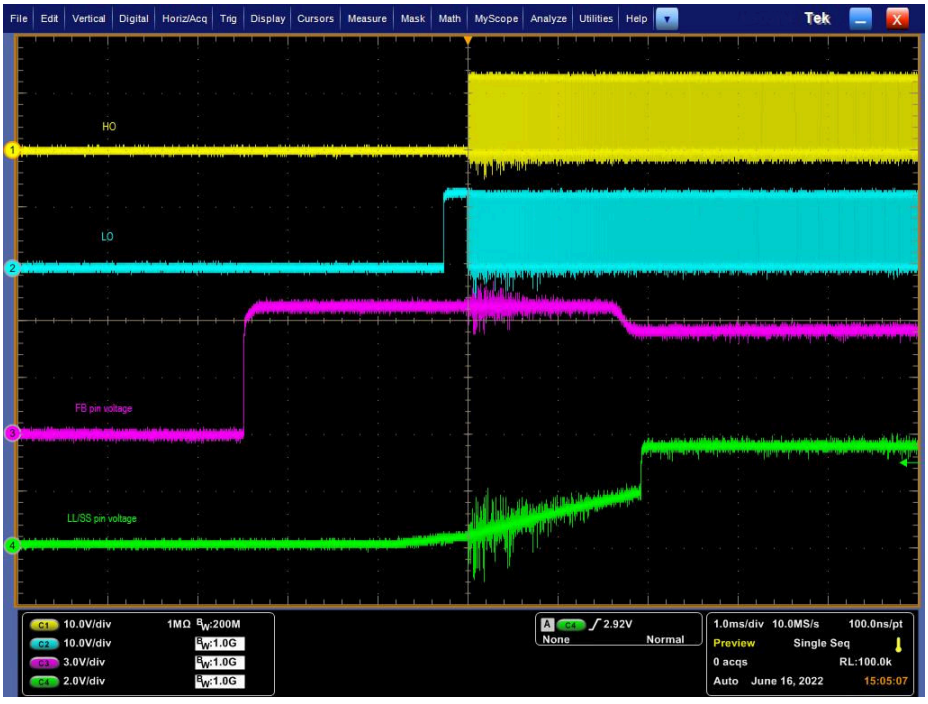

Figure 2-21. Startup waveform Ch1 – HO Ch2 – LO Ch3 – FB Ch4 – LL/SS

2.5.2 Soft Start Initial Voltage Programming

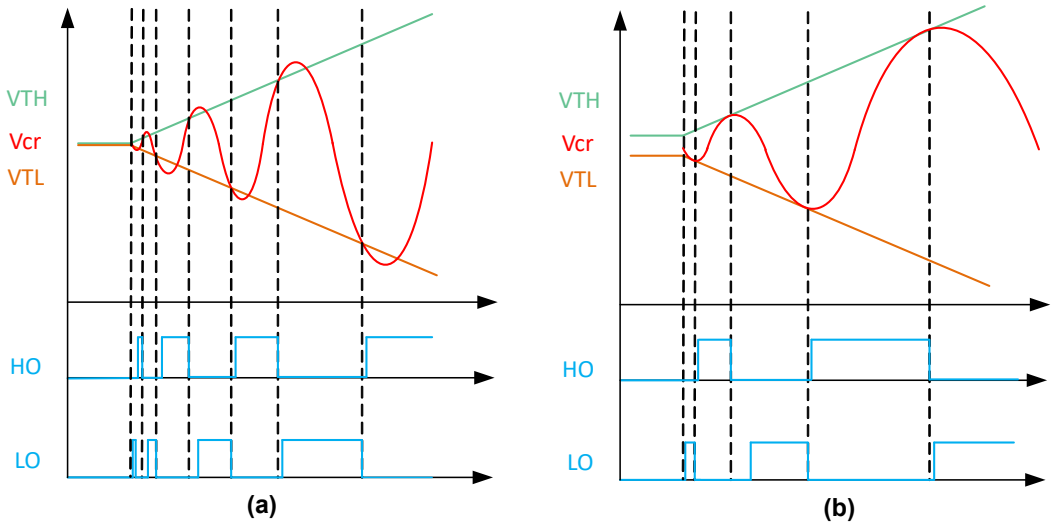

Figure 2-22. a) With Soft Start Initial Voltage (Vssinit) is Zero Volts b) Vssinit not at 0 V

- Figure 2-22 shows that, Vssinit voltage adjusts the maximum startup switching frequency. This helps to prevent the hard switching at the startup which is shown in Figure 2-23.
- The suggested range for the Vssinit would be 0 V to 1 V.

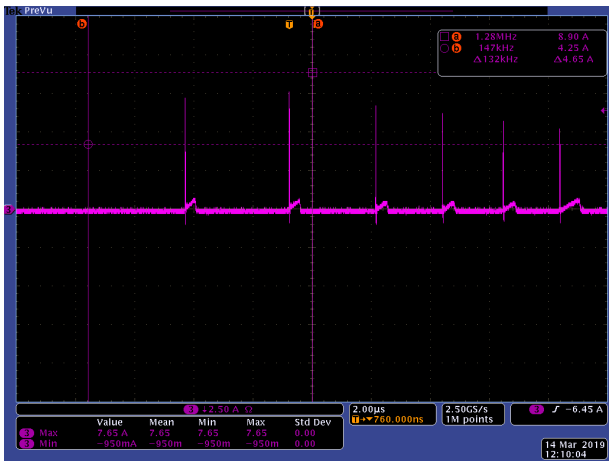

Figure 2-23. High Side MOS Current Without Initial Voltage on LL/SS Pin

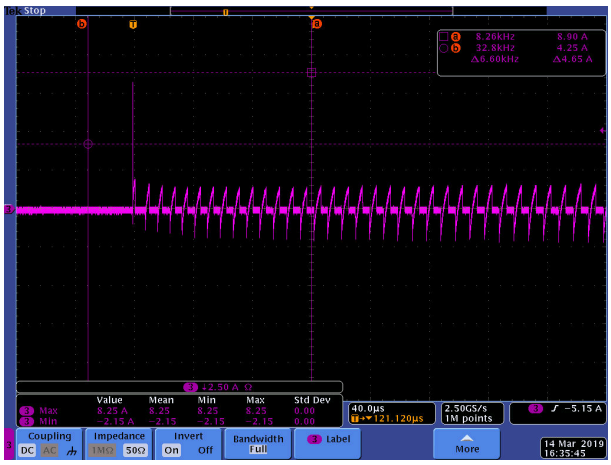

Figure 2-24. High Side MOS Current with 0.5 V Initial Voltage on LL/SS Pin

2.6 Burst Mode

Burst Mode Threshold (BMT), is an internal voltage threshold used to determine at what percentage of full load the device will enter/exit burst mode operation. The relationship between BMT and burst mode enter/exit load condition is dependent on the power stage and VCR capacitors. Typically, higher BMT means the device will enter/exit burst mode at a heavier load condition. From the system side, this typically leads to higher light load efficiency and higher output voltage ripple. In UCC25640x, BMT is a fully programmable parameter that can be used to optimize the light load efficiency and output voltage ripple.

2.6.1 Burst Patterns

UCC256403 and UCC256404 uses the burst pattern shown in Figure 2-25 with minimal 40 pulses where burst soft on and soft off are enabled. This burst soft-on and soft-off can effectively help to minimize the audible noise during burst mode operation.

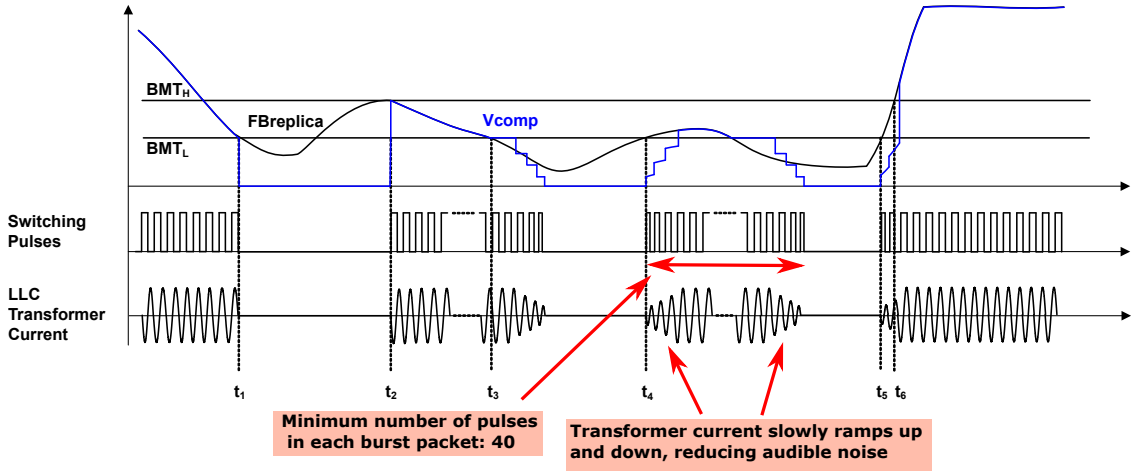

Figure 2-25. With Burst Soft On and Soft Off with Minimal 40 Pulses

UCC256402, UCC256402A, and UCC256404A uses the pattern shown in Figure 2-26 with 16 minimal pulses. This burst pattern helps to minimize the voltage ripple during the burst mode.

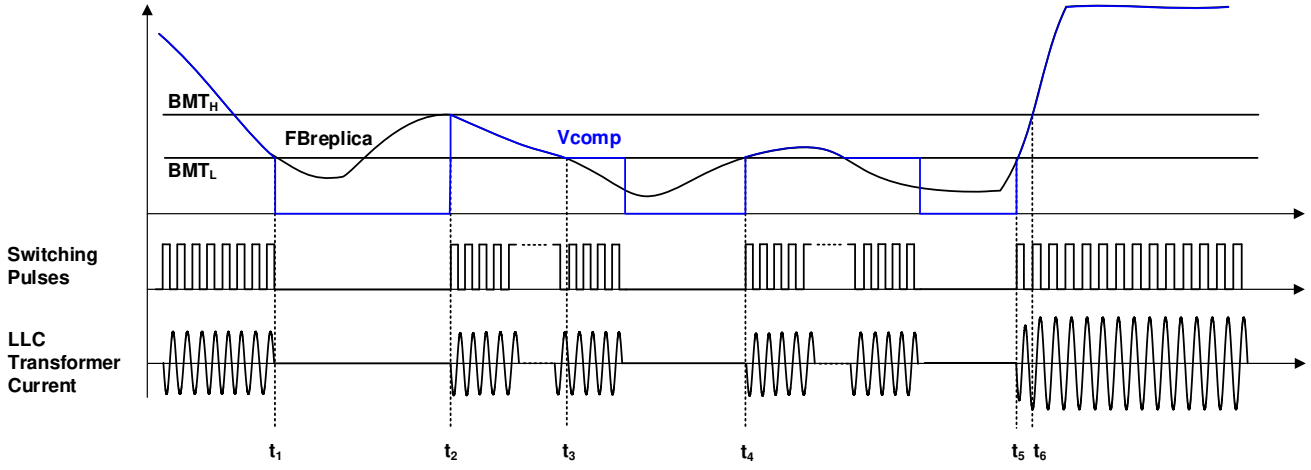

Figure 2-26. With No Burst Soft On and Soft Off with Minimal 16 Pulses

2.6.2 BMTL/BMTH Ratio Programming

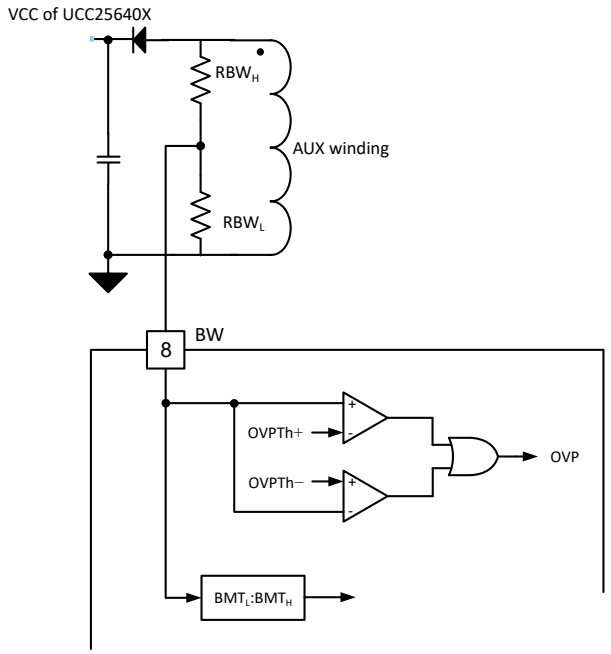

Figure 2-27. Internal Diagram and Typical Circuit of BW Pin of UCC25640X

$$R_{BW} = \frac{RBW_H \cdot RBW_L}{RBW_H + RBW_L} \tag{8}$$

- BW pin is multiplex for BMTL/BMTH ratio programming and Over voltage protection (OVP). This pin sources a fixed current of 54 uA before soft start to determine the BW voltage and it is internally compared with a series of voltage levels to determine the BMTL/BMTH ratio. It would take 2 ms to determine this BW pin voltage.
- In case if the capacitor is connected the BW pin to eliminate the high frequency noise, its value should be such that time constant of RBW and CBW much less than 2 ms of the proper programming.
- Based on the BW pin equivalent resistance (R_{BW} value as given in Equation 8), the ratio of BMTL and BMTH is determined as shown in the Table 2-1

Table 2-1. BMTL/BMTH value

Option	R_{BW}	BMTL/BMTH
1	> 24.7 k	0.95
2	17.1 k – 19.9 k	1
3	12.5 k – 13.6 k	0.9
4	9.02 k – 9.81 k	0.8
5	6.48 k – 6.85 k	0.6 (No Vssinit)
6	4.45 k – 4.73 k	0.6
7	2.42 k – 3.04 k	0.4 (Burst disabled)
8	Shorted	0.6

2.6.3 BMTH Generation

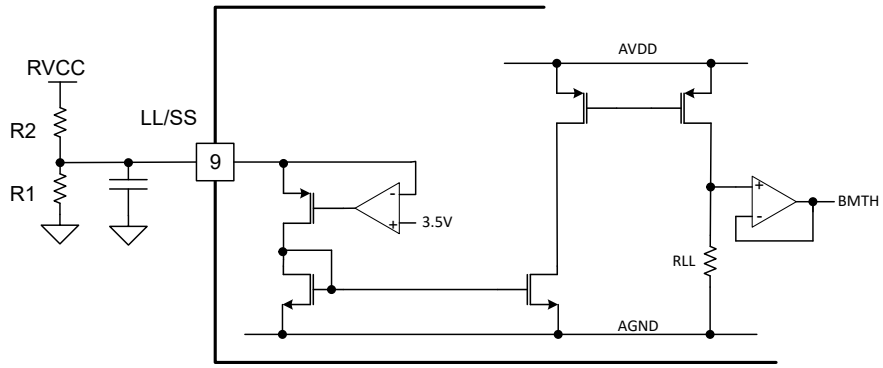

Figure 2-28. UCC25640x BMTH Programming Circuit

- Burst mode thresholds will be programmed after startup process is finished.
- Once the startup is finished, LL/SS pin is kept constant at 3.5 V.
- Current sinks to LL/SS pin is the current mirrored flowing through an internal RLL (100kOhm) and the voltage on the RLL is nothing but BMTH.
- The current flowing into the LL/SS pin is derived as

$$I_{LLSS} = \frac{RVCC - 3.5V}{R2} - \frac{3.5V}{R1} \tag{9}$$

- BMTH voltage is given by

$$BMTH = I_{LLSS} \cdot RLL = I_{LLSS} \cdot 100k\Omega \tag{10}$$

$$BMTH = \left(\frac{13V - 3.5V}{R2} - \frac{3.5V}{R1}\right) \cdot 100k\Omega \tag{11}$$

- Burst mode thresholds will be kept at a minimum value of 0.2 when R2 removed to limit the maximum operating switching frequency.

2.6.4 Interpreting BMTL and BMTH

- BMTL is the effective burst mode threshold (entering and exiting) from system level. BMTL and FBreplica are the inputs for the pick higher block.
- Internally, for digital state machine, BMTL is the burst mode entering threshold and BMTH is the burst mode exiting threshold. When Vcomp is between BMTL and BMTH, the switching pulses are continuous.
- ZCS protection disabled when Fbreplica is lower than BMTH. So BMTH can be adjusted to prevent nuisance ZCS protection.

2.6.5 Soft On or Off

- During the first 7 steps and last 7 steps of the burst packets (as shown in Figure 2-25), Vcomp uses a smaller value to generate ramped resonant current in UCC256403 and UCC256404 devices.
- Soft on or off is terminated when Fbreplica is higher than BMTH, to achieve good transient performance.

2.6.6 Operation when Burst Mode Disabled

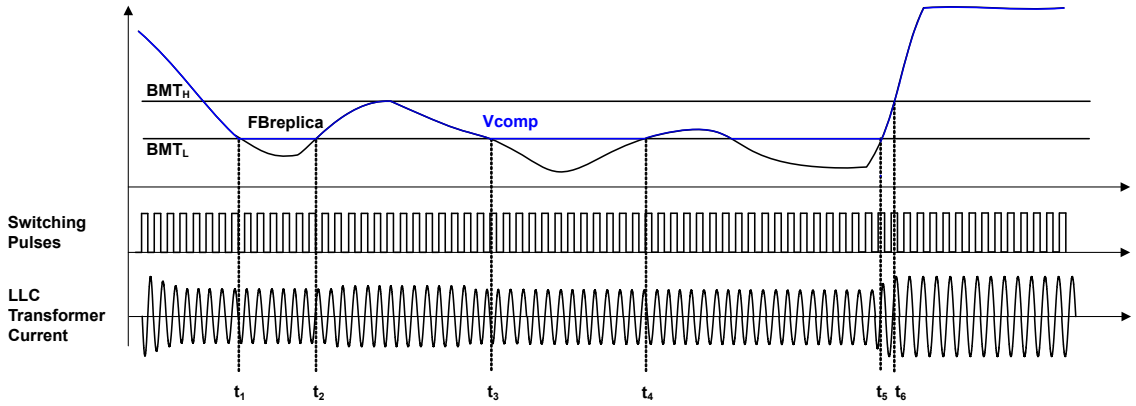

Figure 2-29. Switching Pattern with Burst Mode Disabled

- Figure 2-29 shows that, when the burst mode is disabled (using option 7 given in Table 2-1), switching pulses are not turned off even when the Fbreplica becomes lower than BMTL.
- BMTL becomes the effective maximum switching frequency limiter
- When burst mode is disabled, FBreplica needs to be higher than BMTL at steady state. Otherwise, LLC output voltage will lose regulation as it continues deliver more energy than what is demanded from the feedback. For a transient period, it is acceptable for FBreplica to be lower than BMTL.

2.6.7 Typical Waveforms

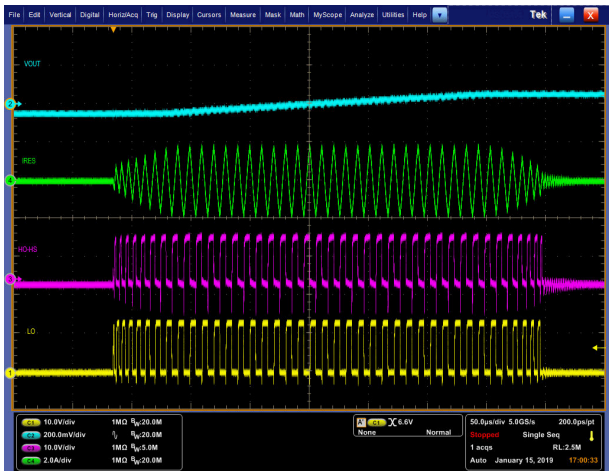

Figure 2-30. IC Version with Burst Soft On or Off enabled Ch1 – LO; Ch2 – VOUT; Ch3 – HO-HS; Ch4 – IRES; Zoomed in Version

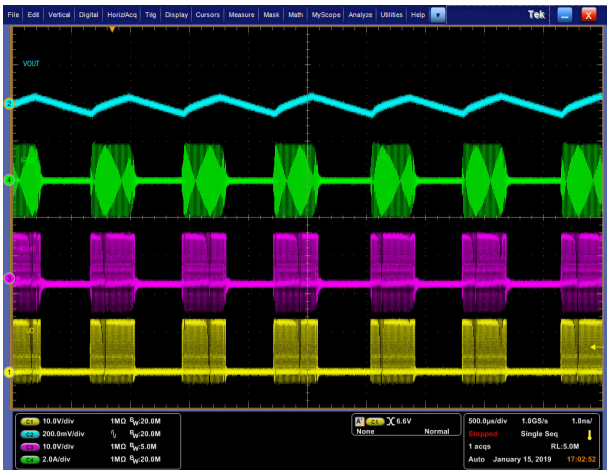

Figure 2-31. IC Version with Burst Soft On Off Enabled Ch1 – LO; Ch2 – VOUT; Ch3 – HO-HS; Ch4 – IRES; Zoomed out Version

- In Figure 2-30, we can observe that the resonant current slowly ramps up and ramps down due to the soft-on and soft-off introduced in UCC25640x. This burst mode soft-on and soft-off can effectively reduce the audible noise at standby operation.

2.7 Adaptive Dead Time Control

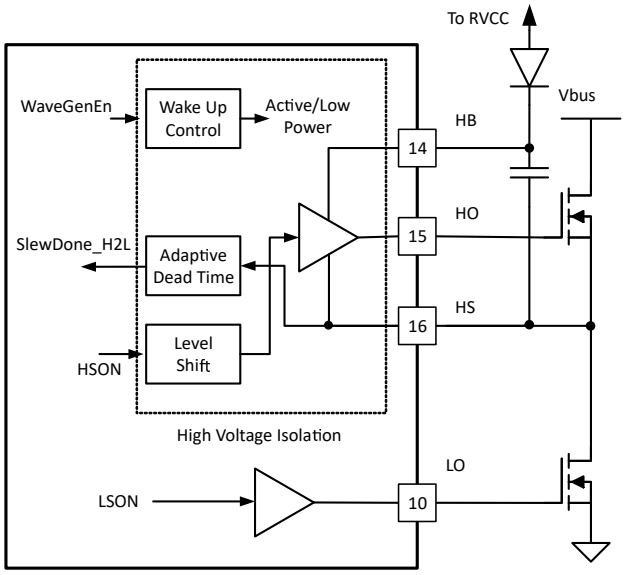

Figure 2-32. Adaptive Dead Time Control

- LO turns on when HS detects a slew rate change from high to low (During a switching transition, the slew rate rises up first and then drops back to zero) – indicating HS voltage reaches the minimal value. So, the dead time from HO to LO is automatically adjusted based on HS voltage.
- Minimal detectable slew rate is 0.1 V/ns (check when HS at 20 V).
- Dead time from LO to HO is copied from the previous HO to LO switching.

2.8 Fault Management

2.8.1 OCP Protection

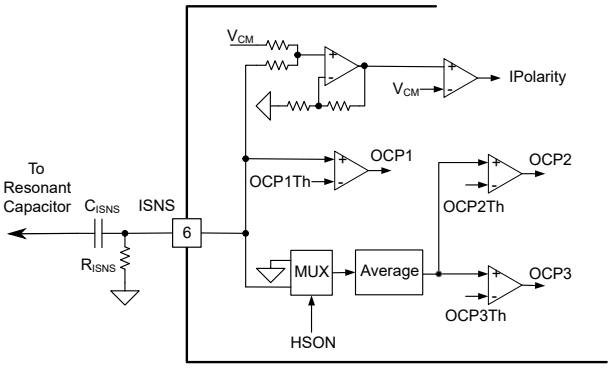

Figure 2-33. Over Current Protection (OCP) Protection

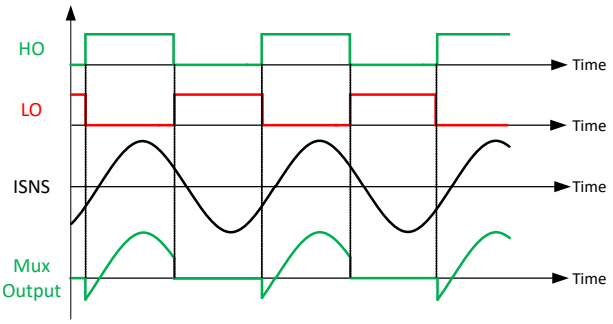

Figure 2-34. High Side Switch Current Extraction from ISNS Signal

- Resonant current is reconstructed as ISNS voltage using a differentiator connected to the resonant capacitor.
- OCP1 (OCP1Th: 4 V) is for output short circuit protection; it checks the magnitude of the resonant current.
- OCP2 (OCP2Th: 0.6 V) is for over-load protection; it checks the average DC input current. The time the average input current needs to stay above OCP2 threshold before OCP2 is triggered is 2 ms.
- OCP3 (OCP3Th: 0.43 V) is also for over-load protection but it has lower threshold value compared to OCP2, OCP1; it checks the average DC input current. The time the average input current needs to stay above OCP3 threshold before OCP3 is triggered is 50 ms.
- DC input current is reconstructed by capturing the current flowing through high side MOSFET.
- Internally, ISNS voltage is truncated when HO is high and then filtered to get the average dc value.

2.8.2 OCP Fault Typical Waveforms

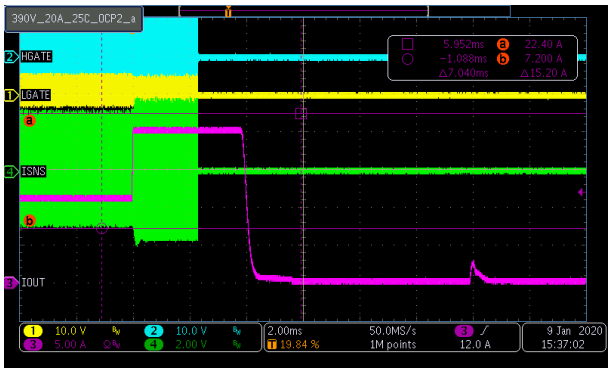

Figure 2-35. OCP 2: 2 ms

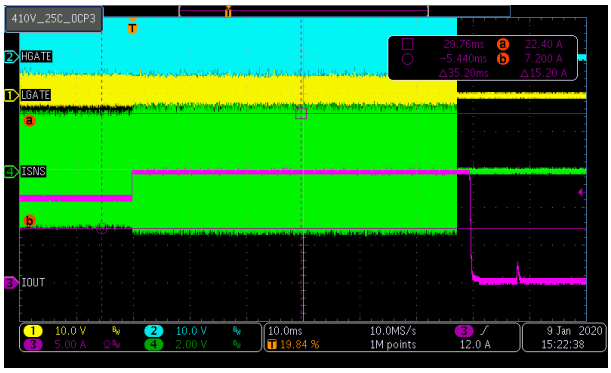

Figure 2-36. OCP 3: 50 ms

2.8.3 Over Voltage Protection using Bias Winding (BW OVP)

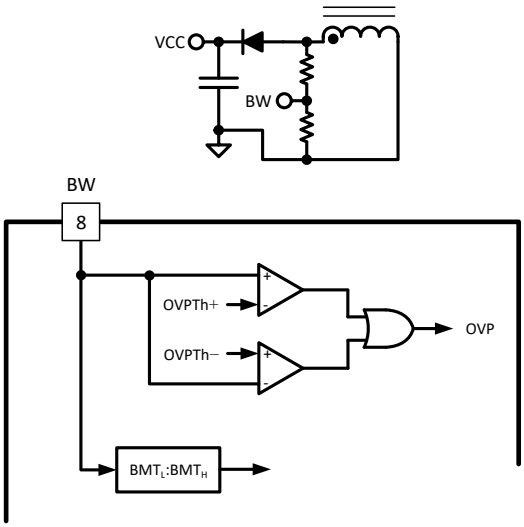

Figure 2-37. OVP Protection Using Auxiliary Winding

- Transformer bias winding can reflect the output voltage – the accuracy depends on if the bias winding coupled to the secondary side and also the load current.
- BW OVP is triggered after five consecutive cycles BW voltage crosses the thresholds (±4 V).

2.8.4 Restart or Latch

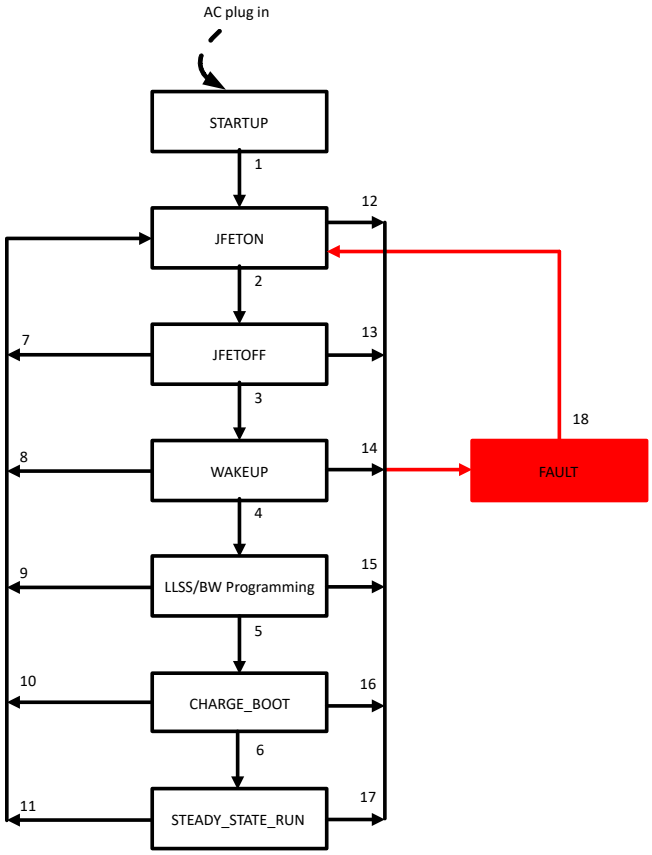

Figure 2-38. State Diagram for UCC25640x

- Over Temperature (OTP), Low DC Input Voltage (BLK UVLO), Over voltage at the DC Input (BLK OVP), RVCC UVLO will also get part into fault state
- For “restart” IC version, IC goes into fault state (gate turns off, RVCC shut down, etc) and stays in fault idle state for 1s, before entering JFETON.
- For “latch” IC version, IC goes into fault state and stay latched. VCC is supplied from HV pin and regulated at ~14.5 V.
- For external fault protection, pull down the BLK pin voltage.

2.9 ZCS Region Prevention Scheme

2.9.1 ZCS Effects

- Operating at Zero Current Switching (ZCS) region leads to the primary side MOSFET's bode diode conduction: Risk of damaging the MOSFET due to large current spike (Refer *22.3 Soft Switching in Fundamentals of Power Electronics*).
- Also, Gain-frequency relationship will be reversed.

2.9.2 ZCS Detection and Prevention and Disabling

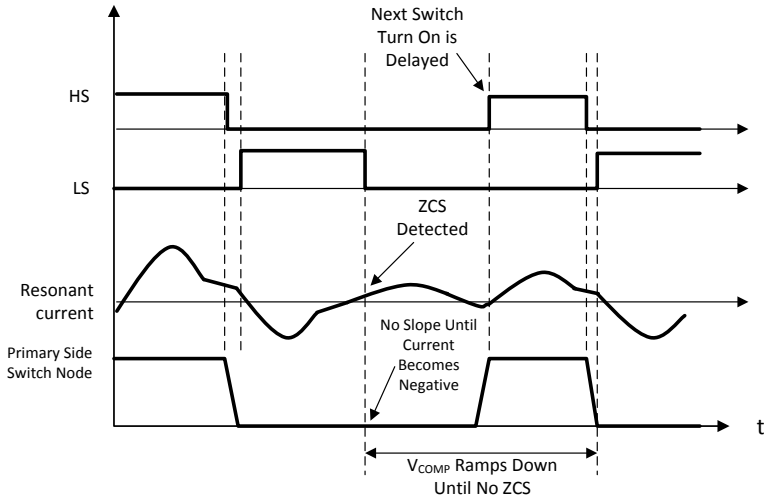

Figure 2-39. Timing Diagram of a ZCS Event

- ZCS is determined by looking for correct polarity on ISNS signal at high side gate and low side gate turn off edges.
- ZCS is detected:
  - If ISNS signal is positive at low side gate falling edge, or ISNS signal is negative at high side galling edge.
  - Next switch turn on delayed until correct Ipolarity is detected or maximum dead time of 150 us expires.
  - SS pin is pulled low to re-initiate a soft start to push system operating at higher switching frequency.
- Disable ZCS:
  - If FBreplica<BMTH this is when system is in light load, ZCS is disabled.

3 UCC25640x Power Up Guidelines and Debugging Notes

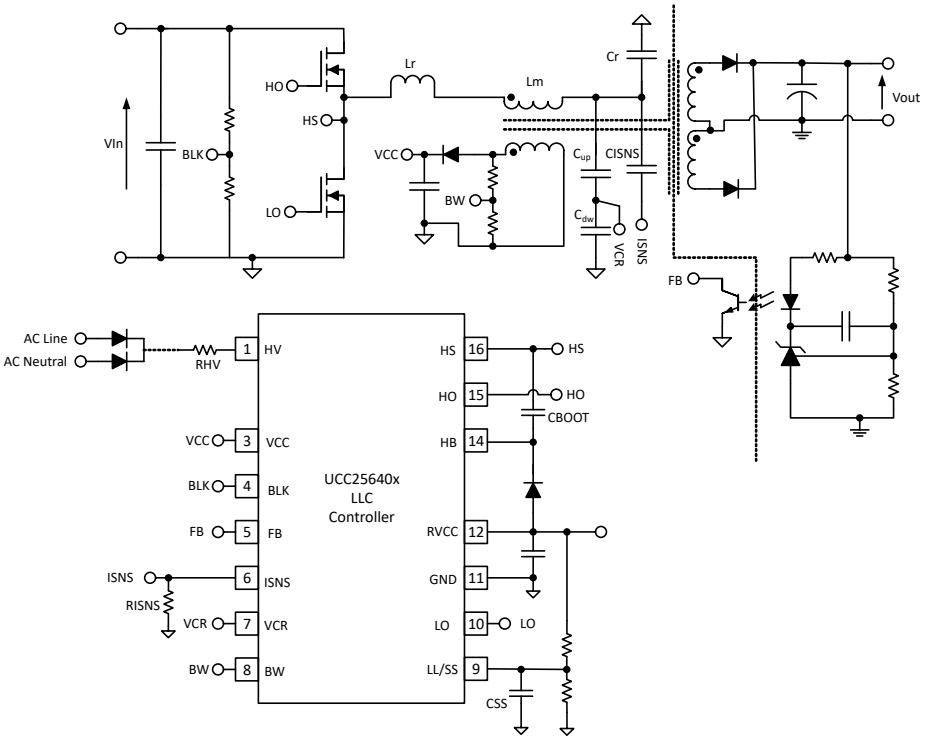

Figure 3-1. Application Schematic

3.1 Power Up Procedure

- Check the HV pin. Rectified AC or DC voltage should be available depending on the IC version.
- Check the VCC voltage. It needs to reach 26 V, to enable the RVCC. In case of UCC256403/403A VCC needs to reach 10.9 V to enable the RVCC. When BLK input reaches BLKStart threshold, softstart will be initiated.
- Check the RVCC voltage, it should start when VCC reaches 26 V (10.9V for UCC256403/403A), and should stay at 13-V constant. If RVCC goes up and down every 1s, it means that there is a fault condition.
- For the fault identification, check the BLK, ISNS, and BW pins for input voltage OVP and undervoltage protection (UVP), overcurrent protection (OCP), output OVP protections. Also check VCC and RVCC voltages for undervoltage protections.
- Check gate pulses. A typical LO pulse of 265 us is an indicator of system restart.
- Check FB pin voltage. If the FB pin is pulled low, the system will not start switching.

3.2 HV Pin

- When x-cap discharge is disabled, this pin can be connected to either rectified AC or DC.
- When x-cap discharge is enabled, this pin can only be connected to rectified AC. Connecting this pin to DC might not break the device, but the system will consume more power and might run into over temperature protection
- For debugging purpose, the current flowing into the HV pin can be measured by the voltage across the HV pin series resistors.

3.3 VCC Pin

- JFET is turned off when VCC reaches VccStartSelf (26 V) (402 and 404 devices) /VccStartSwitching threshold (10.9 V) (403 device).
- When VCC reaches VCCStartSelf, RVCC turns on.
- JFET is turned on when VCC drops below VCCReStartJfet (For 402, 404, it is 9.65 V).
- It is recommended to keep VCC above 14 V during normal operation to give RVCC enough headroom.

3.4 BLK Pin

- This pin has undervoltage protection.
- Only UCC256402A has overvoltage protection at this pin.
- For startup, the BLK voltage should be at least BLKStart.
- This pin is a high impedance node. The voltage divider lower resistor and the filtering cap should be put as close as possible to the pin.
- For external shut down, its recommended to pull the BLK pin low.

3.5 FB Pin

- The voltage on this pin does not move during normal operation (unless the optocoupler is saturated), so adding a capacitor from the FB pin to ground does not add a pole to the system.
- Adding a resistor from the FB pin to ground can set a maximum clamp on Vcomp level. This can be used for maximum power level, maximum input current, and minimum frequency clamp.
- Voltage at this pin varies depending on the current being sunk:
  - If there is no current sunk at this pin, voltage at this pin will be at 7 V.
  - If the current drawn is below FB pin max source current (164 uA for 402 and 404 devices, 246 uA for 403), FB voltage will be close to 5.6 V.
  - If the current drawn is more than FB pin maximum source current (164 uA for 402 and 404 devices, 246 uA for 403), FB voltage will be 0.

3.6 ISNS Pin

- Use < 500-Ω resistor on the ISNS pin.
- Too much low pass filtering on ISNS can result in a delay in resonant current polarity sensing and error in overcurrent protection.
- Inside the ISNS pin, input current is reconstructed and averaged.
- OCP1 = 4 V during normal operation and during soft start it is 5 V, OCP2 = 0.6 V, OCP3 =0.43 V
- To set OCP level:
  - Calculate the desired input current level (in amps) for OCP.
  - Set the desired current sense ratio by adjusting RISNS and CISNS.
- Adding some low pass filtering on ISNS can help avoid OCP1 tripping during the first few switching cycles also it helps to avoid unwanted ZCS tripping.
- To avoid OCP fault at startup:
  - Reduce the soft start offset voltage or reduce the VCR lower capacitor or increase the LL/SS capacitor. These three methods can be used to increase the initial switching frequency during startup. Relaxing the OCP threshold also helps to avoid OCP at startup.

3.7 VCR Pin

- The ratio between Cup and Cdw on the VCR pin should be determined by the maximum peak-to peak resonant capacitor voltage waveform. These capacitor values needs to be chosen such that the maximum VCR pin voltage peak to peak (occurs at the minimum operating input voltage and maximum load current) should be always less than 6 V.
- Lower Cdw results in a higher switching frequency at a given Vcomp level.
- The internal 2-mA current source is on during dead time. If VCR voltage rails out to 0 V or +7 V, it means that the dead time is very long. In case of ZCS detection, maximum dead time would be 150 us. In case of missing slew rate detection, maximum dead time would be 1.1 us. The VCR pin voltage can also rail out during burst. This is usually caused if the boot capacitor too small and the high-side gate does not turn on.

3.8 BW Pin

- The voltage level on both the half cycles on BW is sampled and compared with OVP comparator.
- OVP = +/-4 V
- Add necessary low pass filtering on this pin if there are high spikes on the BW signal.
- OVP can be disabled by removing upper resistance of the BW voltage sensing resistors. In this case lower resistor decides the BMTL/BMTH ratio.
- If this pin shorted to ground, BMTL/BMTH is 0.6.

3.9 LL/SS Pin

- This pin should have a small ground loop.
- Removing the top resistor on the resistor divider will set the burst mode threshold to the minimum value: 0.2 V. However, removing this top resistor might cause nuisance ZCS detection at lighter loads. Also, this process prevents the buildup of voltage on the soft start pin before the LLC starts switching.
- After the startup, this pin voltage will be maintained at 3.5 V.
- If the ZCS is detected, the voltage on LL/SS pin will go down from 3.5 V to ramp up the switching frequency.

3.10 LO Pin

- A long LO pulse at the beginning of switching is used to charge the boot capacitor.

3.11 RVCC Pin

- Whenever a fault happens (except ZCS fault and boot UVLO), RVCC will be shut off and the system will retry startup after 1s.
- RVCC supplies the gate driver and various internal circuits.
- During the burst mode, need to make sure there is enough VCC voltage such that RVCC is well regulated.

3.12 HS, HO, HB Pins

- High-side gate has UVLO protection.
- If one high-side pulse is missing, it usually means that the boot voltage is not enough.
- System state machine will not react to boot UVLO protection.

4 References

For additional references, see:

- Texas Instruments, *UCC25640x LLC Resonant Controller with Ultra-Low Audible Noise and Standby Power* data sheet.
- Texas Instruments, *UCC25640x Design Calculator*.
- Texas Instruments, *UCC25640x Simplis Model*.
- Texas Instruments, *Designing an LLC Resonant Half-Bridge Power Converter* .

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