Application Note

Stability Analysis and Design of Internally-Compensated Peak Current Mode TPS62933 - Part II: How to Select the Feedforward Capacitor

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ABSTRACT

This application note is part two of a two-part series:*Stability Analysis and Design of Internally Compensated Peak Current Mode TPS62933*. In *Part I: How to Select the Output Capacitor*, the output capacitor selection method is proposed to ensure the stability of the TPS62933, an internally-compensated, peak current-mode, buck converter. On this basis, the method to select a feedforward capacitor (C_{ff}) is further introduced in this application note. First, the necessity to add C_{ff} for high output voltage applications is introduced. Next, the impacts of C_{ff} on converter phase margin improvement is analyzed. Combined with the loop feature of TPS62933, a method for stability enhancement with C_{ff} is then proposed. Compared with conventional C_{ff} selection method, the bode plot without C_{ff} is not needed for the design, which makes it more applicable for the overall system design. Finally, an application design example is given to verify the effectiveness of the proposed method.

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Trademarks

1 Introduction

Peak current mode (PCM) control is widely used in buck converters due to the advantages such as good dynamic performance and easy compensation. By using internal compensation with PCM control, the TPS62933 device further reduces the customer-application BOM, which helps to reduce the solution size and design complexity. For common applications, components are selected based on the recommended table and design applications are quickly implemented(1). Methods for choosing output capacitors in applications with *large* output capacitors are detailed in *Stability Analysis and Design of Internally-Compensated Peak Current Mode TPS62933 - Part I: How to Select the Output Capacitor*.

However, from the results derived in *Part I: How to Select the Output Capacitor*, the maximum output capacitance value under the stability constraint is inversely proportional to the output voltage, which makes it difficult to select a large capacitance in high output voltage applications. This difficulty leads to the contradiction between voltage ripple, voltage noise, and a stable design. This document first explains the root cause of the contradiction based on theoretical analysis. Then the effects of feedforward capacitor C_{ff} on the loop are introduced. With a pair of introduced zero and pole in the loop, the phase margin can be improved for stability, which enlarges the range of output capacitance selection in high output voltage applications.

2 C_{ff} in High-Output Voltage Internally Compensated PCM Buck Converter

Loop Response Considerations in Peak Current Mode Buck Converter Design introduces the loop response model of PCM mode buck converters, as shown in Figure 2-1. The initial loop gain slope of the PCM converter is 0, it changes from 0 to –20 dB/dec at the initial pole frequency f_{P1_EA}. At pole f_{P_OUT}, the loop gain slope changes to –40 dB/dec. With the compensation of zero f_{Z_EA}, the gain slope becomes –20 dB/dec, and the gain curve crosses 0 dB with a –20-dB/dec slope. That slope can normally bring sufficient phase margin for the converter.

The TPS62933 has internal compensation, the f_{P1_EA}, f_{Z_EA}, and f_{P2_EA} are the frequencies of poles and zero generated by the internal compensation and fixed as Equation 1:

$$\begin{cases} f_{P1\_EA}=1.2\text{Hz} \\ f_{P2\_EA}=275\text{kHz} \\ f_{Z\_EA}=10.6\text{kHz} \end{cases} \tag{1}$$

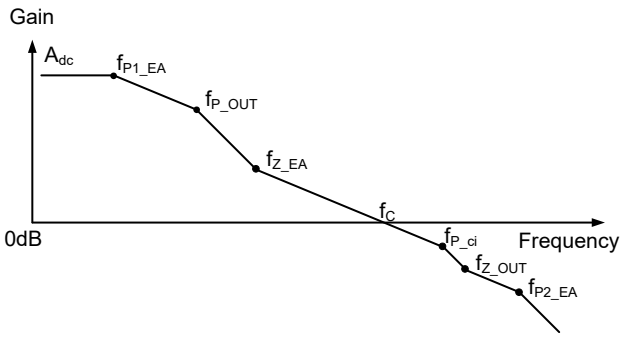

Figure 2-1. Bode Plot of PCM Buck Converter Open Loop Response

The DC gain A_{dc} is related with output current. The A_{dc} of TPS62933 can be expressed as:

$$A_{dc}=\frac{352000}{I_{out}} \tag{2}$$

f_{P_OUT} is the frequency of the pole formed with the output capacitance and loading, which can be expressed as:

$$f_{P\_OUT}=\frac{1}{2\pi(R_{ESR}+R_O)C_O} \tag{3}$$

The expressions of A_{dc} and f_{P_OUT} include the output current I_{out} and the load resistance R_O, respectively.

For the application with a fixed load resistance R_O, when output voltage increases, output current increases and the DC gain A_{dc} decreases. As Figure 2-2 illustrates, this causes the bandwidth decrease. If the zero f_{Z_EA} becomes out of bandwidth, the –40 dB/decade gain slope occurs at gain crossover frequency and could cause insufficient phase margin.

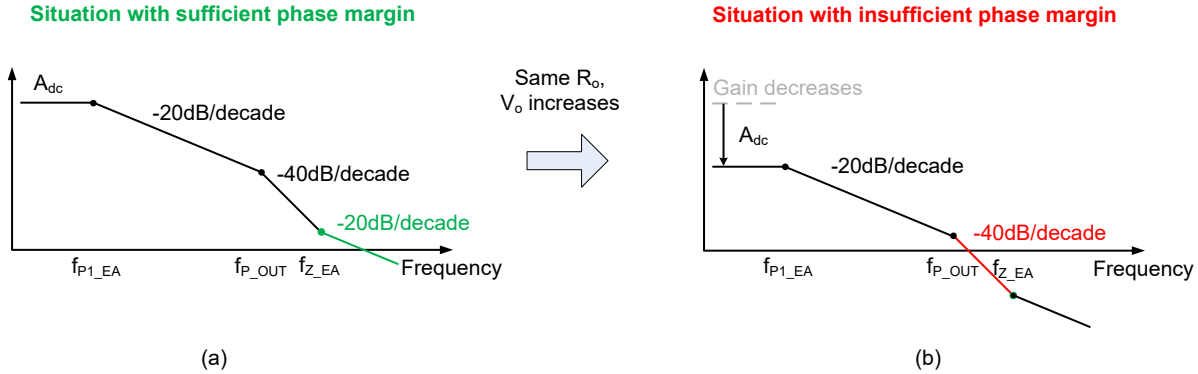

Figure 2-2. Loop Gain of TPS62933 With Fixed Load Resistance R_O (a) Low V_O With –20 dB/dec Crossing (b) High V_o With –40 dB/dec Crossing

For converters with fixed output current I_{out}, the equivalent output resistance R_O increases with increasing output voltage, which makes the frequency f_{P_OUT} in Equation 3 decrease. As Figure 2-3 shows, that results in bandwidth decrease and could also cause the compensated zero f_{Z_EA} to become out of bandwidth. The –40 dB/decade gain slope also occurs at gain crossover frequency and could cause insufficient phase margin.

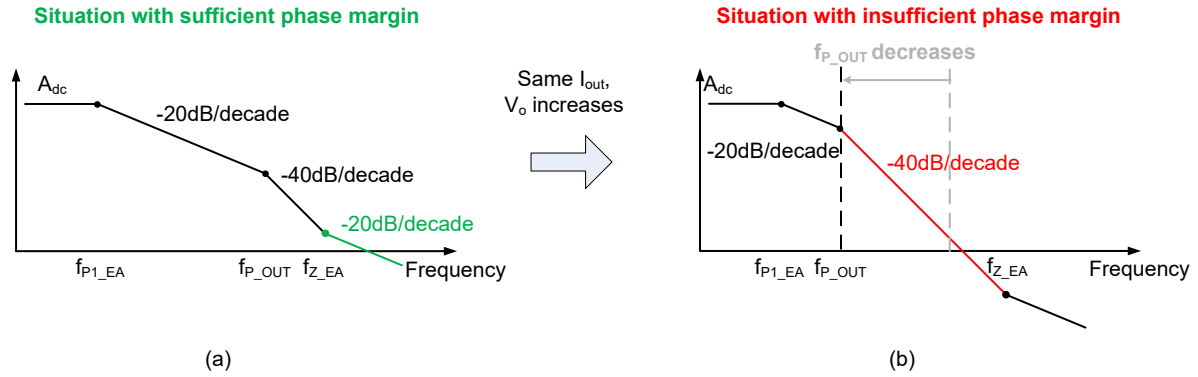

Figure 2-3. Loop Gain of TPS62933 With Constant Output Current I_{out} (a) Low V_o With –20 dB/dec Crossing (b) High V_o With –40 dB/dec Crossing

Above all, increasing output voltage tends to cause the internal peak-current-mode converter to be unstable, which makes it hard to design an application with high output voltage.

Since the pole frequency f_{P_OUT} is inversely proportional to the output capacitance C_o, reducing C_o can help to increase the frequency f_{P_OUT}, making the zero f_{Z_EA} inside bandwidth again and bringing enough phase margin. Just as the derived output capacitance range with Equation 4 in *Part I*, the maximum output capacitance is reduced by increasing the output voltage V_O for stability. But reducing output capacitance has many side effects, such as poor transient performance, larger ripple, and larger noise.

$$C_o < \frac{5.98\times10^{-4}}{I_{out}R_{ESR}+V_O} \tag{4}$$

This analysis proves that in high-voltage applications, there is a contradiction between performance and stability in an internally-compensated PCM buck converter. Adding a feedforward capacitor C_{ff} can help solve the issue at this condition.

3 Effects of C_{ff} on the Loop

The *Optimizing Transient Response of Internally Compensated dc-dc Converters With Feedforward Capacitor* application report details the effects of adding a feedforward capacitor in the feedback divider. Figure 3-1 shows feedback divider including C_{ff}.

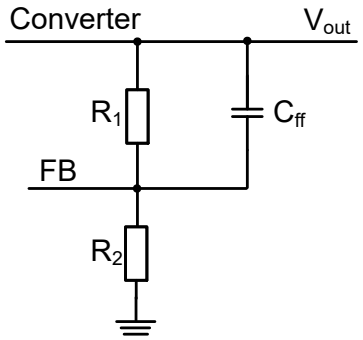

Figure 3-1. Scheme of Feedback Divider Including Feedforward Capacitor

C_{ff} introduces a pair of zero and pole in the converter loop. The frequency of the introduced zero and pole are:

$$f_z = \frac{1}{2\pi R_1 C_{ff}} \quad (5)$$

$$f_p = \frac{1}{2\pi C_{ff}}\left(\frac{1}{R_1} + \frac{1}{R_2}\right) \quad (6)$$

Figure 3-2 shows the effects of the zero and pole introduced by C_{ff}.

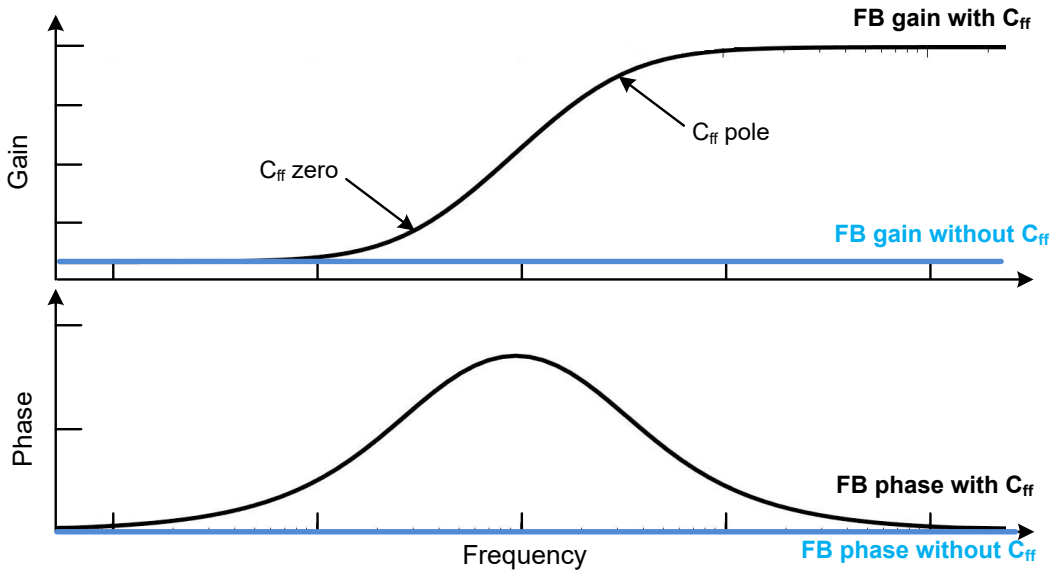

Figure 3-2. Bode Plot of Feedback Divider Transfer Function Including C_{ff}

C_{ff} has both effects on the loop gain and phase. The loop gain is increased to enlarge bandwidth which benefits transient response, and the phase is also boosted to increase the phase margin for system stability.

In application notes such as *Optimizing Transient Response of Internally Compensated dc-dc Converters With Feedforward Capacitor*, some methods have been proposed to use C_{ff} for phase margin enhancement. But in those methods, the bode plot results without C_{ff} are always needed to get the recommended C_{ff} value. The C_{ff} selecting method is more applicable in the solution validation process but not in the application design process.

A new method to choose C_{ff} is proposed in this application report. The bode plot results without C_{ff} are not needed to get the recommended C_{ff} value in this method, which makes it more applicable in TPS62933 application design.

4 Method for Selecting C_{ff}

This method is implemented by letting the loop gain cross 0 dB with –20 dB/dec slope. To be noted, –20 dB/dec gain at 0 dB is not a necessary condition for stability. So this method just provides an allowable range for C_{ff} and it does not mean the converter will be unstable if C_{ff} exceeds this range.

For the case as Figure 4-1(a) shows, when the EA zero frequency f_{Z_EA} is larger than bandwidth, the C_{ff} zero f_z can be added inside bandwidth, then the loop gain *can* cross 0 dB with –20 dB/dec, as Figure 4-1(b) shows.

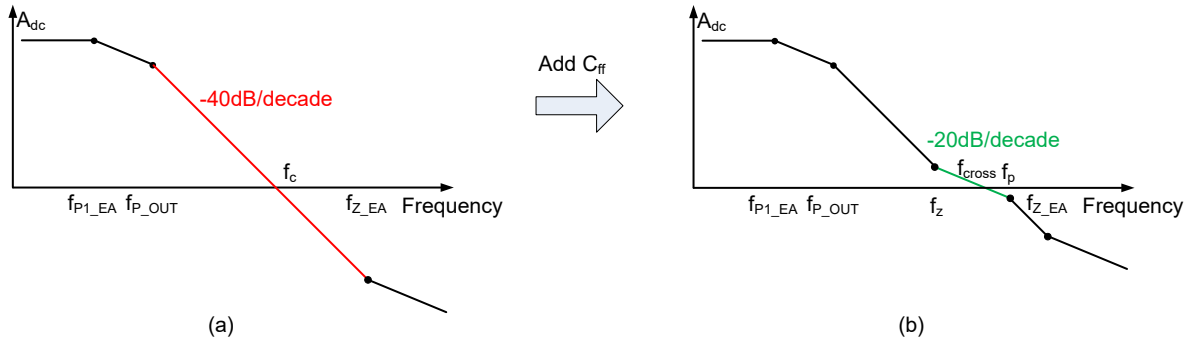

Figure 4-1. Correct Method to use C_{ff} by Only Adding C_{ff} Zero Inside Bandwidth

As the case in Figure 4-2 shows, the zero and pole introduced by C_{ff} are both added inside bandwidth and the system stability can still be ensured. Although the slope of loop gain becomes –40 dB/dec again after the pole f_p, the increase in loop gain with C_{ff} makes the bandwidth increase and the f_{Z_EA} becomes smaller than the bandwidth. A –20-dB/dec crossing is achieved and the system has enough phase margin.

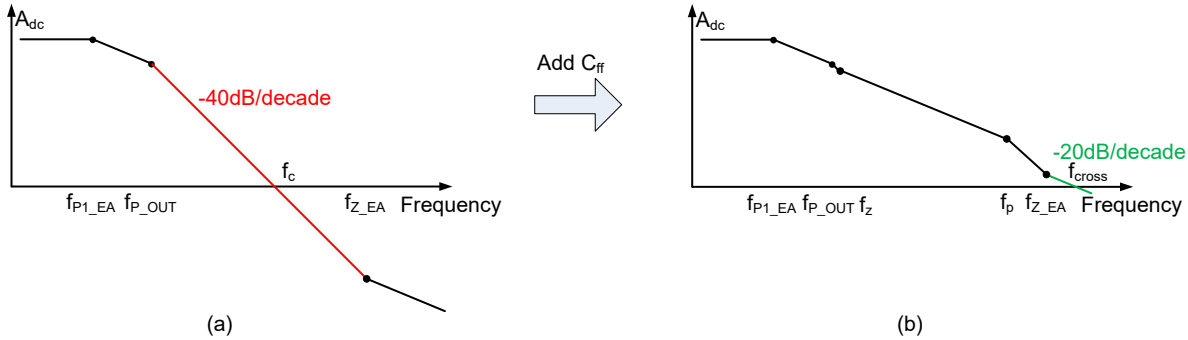

Figure 4-2. Correct Method to use C_{ff} by Adding Both the C_{ff} Zero and Pole Inside Bandwidth

As the case in Figure 4-3 shows, both the zero and pole introduced by C_{ff} are inside bandwidth, but the EA zero frequency f_{Z_EA} is still larger than the bandwidth. At this condition, the loop gain will still cross 0 dB with –40 dB/dec, which cannot ensure the system phase margin.

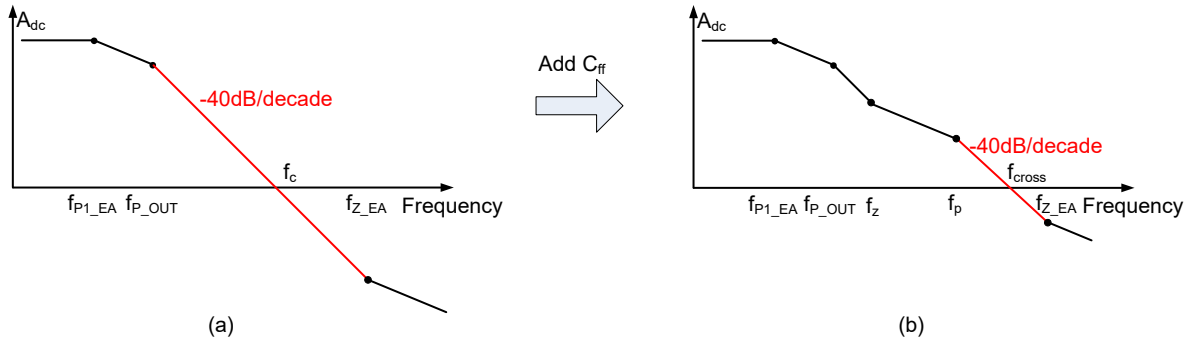

Figure 4-3. Incorrect Method to use C_{ff} by Adding Both the C_{ff} Zero and Pole Inside Bandwidth

Therefore, the two restrictions deduced to achieve a stable state with –20 dB/dec crossing after adding feedforward capacitor are (1) $f_z < f_c$, and (2) avoiding the condition as exhibited in Figure 4-3. f_c is the gain crossover frequency when not adding C_{ff}.

The expression of f_c has already been derived in *Part I*, as shown in Equation 7.

$$f_c = f_{P\_OUT}\sqrt{A_{P\_OUT}} = \sqrt{A_{dc} f_{P\_OUT} f_{P1\_EA}} \tag{7}$$

With the restriction $f_z < f_c$, the low limit of C_{ff} is obtained based on Equation 5 and Equation 7:

$$C_{ff} > \frac{\sqrt{C_O(V_O + I_{out}R_{ESR})}}{1629R_1} \tag{8}$$

This equation corresponds to the limit for restriction 1. Since Equation 9 corresponds to the condition as Figure 4-3(b), restriction 2 to avoid that condition corresponds to Equation 10.

$$20\lg(A_p) > 0\text{dB} \quad \text{and} \quad f_{Z\_EA} > f_{cross} \tag{9}$$

$$20\lg(A_p) \le 0\text{dB} \quad \text{or} \quad f_{Z\_EA} \le f_{cross} \tag{10}$$

where A_p is the amplitude of gain at f_p.

To get the expressions of A_p and f_{cross}, first determine the relation between gain and frequency as Equation 11, Equation 12, and Equation 13.

$$\frac{20\lg(A_{P\_OUT}) - 20\lg(A_z)}{\lg(f_{P\_OUT}) - \lg(f_z)} = -40\text{dB/decade} \tag{11}$$

$$\frac{20\lg(A_z) - 20\lg(A_p)}{\lg(f_z) - \lg(f_p)} = -20\text{dB/decade} \tag{12}$$

$$\frac{20\lg(A_p) - 0}{\lg(f_p) - \lg(f_{cross})} = -40\text{dB/decade} \tag{13}$$

Next, the expressions of A_p and f_{cross} as Equation 14 and Equation 15 are determined.

$$A_p = \frac{A_{P\_OUT} f_{P\_OUT}^{\ 2}}{f_z f_p} \tag{14}$$

$$f_{cross} = f_p \sqrt{A_p} \tag{15}$$

Substituting expressions for A_{P_OUT}, f_{P_OUT}, f_z, and f_p into Equation 14 and Equation 15, then Equation 16 is calculated as the equation for restriction 2 based on Equation 10, Equation 14, and Equation 15.

$$C_{ff} \le \sqrt{\frac{C_O(R_1+R_2)(V_O+I_{out}R_{ESR})}{844800\pi R_1^{\ 2} R_2}} \text{ or } C_O \le \frac{R_1+R_2}{1670(V_O+I_{out}R_{ESR})R_2} \tag{16}$$

Combining Equation 8 for restriction 1 and Equation 16 for restriction 2, Equation 17 and Equation 18 are the limits for C_{ff}.

$$C_{ff} > \frac{\sqrt{C_O(V_O+I_{out}R_{ESR})}}{1629R_1}, \quad \text{if } C_O \le \frac{R_1+R_2}{1670(V_O+I_{out}R_{ESR})R_2} \tag{17}$$

$$\frac{\sqrt{C_O(V_O+I_{out}R_{ESR})}}{1629R_1} < C_{ff} \le \sqrt{\frac{C_O(R_1+R_2)(V_O+I_{out}R_{ESR})}{844800\pi R_1^{\ 2} R_2}}, \text{ if } C_O > \frac{R_1+R_2}{1670(V_O+I_{out}R_{ESR})R_2} \tag{18}$$

5 Experimental Verification for TPS62933

Using the typical application as an example, V_{in} = 24 V, V_{out} = 5 V, I_{out} = 3 A, f_{sw} = 500 kHz, L = 6.8 µH. For the voltage divider resistance, R_1 = 52.5 kΩ and R_2 = 10 kΩ.

With the method demonstrated in *Part I*, the calculated output capacitance upper limit is 106 µF without feedforward capacitor. Here 20 × C3216X5R1V226M160AC capacitors are selected for lower voltage ripple and better transient performance, which equals to about 264-µF C_o effective value, which is much higher than the 106 µF upper limit without C_{ff}.

This example has been validated on the TPS62933EVM. C3216X5R1V226M160AC (22 µF) and CGA5L1X7R1H106K160AC (10 µF) are selected as C_o, the effective value of C3216X5R1V226M160AC is about 13.2 µF when biased at 5 V, the effective value of CGA5L1X7R1H106K160AC is about 9.4 µF.

Since 20 × parallel capacitors are used, the ESR of output capacitors can be ignored. With Equation 17 and Equation 18, the range of C_{ff} as C_{ff} > 425 pF, is calculated. So, 470 pF C_{ff} is selected for the application.

Figure 5-1 shows the bode plot test results with added 470 pF C_{ff}. The phase margin is boosted to 83.464 degrees, which validates the effectiveness of the proposed method. See more validation results in Appendix A.

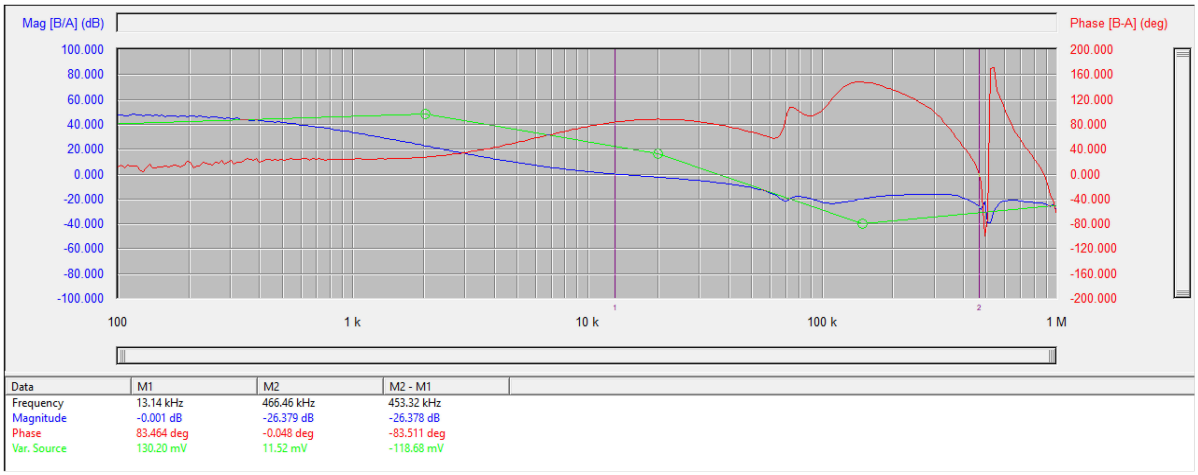

Figure 5-1. Bode Plot With the Selected Feedforward Capacitor

6 Summary

A selection method for feedforward capacitors is proposed in this application note for TPS62933, based on loop stability analysis. First, the necessity of adding C_{ff} in an application with high output voltage is analyzed. Then the impacts of the C_{ff} on the converter loop is introduced and a method to choose C_{ff} for stability is proposed by ensuring –20 dB/dec gain slope at gain crossover frequency. Compared with previous methods, the bode plot test results without C_{ff} are not needed to get recommended C_{ff} value, which makes the method more applicable in application design. The proposed methods expressed in this application note are verified by experiment.

7 References

1. Texas Instruments, *TPS62933 3.8-V to 30-V, 3-A Synchronous Buck Converter in SOT583 Package* Data Sheet
2. Texas Instruments, *Loop Response Considerations in Peak Current Mode Buck Converter Design* Application Report
3. Texas Instruments, *Optimizing Transient Response of Internally Compensated dc-dc Converters With Feedforward Capacitor* Application Report.

A Validation Results for the Proposed Method

Table A-1 details the validation of feedforward capacitance.

Table A-1. Validation Results

V_{IN} (V)	V_{OUT} (V)	f_{SW} (kHz)	L_{choose} (µH)	High Limit C_O (µF) Without Cff	C_{choose} (µF)	C_{ff} limit	C_{ff} choose (pF)	PM_{bench} (deg)
24	5	500	6.8	106	20 × 22 µF ($C_{effective}$: 264 µF)	C_{ff} > 425 pF	470 pF	83.464
24	5	1200	3.3	119.6	20 × 22 µF ($C_{effective}$: 264 µF)	C_{ff} > 425 pF	470 pF	86.143
24	12	500	12	40.7	20 × 22 µF ($C_{effective}$: 98.5 µF)	C_{ff} > 402 pF	470 pF	102.6

For 5 V V_{out}, R_{upper} (R_1) is 52.5 kΩ and R_{lower} (R_2) is 10 kΩ.

For 12 V V_{out}, R_{upper} (R_1) is 52.5 kΩ and R_{lower} (R_2) is 3.75 kΩ.

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