Application Note

UCC28782 Practical Design Guidelines

ABSTRACT

This application note provides system design guidelines for UCC28782 ACF controller. The process for optimizing certain ACF design parameters such as ACF and IC key function introduction and design SOP, check list, and transformer design. The application note also provides several useful tools and reference designs, to refer these document to design UCC28782 easily.

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Trademarks

1 Introduction

The UCC28782 is a transition-mode (TM) active clamp flyback (ACF) controller, equipped with advanced control schemes, to enable significant size reduction of passive components, for higher power density and higher average efficiency. The control law is optimized for Silicon (Si) and Gallium Nitride (GaN) power FETs in a half-bridge configuration and is capable of driving high-frequency AC/DC converters up to 1.5 MHz. The zero voltage switching (ZVS) control of the UCC28782 is capable of auto-tuning the on-time of a high-side clamp switch (QH) by using a unique loss less ZVS sensing network connected between the switch-node voltage (VSW) and SWS pin. The ACF controller is designed to adaptively achieve targeted full-ZVS or partial-ZVS conditions for the low-side main switch (QL) with minimum circulating energy over wide operating conditions. Auto-tuning eliminates the risk of losing ZVS due to component tolerance, input/output voltage changes, and temperature variations, since the QH on-time is corrected cycle-by-cycle.

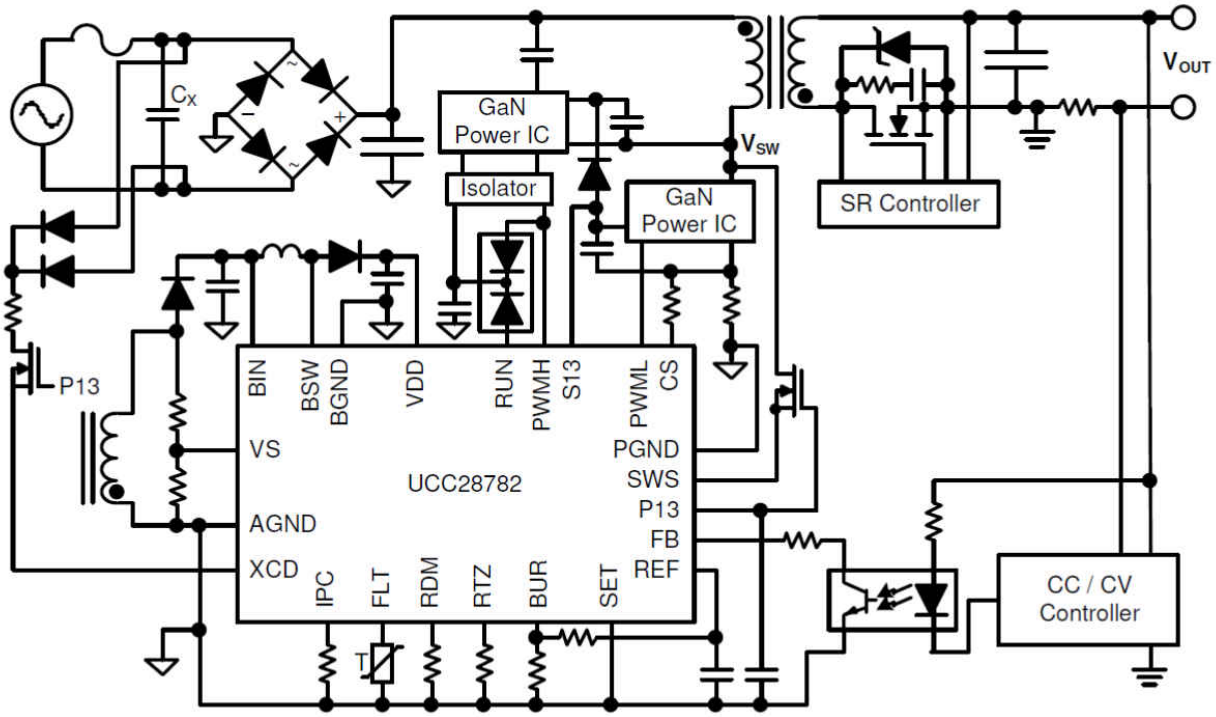

Figure 1-1. Simplified Type Circuit

2 Control Law across Entire Load Range

UCC28782 contains six modes of operation summarized in Table 2-1. Starting from heavier load, the AAM mode forces PWML and PWMH into complementary switching with ZVS tuning enabled. ABM mode generates a group of PWML and PWMH pulses as a burst packet, and adjusts the burst off-time to regulate the output voltage. At the same time, the burst frequency variation is confined above 20kHz by adjusting the number of PWML and PWMH pulses per packet to mitigate audible noise and reduce burst output ripple. In LPM, SBP1, and SBP2 modes, PWMH and the ZVS tuning loop are disabled, so the converter operates in valley-switching. The survival mode is to maintain V_{VDD} higher than $V_{VDD(OFF)}$ in a long burst off time, and also performs the clamping capacitor balancing function to reduce the voltage stress of the secondary-side rectifier .

Table 2-1 and Figure 2-1 also show the frequency and power level at each mode, so it helps to understand the mode operation.

Table 2-1. Functional Modes

	MODE	OPERATION	PWMH	ZVS
AAM	Adaptive Amplitude Modulation	ACF operation with PWML and PWMH in complementary switching	Enabled	Yes
ABM	Adaptive Burst Mode	Variable $F_{BUR} > F_{BUR(LR)}$, ACF operation in complementary switching	Enabled	Yes
LPM	Low Power Mode	Fix $F_{BUR} \approx F_{LPM}$, valley-switching	Disabled	No
SBP1	First Standby Power Mode	Variable F_{BUR} between $F_{SBP2(LR)}$ and $F_{SBP2(UP)}$, valley-switching	Disabled	No
SBP2	Second Standby Power Mode	Variable $F_{BUR} < F_{SBP2(UP)}$ as $V_{BUR} < 0.9$ V; Variable $F_{BUR} < F_{SBP2(LR)}$ as $V_{BUR} > 0.9$ V; Both are in valley-switching	Disabled	No
INT_STOP	Survival Mode	When $V_{VDD} < V_{VDD(OFF)} + V_{VDD(PCT)}$, a series of PWML pulses followed by a long PWMH pulse is generated	Enabled in the lastswitching cycle of a survival-mode burst packet	No

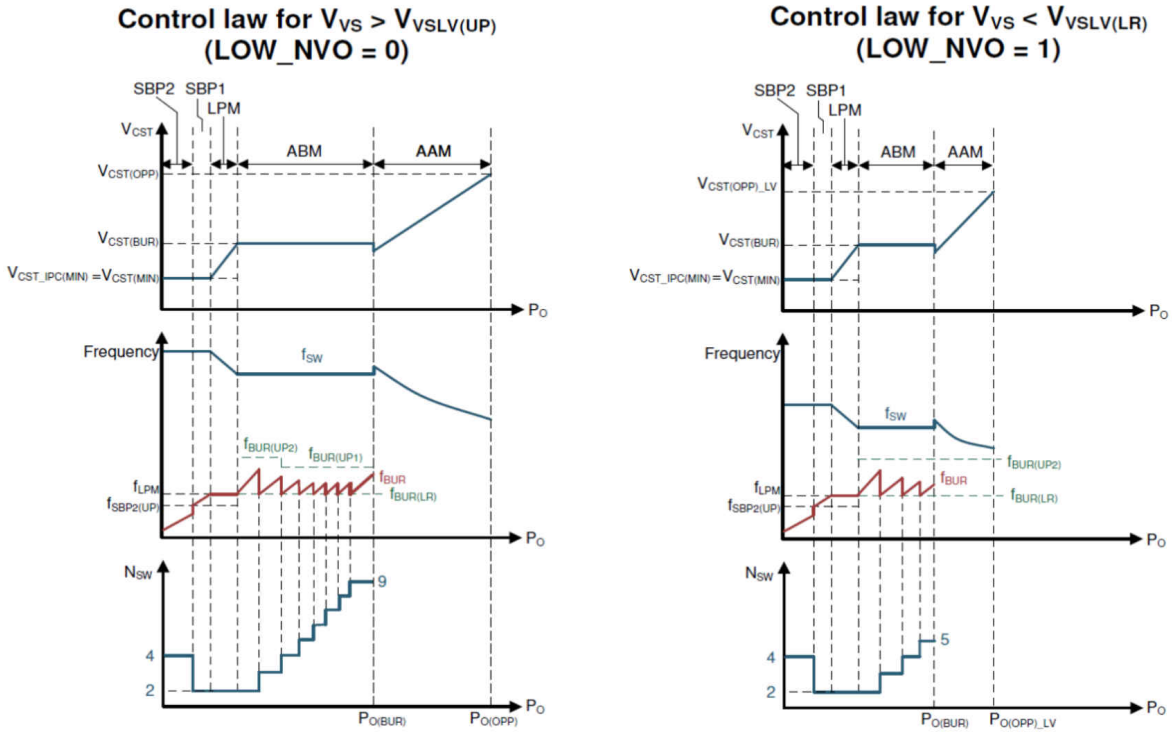

Figure 2-1. Control Law Over Entire Load Range Based on the V_{VS} Condition as $V_{IPC} < 0.9$ V

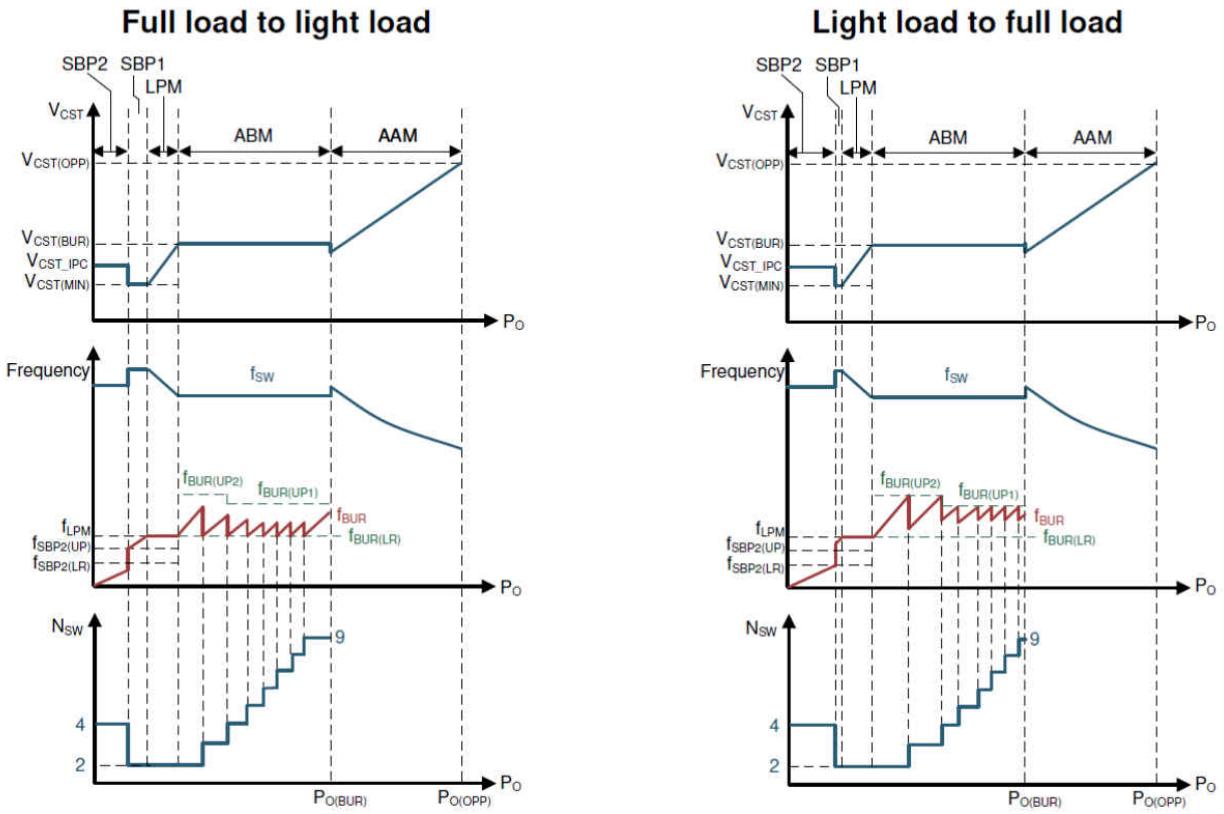

Figure 2-2. Control Law Under Different Load Sweep Direction as V_{IPC} > 0.9 V and V_{VS} > $V_{VSLV(UP)}$

3 Design SOP and Checklist

TI has several publications and reference design to assist customers with designing the UCC28782. The following are some of the publications to assist with customer design.

Selecting the correct reference design as a starting point

- 65W ACF for PD application
- 65W ZVS flyback for PD application
- 100W PFC + ACF with Si-MOS application
- 100W PFC + ACF with GaN application

Using calculator to design parameter

After choosing the correct reference design, the user can customize the parameter with their spec by calculator, UCC28782 calculator includes the IC parameter design and transformer design and secondary side resonance tuning and feedback loop design with TL431, so it is very helpful for customer to design the ACF board.

UCC28782 design calculator tool

Refer the layout guidelines with the data sheet section 11

When the schematic is completed, the layout can be started, the layout guidelines shown at data sheet section 11, and it includes general considerations and detail layout suggestion for each pin and layout example, it covers almost all layout suggestion with UCC28782. It is recommended to review before layout.

UCC28782 data sheet

Review the schematic and layout with checklist

The the schematic and layout design is completed, refer to the checklist shown in Table 3-1 and Table 3-2, so the user can double check that they did not miss any significant item.

UCC28782 system bring up guideline and debug FAQ

After the schematic and layout is finished, the user needs to evaluate the board, and might also face several issue. The user can refer to the application note for these item to speed up the debugging.

UCC28782 system timing up guideline and debug FAQ:

EMI filter design

After the system performance meets the spec without issue, the user needs to fine tune the EMI. TI has several application notes to assist with EMI tuning that include the following:

- Transformer structures that achieve low EMI with low and high side rectifiers
- Flyback Transformer Design for Efficiency and EMI
- Designing Low EMI Power Converters for Industrial and Automotive Systems
- Input EMI Filter Design for Offline Phase-Dimmable LED Power Supplies

Table 3-1. Schematic Checklist

Checklist item	Purpose
The high-side driver with short power-on delay less than 10 µs	Make sure the high side GaN switching can follow PWMH signal immediately
Boostrap diode trr around 35ns	boostrap capacitor voltage charged quickly
Add 24 V or 27 V TVS at BIN pin	BIN and BSW pin voltage rating is 30V, so add TVS to prevent it damaged
Choice the boost inductor with higher than 0.4-A saturation current capability and DCR less than 1 Ω resistance	Prevent it trigger the survival mode easily
RVS1 using 0805 package	The voltage at RVS1 would up to 100V for 20V PD application
Choice the capacitor with low DC bias influenced at BIN, VDD, and Co1	The capacitor may use 35V rating, but its capacitance is derating during 20Vo
Choice the optocoupler with higher CTR and low temperature variation, TLP383 or FODM8801A is suggested	Prevent the lower low frequency gain to suppress the AC ripple.
add the Rdiff and Cdiff at feedback loop	For dynamic load performance tuning
Add the bi-direction TVS diode at depletion FET GS pin	Protect the depletion FET
Reserve the Rrun and Drun	For LPM to ABM transition tuning
Add serial damping inductor with 1206 package	Improve the stability at ABM
SR MOS with 150 V rating for ACF 20V PD application,reserve the TVS at SR DS site	SR spike is observed at output voltage transition and SCP and LPM to ABM
Reserve the RC filter at high side GaN PWM input pin	Prevent the GaN fault turn on by noise

Table 3-2. Layout Checklist

Completed	Layout Checklist
	Minimize the power stage high dv/dt, di/dt, and dB/dt loop to prevent noise coupling to noise sensitive signals, and get better EMI performance
	GaN thermal dissipate by the PCB, make sure add enough via at GaN copper
	Avoid any trace overlap with VS pin trace, and minimize the VS pin trace
	Minimize these high dv/dt trace Vaux, BSW, and SWS to prevent noise coupling to noise sensitive signals
	Make sure these component close to IC to minimize noise coupling: RRDM, RRTZ, RFB, CFB, RVS2, RBUR1, RBUR2, CBUR, Cref, CS pin RC filter, BIN pin TVS, CP13, CBIN2, and CVDD
	Minimize the FB and CS loop to minimize noise coupling
	Csws and Dsws ground connect to Cbulk ground
	For GaN setting, RVS2 ground connect to SET pin and SET pin connect to thermal pad directly, and minimize the ground connection at set pin.
	AGND: the decoupling capacitors for REF, CS, BUR, and P13 connect to AGND, and use kelvin connection to Rsense return path.
	BGND: boost ground, CBIN, CVDD, and Auxwinding ground path connect to BGND, and connect to AGND at thermal pad or CVDD ground.
	PGND : gate driver return for PWML signal, if using the GaN with integrated gate driver, PGND connect to thermal pad directly, if not, connect to source pin of low side FET.
	Provide the shielding with ground planes on these pin : BUR pin and FB loop
	Avoide the shielding with ground planes on these pin : RDM, RTZ, and VS pin
	Make sure the RC filter for high side GaN PWM input pin close to GaN

4 Practical IC Pin Setting

4.1 BUR Pin (Programmable Burst Mode)

The voltage at the BUR pin (V_{BUR}) sets a target peak current threshold ($V_{CST(BUR)}$) which programs the onset of adaptive burst mode (ABM) and determines the clamped peak current level of switching cycles in each burst packet. When VBUR is set higher, ABM will start at heavier output load conditions with higher peak current, so the benefit is higher light-load efficiency but the side effect is a larger burst-mode output voltage ripple. Therefore, 50% to 60% of output load at high line is the recommended highest load condition to enter ABM ($I_{O(BUR)}$) for both Si and GaN-based ACF designs, same as Figure 4-1 showing that IC can program the hysteresis voltage at mode transition.

BUR pin minimum voltage is clamped at 0.7V.

Normally the first high side turn on during the LPM to ABM transition, and it is set by BUR pin, but VDS spike will cause the BIN pin voltage increased during LPM, so deeper burst mode may cause higher voltage then it may damage the BIN and BSW pin, so the BUR pin can set to around 0.7 V as starting point,and then fine tune it during optimizing the average efficiency.

$$R_{BUR2} = \frac{R_{BUR1}K_{BUR-CST}V_{CST(BUR)}}{V_{REF} - K_{BUR-CST}V_{CST(BUR)}} = \frac{4 \times R_{BUR1}V_{CST(BUR)}}{5V - 4 \times V_{CST(BUR)}} \quad (1)$$

$$\Delta V_{BUR(LPM)} = I_{BUR(LPM)} \times \left(\frac{R_{BUR1} \times R_{BUR2}}{R_{BUR1} + R_{BUR2}}\right) \quad (2)$$

$$\Delta V_{BUR(AAM)} = I_{BUR(AAM)} \times \left(\frac{R_{BUR1} \times R_{BUR2}}{R_{BUR1} + R_{BUR2}}\right) \quad (3)$$

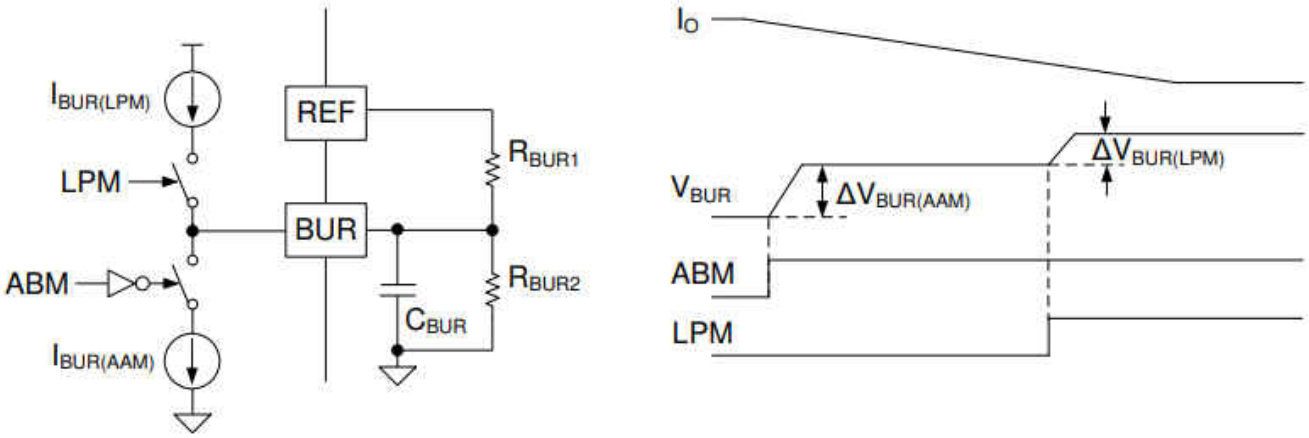

Figure 4-1. Hysteresis Voltage Generation on BUR Pin

4.2 RDM Pin (Sets Synthesized Demagnetization Time for ZVS Tuning)

The R_{RDM} resistor provides the power stage information to the t_{DM} optimizer for auto-tuning the on-time of PWMH to achieve ZVS within a given tz discharge time. The following equation calculates the resistance, based on the knowledge of the primary magnetizing inductance (LM), auxiliary-to-primary turns ratio (NA/NP), the values of the resistor divider (R_{VS1} and R_{VS2}) from the auxiliary winding to VS pin, and the current sense resistor (R_{CS}). Among those parameters, LM contributes the most variation due to its typically wider tolerance. The optimizer is equipped with wide enough on-time tuning range of PWMH to cover tolerance errors. Therefore, just typical values are enough for the calculation.

The RDM resistance is designed by calculator, and the RDM resistance tuning range is around 30% of calculated result to make sure the internal tuner would not saturate.

Normally the RDM needs to fine tune for SR voltage stress issue.

UCC28782 automatically extends the first PWMH pulse width around 140% longer than the following PWMH pulse to prevent it non ZCS turn off. When the high side switch turns off at lower di/dt current instance, the voltage stress can be reduced, but it created more negative magnetizing current, so it would cause SR VDS spike higher as Figure 4-2, so RDM resistance needs to be reduced at this case.

$$R_{RDM} = \frac{N_A R_{VS2}}{N_P (R_{VS1} + R_{VS2})} \frac{K_{DM} L_M}{R_{CS}} \tag{4}$$

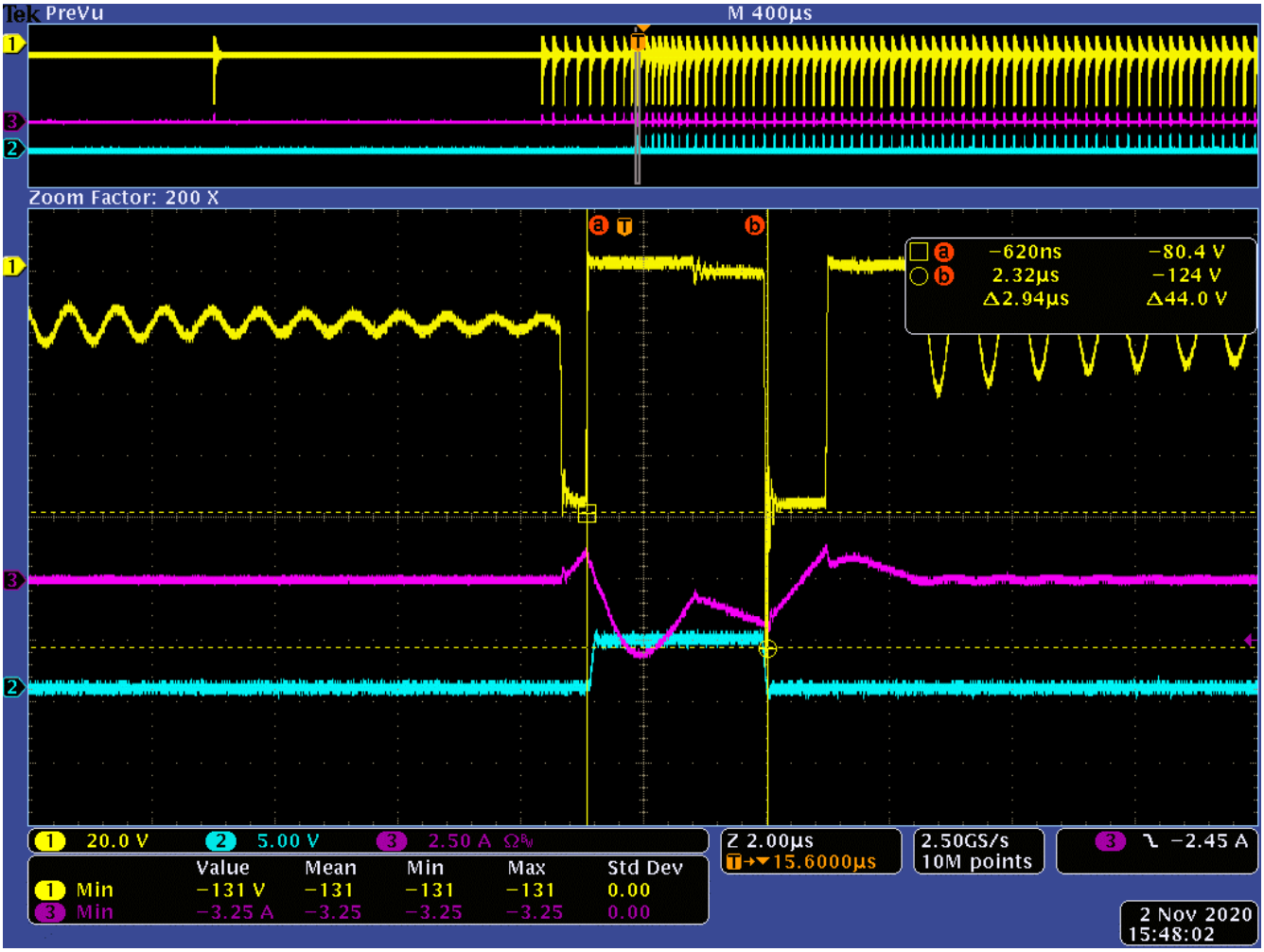

Figure 4-2. SR VDS spike during first high side turn on

4.3 RTZ Pin (Sets Delay for Transition Time to Zero)

The dead-time between PWMH falling edge and PWML rising edge (tz) serves as the wait time for V_{SW} transition from its high level down to the target ZVS point. Since the optimal tZ varies with V_{BULK}, the internal dead-time optimizer automatically extends tz as V_{BULK} is less than the highest voltage of the input bulk capacitor ($V_{BULK(MAX)}$). The circulating energy for ZVS can be further reduced, obtaining higher efficiency at low line versus a fixed dead-time over a wide line voltage range. A resistor on the RTZ pin (R_{RTZ}) programs the minimum tZ ($t_{Z(MIN)}$) at $V_{BULK(MAX)}$, which is the sum of the propagation delay of the high-side driver ($t_{D(DR)}$) and the minimum resonant transition time of V_{SW} falling edge ($t_{LC(MIN)}$).

Normally the RTZ is designed as calculator result. If the VDS voltage has ring back voltage as Figure 4-3 showing, you need to reduce the RTZ resistance.

$$R_{RTZ} = K_{TZ} \times t_{Z(MIN)} = K_{TZ} \times \left(t_{D(DR)} + t_{LC(MIN)}\right) \tag{5}$$

$$t_{LC(MIN)} = \left[\pi - COS^{-1}\left(\frac{N_{PS}(V_O + V_F)}{V_{BULK(MAX)}}\right)\right] \times \sqrt{L_M C_{SW}} \tag{6}$$

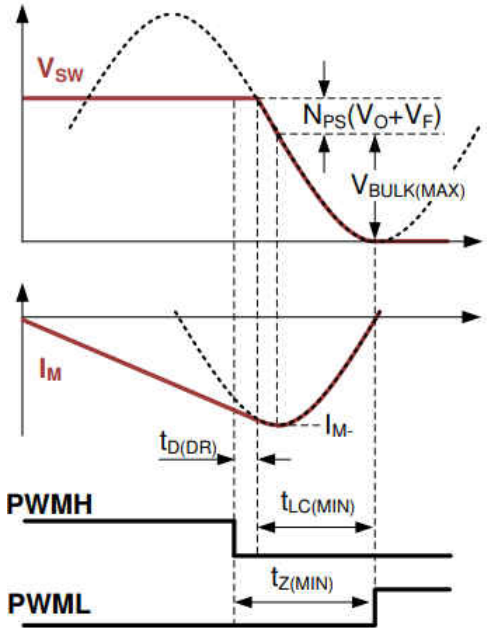

Figure 4-3. RTZ Setting for the Falling-edge Transition of VSW

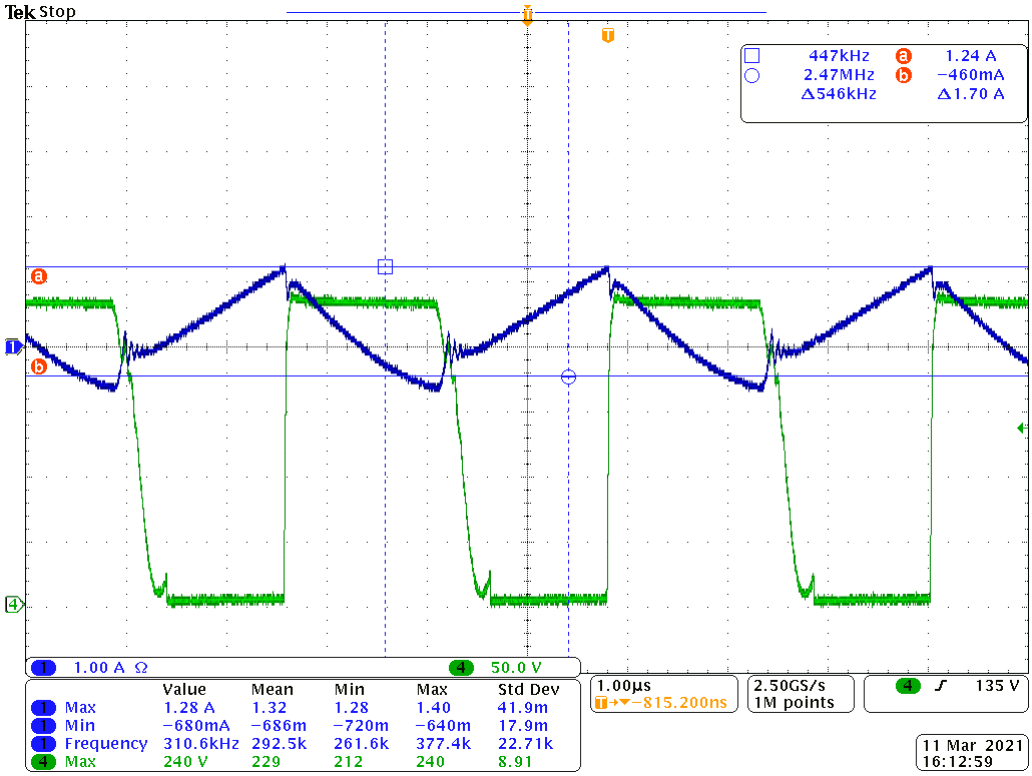

Figure 4-4. RTZ Setting too large cause VDS ring back

4.4 Boost Pin

The controller bias power for a wide output voltage range can be simplified with the integrated switching regulator of the UCC28782 and a single auxiliary winding on primary side. The boost conversion mode provides an 18.5-V regulation level for the V_{DD} pin from the rectified auxiliary-winding voltage at the BIN pin.

The boost circuit shown as Figure 4-5, and each component suggestion as below list.

- D_{AUX}: using Schottky diode with 150 V rating for PD application, low Vf is better for low Vo.
- C_{BIN}: if customer does not want to trigger the survival mode, the E-capacitor with larger capacitance is suggested, and it has lower influence with DC bias, and ceramic capacitor still needs to close IC BIN pin.
- D_{BIN}: the BIN pin and BSW pin voltage rating is 30 V, so clamping voltage is suggested 24 V, but it must be higher OVP threshold.
- L_B: the 22-µH inductor with higher than 0.4-A saturation current capability and DCR less than 1 Ω resistance is recommended for boost inductor selection.
- D_B: the Boost diode is suggested with Schottky diode with 30V rating

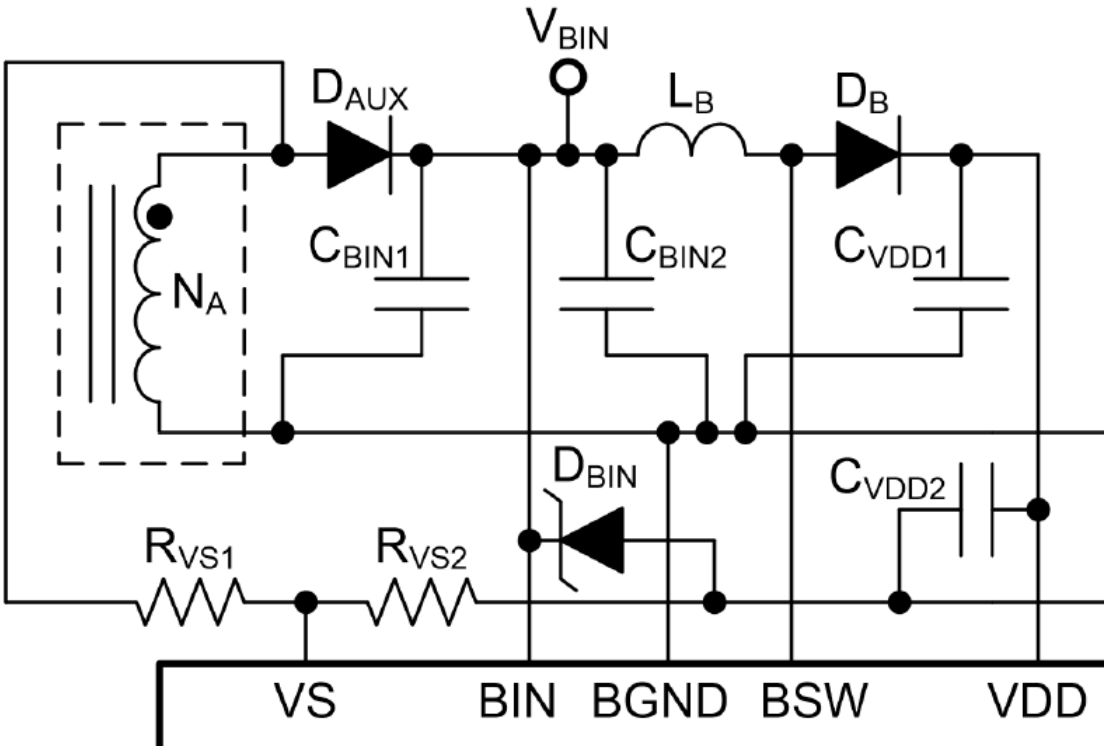

Figure 4-5. Boost Circuit

5 Transformer design

ACF is designed for high switching frequency application, so there are several item also need to be careful during the transformer design, and these suggestion is based on 60W PD design.

Using Litz wire for bobbin design

The ACF is designed for high switching frequency application, and its switching frequency may up to 500KHz during the ABM, so the skin effect will cause lots of ACR loss, the suggested primary side winding is 20*0.05mm, and secondary side winding is 150*0.05mm. Aux-winding DCR need to less than 0.1Ω.

Core material

Same as previous mention that switching may up to 500KHz, so Core material suggest optimized with 300KHz~500KHz range to reduce the core loss, and there are some suggested core material as below list. The Bmax also suggest to within 0.2T to reduce the core loss.

TDK-N49; Ferroxcube-3F36; Hitachi-ML90S

Turn ratio

The turn ratio is limited by primary side MOS and SR MOS voltage rating, turn ratio within 5~6 is suggested for 20V PD application.

Maximum turn ratio ($N_{PS(MAX)}$) is limited by the maximum derated drain-to-source voltage of low side MOS ($V_{DS\_QL(MAX)}$). In the expression below, ΔV_{CLAMP} is a voltage deviation above the reflected output voltage. It can be either the ripple voltage of C_{CLAMP} in AAM mode, or the voltage over-charge of C_{CLAMP} by the leakage inductance energy when high side MOS is disabled in LPM. V_O is the output voltage, and VF is the forward voltage drop of the secondary rectifier.

$$N_{PS(MAX)} = \frac{V_{DS\_QL(MAX)} - V_{BULK(MAX)} - \Delta V_{CLAMP}}{V_O + V_F} \tag{7}$$

Minimum turn ratio ($N_{PS(MIN)}$) is limited by the maximum derated drain-to-source voltage of the secondary rectifier ($V_{DS\_SR(MAX)}$). In the expression for $N_{PS(MIN)}$, ΔVSPIKE should account for any additional voltage spike higher than $V_{BULK(MAX)}$/NPS that occurs when high side MOS is active and turns-off at non-zero current in AAM mode.

$$N_{PS(MIN)} = \frac{V_{BULK(MAX)}}{V_{DS\_SR(MAX)} - V_O - \Delta V_{SPIKE}} \tag{8}$$

Inductance

Lm can be estimated based on minimum switching frequency ($F_{SW(MIN)}$) at $V_{BULK(MIN)}$, maximum duty cycle (D_{MAX}), and output power at highest nominal output voltage, nominal full-load current ($P_{O(FL)}$).

Lr is suggested within 3uH to reduce the VDS spike during LPM.

$$D_{MAX} = \frac{N_{PS}(V_O + V_F)}{V_{BULK(MIN)} + N_{PS}(V_O + V_F)} \tag{9}$$

$$L_M = \frac{D_{MAX}^2 V_{BULK(MIN)}^2 \eta}{2P_{O(FL)}} \times \frac{(1 - K_{RES})}{F_{SW(MIN)}} \tag{10}$$

6 References

1. Texas Instruments, UCC28782 High-Density Active-Clamp Flyback Controller with EMI Dithering, X-CapDischarge, and Bias Power Management data sheet.
2. Texas Instruments, UCC28782 design calculator tool.
3. Texas Instruments, 65W ACF for PD application user guide.
4. Texas Instruments, 65W ZVS flyback for PD application reference guide.
5. Texas Instruments, 100W PFC + ACF with Si-MOS application reference guide.
6. Texas Instruments, 100W PFC + ACF with GaN application reference guide.
7. Texas Instruments, Transformer structures that achieve low EMI with low and high side rectifiers publication.
8. Texas Instruments, Flyback Transformer Design for Efficiency and EMI
9. Texas Instruments, Designing Low EMI Power Converters for Industrial and Automotive Systems presentation.
10. Texas Instruments, Input EMI Filter Design for Offline Phase-Dimmable LED Power Supplies presentation.

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