User's Guide

TPS92682-Q1 Frame Definitions and Examples

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ABSTRACT

This document serves as a quick reference for Software or Firmware Engineers tasked with establishing and maintaining communications with the TPS92682 device. There are real code examples written in the C programming language designed to accelerate the learning curve required to effectively manipulate the various registers found in TPS92682 devices. All data sheet references are from the *TPS92682-Q1 Dual-Channel Constant-Voltage and Constant-Current Controller with SPI Data Sheet*.

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Trademarks

1 Build a Frame

Create a valid frame based on address and data with parity.

```
Uint16 assembleSPICmd_682(Uint16 write, Uint16 address, Uint8 data)
{
    Uint16 assembledCmd = 0; // Build this to shift through parity calculation
    Uint16 parity = 0;       // Parity bit calculated here
    Uint16 packet = 0;       // This will be what we send

    if(write)
    {
        assembledCmd |= 0x8000;  // Set CMD = 1
    }

    assembledCmd |= (((address << 9) & 0x7E00) | (Uint16)(data & 0x00FF));
    packet = assembledCmd;

    // Calculate parity
    while(assembledCmd > 0)
    {
        // Count the number of 1s in the LSb
        if(assembledCmd & 0x0001)
        {
            parity++;
        }
        // Shift right
        assembledCmd >>= 1;
    }

    // If the LSb is a 0 (even # of 1s), we need to add the odd parity bit
    if(!(parity & 0x0001))
    {
        packet |= (1 << 8);
    }

    return(packet);
}
```

7.5.2 Command Frame

The command frames are the only defined frame-format that are sent from master to slave on MOSI. A command frame can be either a read command or a write command. A Command frame consists of a CMD bit, six bits of ADDRESS, a PARITY bit (odd parity), and eight bits of DATA. The format of the Command frame is shown in Figure 7-23. The bit sequence is as follows:

1. The COMMAND bit (CMD). CMD = 1 means the transfer is a write command; CMD = 0 means it is a read command.
2. Six bits of ADDRESS (A5..A0)
3. The PARITY bit (PAR). This bit is set by the following equation: PARITY = XNOR(CMD, A5..A0, D7..D0).
4. Eight bits of DATA (D7..D0). For read commands, the DATA bits must be set to zero.

Both the Read and the Write Command follow the Command frame format.

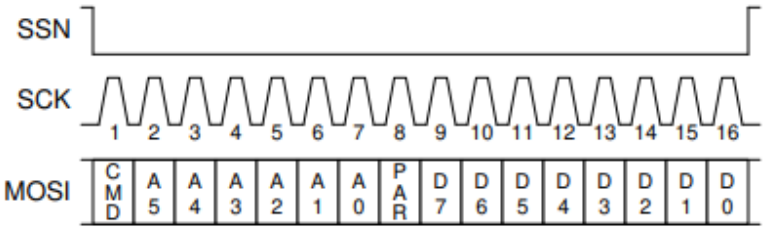


Figure 7-23. Command Frame Format

2 Response Frame

The command response frames are defined in the following portions of the *TPS92682-Q1 Dual-Channel Constant-Voltage and Constant-Current Controller with SPI Data Sheet*.

The following image illustrates the read response frame section of the data sheet.

7.5.3 Response Frame

There are three possible response frame formats: Read Response, Write Response, and Write Error/POR. These formats are further described below.

7.5.3.1 Read Response Frame Format

The Read Response has the following format:

1. The SPI Error bit (SPE)
2. Four reserved bits (always '1100')
3. The RT Open Fault bit (RTO)
4. The Power-Cycled bit (PC)
5. The Thermal Warning bit (TW)
6. Eight bits of DATA (D7..D0)

This is shown in Figure 7-24. This frame is sent out by the TPS92682-Q1 following a read command.

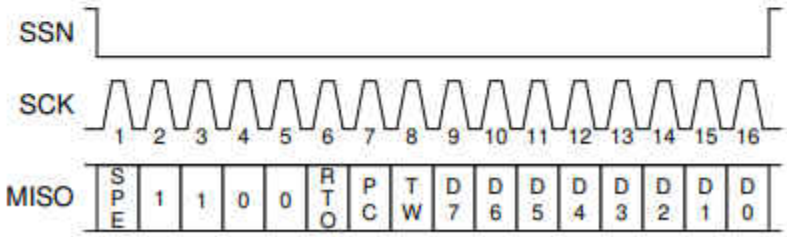
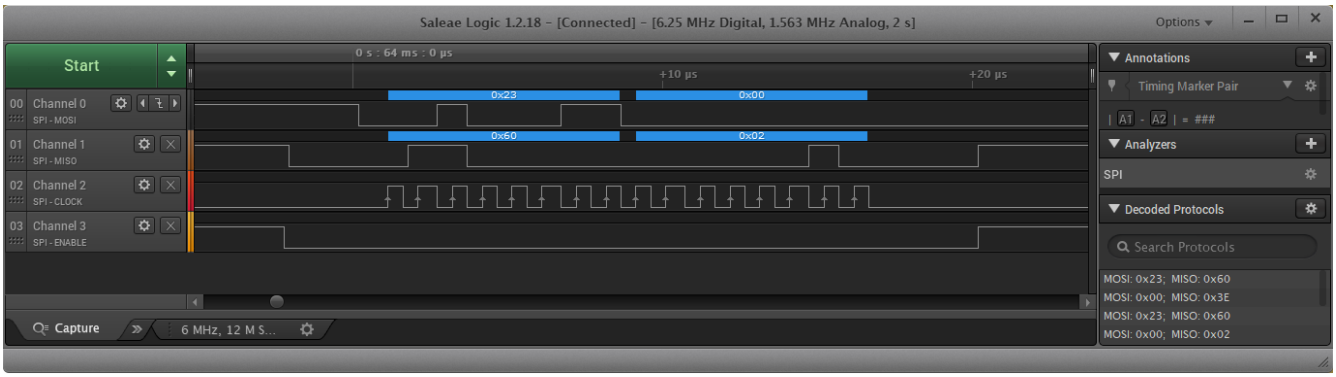


Figure 7-24. Read Response Frame Format

The command frame (Build a Frame) is SPI MOSI and the response is found in SPI MISO following it. The SPI MOSI command issued = 0x23 0x00. In this example the return (MISO result of 2 reads per SPI) has a status byte of 0x60 with a data byte of 0x02 indicating: CH2UV: Output undervoltage fault (CH2UV is disabled if 2PH is set to '1'). For a detailed explanation of the expected SPI bus return value with the TPS92682-Q1, visit the *TI E2E™ support forum*.

The following image shows the *Read Fault Register 0x11 (FLT1)*.



The following image shows the write response frame format, write error/POR frame format SPI error sections from the data sheet:

7.5.3.2 Write Response Frame Format

The Write Response frame has the following format:

1. The SPI Error bit (SPE)
2. The COMMAND bit (CMD)
3. Six bits of ADDRESS (A5..A0)
4. Eight bits of DATA (D7..D0)

This is shown in Figure 7-25. This frame is sent out following a write command if the previously received frame was a write command and no SPI Error occurred during that frame.
The data and address bits in the write response are the data and address that were sent in the previous write command.

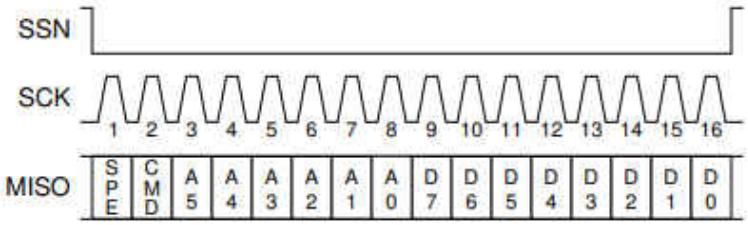


Figure 7-25. Write Response Frame Format

7.5.3.3 Write Error/POR Frame Format

The Write Error/POR frame is simply a '1' in the MSB, followed by all zeroes (see Figure 7-26). This frame is sent out by the TPS92682-Q1 internal digital block during the first SPI transfer following power-on reset, or following a write command with a SPI Error.

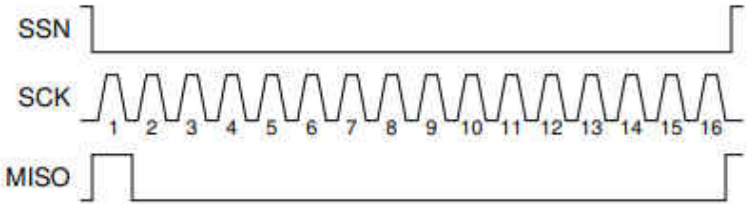
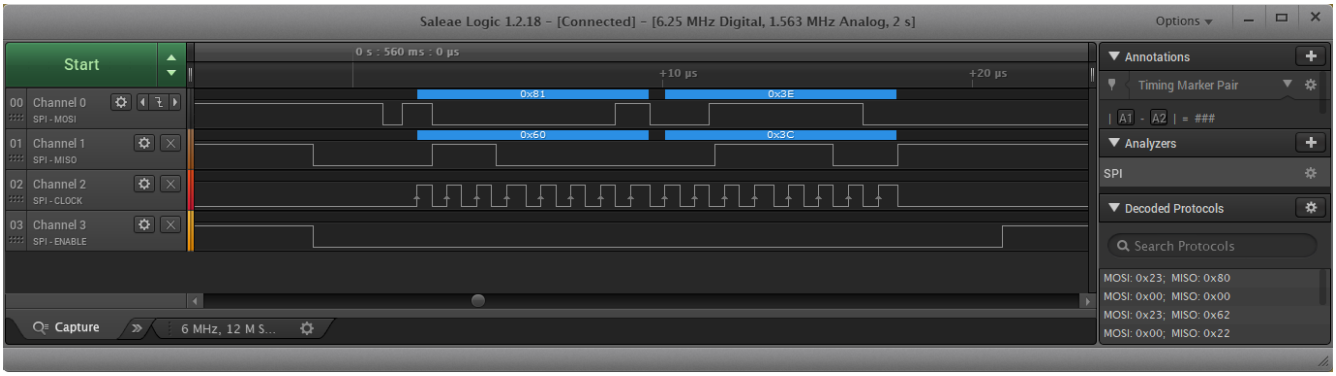


Figure 7-26. Write Error/POR

The following command frame is SPI MOSI and the response is found in SPI MISO after it. The SPI MOSI command issued = 0x81 0x3E. In this example, the return (MISO result of previous read of register 0x00) has a status byte of 0x60 with a data byte of 0x3c indicating: default power up value for register 0x00. For a detailed explanation of the expected SPI bus return value with the TPS92682-Q1, visit the *TI E2E™ support forum*.

The following image shows the Write Enable Register 0x00 (EN).



7.5.4 SPI Error

The TPS92682-Q1 device records a SPI Error if any of the following conditions occur:

- The SPI command has a non-integer multiple of 16 SCK pulses.
- Any of the DATA bits during a read command are non-zero.
- There is a parity error in the previously received command.

If any of these conditions are true, the TPS92682 sets the SPE bit high in the next response frame. A write command with a SPI Error (not 16-bit aligned or bad parity) does NOT write to the register being addressed. Similarly, a read command to FLT1 or FLT2 does not clear any active fault bits in those registers if the command has a SPI Error.

3 Initialization

Note

Initialize the 682 device at power up.

1. Read fault register 0x11 to clear the PC (Power Cycle) bit (D5). SPI Command = 0x23 0x00
2. Read fault register 0x12 to clear any remaining faults. SPI Command = 0x25 0x00

4 Registers

The following image from the data sheet shows the available TPS92682 registers:

7.6 TPS92682 Registers

The SPI-accessible registers are 8-bits wide and exist in a 6-bit-addressable register array (0x00 through 0x3F). The registers in the TPS92682 device contain programmed information and operating status. Upon power-up the registers are reset to their default values. Writes to unlisted addresses are not permitted and may result in undesired operation. Reads of unlisted addresses return the zero value.

Reserved bits ("RSVD") must be written with '0' values when writing. Registers are read/write unless indicated in the description of the register. Table 7-2 lists the TPS92682 register map.

Table 7-2. TPS92682 Register Map

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
00h	EN	FPINRST	SYNCEN	CH2MAXDEN	CH1MAXDEN	CH2PDRVEN	CH1PDRVEN	CH2EN	CH1EN	00111100
01h	CFG1	PWMPH	INTPWM	2PH	LH	CH2HG	CH1HG	CH2CV	CH1CV	00000000
02h	CFG2	CH2LEB	CH1LEB	RSVD	RSVD	CH2FILT1	RSVD	RSVD	CH1FILT1	00000000
03h	SWDIV	RSVD	RSVD	RSVD	RSVD	CH2DIV1:0		CH1DIV1:0		00000000
04h	ISLOPE	RSVD	CH2ISLP2:0			RSVD	CH1ISLP2:0			01010101
05h	FM	RSVD	RSVD	FMMAG1:0		FMFREQ3:0				00000101
06h	SOFTSTART	CH2SS3:0				CH1SS3:0				01110111
07h	CH1IADJ	CH1IADJ7:0								00000000
08h	CH2IADJ	CH2IADJ7:0								00000000
09h	PWMDIV	RSVD	RSVD	RSVD	RSVD	RSVD	PWMDIV2:0			00000001
0Ah	CH1PWML	CH1PWM7:0								00000000
0Bh	CH1PWMH	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	CH1PWM9:8		00000000
0Ch	CH2PWML	CH2PWM7:0								00000000
0Dh	CH2PWMH	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	CH2PWM9:8		00000000
0Eh	ILIM	CH2ILIMCNT1:0		CH1ILIMCNT1:0		CH2ILIM1:0		CH1ILIM1:0		00001111
0Fh	IFT	RSVD	RSVD	RSVD	RSVD	CH2IFT1:0		CH1IFT1:0		00001010
10h	MFT	CH2MFT3:0				CH1MFT3:0				10011001
11h	FLT1	RTO	RSVD	PC	TW	CH2OV	CH1OV	CH2UV	CH1UV	read
12h	FLT2	CH2UC	CH1UC	CH2OC	CH1OC	CH2ILIM	CH1ILIM	CH2ISO	CH1ISO	read
13h	FEN1	CH2RFEN	CH1RFEN	CH2FBOEN	CH1FBOEN	CH2OVEN	CH1OVEN	CH2UVEN	CH1UVEN	00111100
14h	FEN2	OVOPT	RSVD	CH2OCEN	CH1OCEN	CH2ILIMEN	CH1ILIMEN	CH2ISOEN	CH1ISOEN	00001111
15h	FLATEN	CH2ILIMFL	CH1ILIMFL	CH2OCFL	CH1OCFL	CH2OVFL	CH1OVFL	CH2UVFL	CH1UVFL	00000000
16h	OV	RSVD	CH2OV2:0			RSVD	CH1OV2:0			00100010
17h	LHCFG	LHPWMPH	LHINTPWM	LHCH2MAXDEN	LHCH1MAXDEN	LHCH2PDRVEN	LHCH1PDRVEN	LHCH2EN	LHCH1EN	00111100
18h	LHCH1IADJ	LHCH1IADJ7:0								00000000
19h	LHCH2IADJ	LHCH2IADJ7:0								00000000
1Ah	LHCH1PWML	LHCH1PWM7:0								00000000
1Bh	LHCH1PWMH	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	LHCH1PWM9:8		00000000
1Ch	LHCH2PWML	LHCH2PWM7:0								00000000
1Dh	LHCH2PWMH	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	LHCH2PWM9:8		00000000
1Eh	LHILIM	LHCH2ILIMCNT1:0		LHCH1ILIMCNT1:0		LHCH2ILIM1:0		LHCH1ILIM1:0		00001111
1Fh	LHIFT	RSVD	RSVD	RSVD	RSVD	LHCH2IFT1:0		LHCH1IFT1:0		00001010
20h	LHMFT	LHCH2MFT3:0				LHCH1MFT3:0				10011001
21h	LHFEN1	LHCH2RFEN	LHCH1RFEN	LHCH2FBOEN	LHCH1FBOEN	LHCH2OVEN	LHCH1OVEN	LHCH2UVEN	LHCH1UVEN	00111100
22h	LHFEN2	RSVD	RSVD	LHCH2OCEN	LHCH1OCEN	LHCH2ILIMEN	LHCH1ILIMEN	LHCH2ISOEN	LHCH1ISOEN	00001111
23h	LHFLATEN	LHCH2ILIMFL	LHCH1ILIMFL	LHCH2OCFL	LHCH1OCFL	LHCH2OVFL	LHCH1OVFL	LHCH2UVFL	LHCH1UVFL	00000000
24h	LHOV	RSVD	LHCH2OV2:0			RSVD	LHCH1OV2:0			00100010
25h	CAL	CH2CAL2:0			CH2GOFF	CH1CAL2:0			CH1GOFF	00000000
26h	RESET	RESET7:0								00000000

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