Application Note

Using Low-Side FETs with the BQ769x2 Battery Monitor Family

ABSTRACT

The BQ76952, BQ76942, and BQ769142 battery monitors support high-side N-channel FETs switching PACK+. In some designs the battery electronics designer will need or want to control FETs on the low side of the battery switching PACK-. This document discusses and shows results of switching low-side FETs using BQ769x2 devices and provides an example for designers implementing low-side FETs with devices in the BQ769x2 family.

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1 Introduction

The BQ769x2 family of battery monitor devices is designed with integrated high-side N-channel MOSFET drivers CHG and DSG. High-side switching allows easy interface to the battery with simple communication interfaces referenced to PACK- which can still operate when the battery is protected. The data sheet and evaluation module schematics and Figure 1-1 show FETs on the high-side current path. The BQ769x2 uses series FETs connected in a common drain configuration. The charge FET pulls the charger down to the battery voltage when on and the discharge FET pulls the load up to PACK+ when on. Low-side switching may be desired when the system specifications include an isolated interface, or require low side switching, or the design implements FETs not easily driven on the high side. Figure 1-2 shows FETs on the low side, again with a common drain configuration. The discharge FET pulls PACK- down to battery negative when on and the charge FET pulls the charger negative up to the battery negative voltage when on.

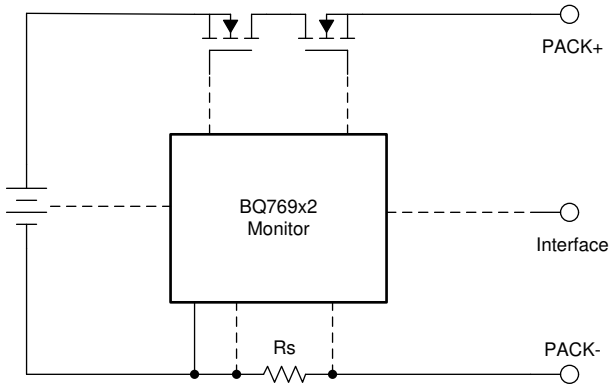

Figure 1-1. High-Side FETs

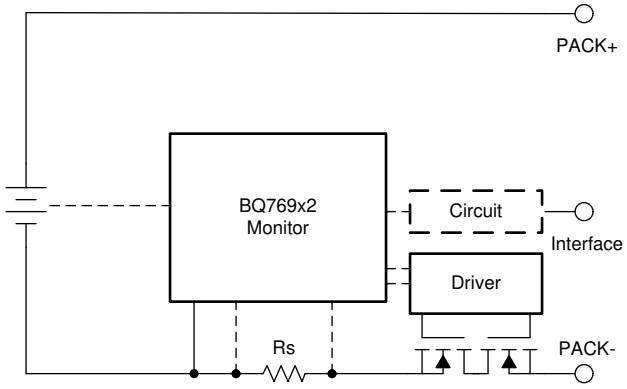

Figure 1-2. Low-Side FETs

The BQ769x2 does not include integrated low-side drivers, but has digital outputs DDSG and DCHG which combine the FET output states with the precharge and predischarge states and can signal the desired state of the FETs. To implement a driver it is good to look at the voltage range needed for the FET gates. With the circuit "GND" reference at the battery negative, when the discharge FET is off the discharge FET gate is at GND and PACK- can be pulled to the PACK+ by a load resistance as shown in Figure 1-3. The system cannot charge in this state and the charge FET can be off with the gate voltage at VBAT also. When the discharge FET is turned on its gate voltage is raised to a voltage V_{FETON} which will turn on the discharge FET. PACK- is pulled down toward the GND voltage as shown in Figure 1-4. The charge FET gate can also be turned on by the V_{FETON} voltage to eliminate the voltage drop across the body diode and avoid heating the FET. Neglecting the voltage drop of the sense resistor and FET resistances PACK- voltage is at GND.

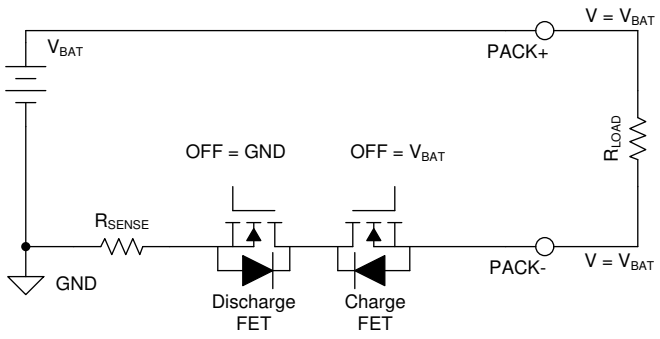

Figure 1-3. Discharge FET Off, Load Attached

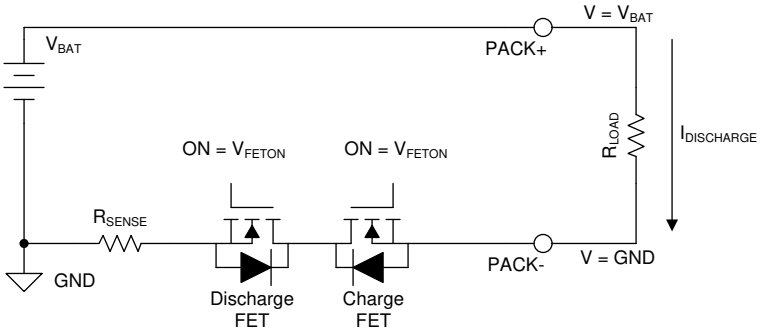

Figure 1-4. Discharge FET On, Load Attached

When the charge FET is off with a charger attached, the PACK- voltage is pushed below the GND level. For the charge FET to stay off the gate voltage must be near the PACK- voltage as shown in Figure 1-5. When the charge FET is on with the charger attached, the gate is raised to the V_{FETON} voltage and PACK- is pulled up toward GND, see Figure 1-6.

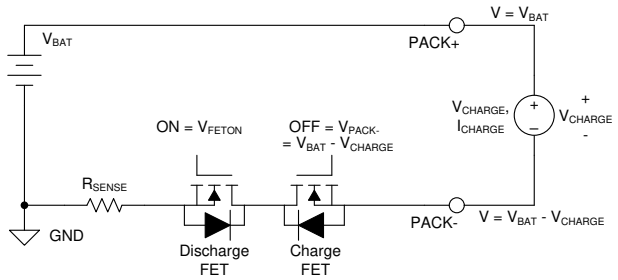

Figure 1-5. Charge FET Off, Charger Attached

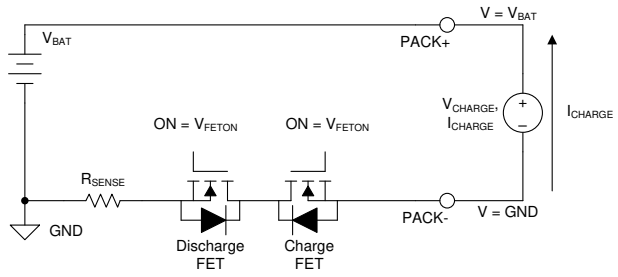

Figure 1-6. Charge FET On, Charger Attached

If a reversed charger can be connected to the battery both the battery and charger want to push current in the same direction. Once the fault is detected and the FETs open, the reversed charger pushes the PACK- voltage above the PACK+ voltage. The discharge FET must withstand the high voltage, and the charge FET gate voltage must rise to prevent damage to the FET. This condition is shown in Figure 1-7.

Figure 1-8 summarizes the voltage range of the FET gates. The discharge gate must move from V_{FETON} when on to GND when off. The charge FET gate voltage must move from V_{FETON} to the PACK- voltage to turn the FET off, but depending on the FET and system conditions that voltage may have a large range above or below the battery voltage. A driver circuit design will need to provide and accommodate these voltage ranges.

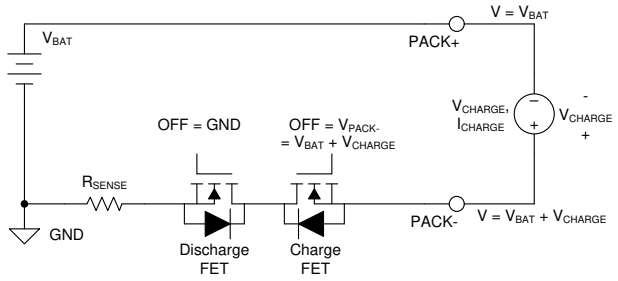

Figure 1-7. Reversed Charger, FETs Off

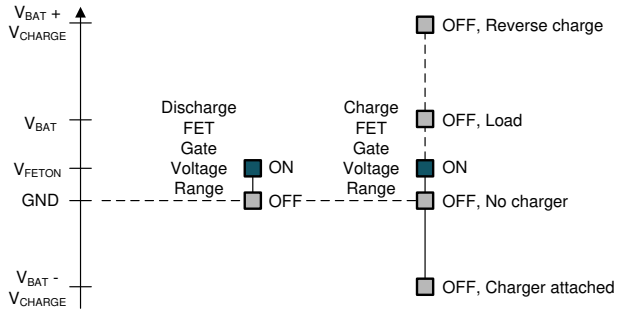

Figure 1-8. Voltage Range for Low Side FET Gates

2 Circuit Concepts

A FET driver circuit then will need to take the digital control signal from the BQ769x2, provide a supply voltage for the V_{FETON} high level, and provide for switching the gates accommodating the voltage range in Figure 1-8 with a speed suitable for the system design.

Figure 2-1 shows a basic circuit approach where a regulator provides a V_{FETON} voltage for a driver which provides level shifting of the digital signal from the BQ76952 to the V_{FETON} voltage. The resistor R4 brings the drive voltage to the discharge FET gate. With the extra range of the charge FET gate, Q3 allows the gate voltage to go negative when the Cdrive is off. D1 blocks current into the driver when PACK- is high. D2 limits the gate -source voltage of the Q1 charge FET. R1 provides a current limit from the driver as Cdrive turns on if Q1 is slow to turn on. R2 turns off the FET when Cdrive goes low since D1 prevents the driver from pulling current from the gate.

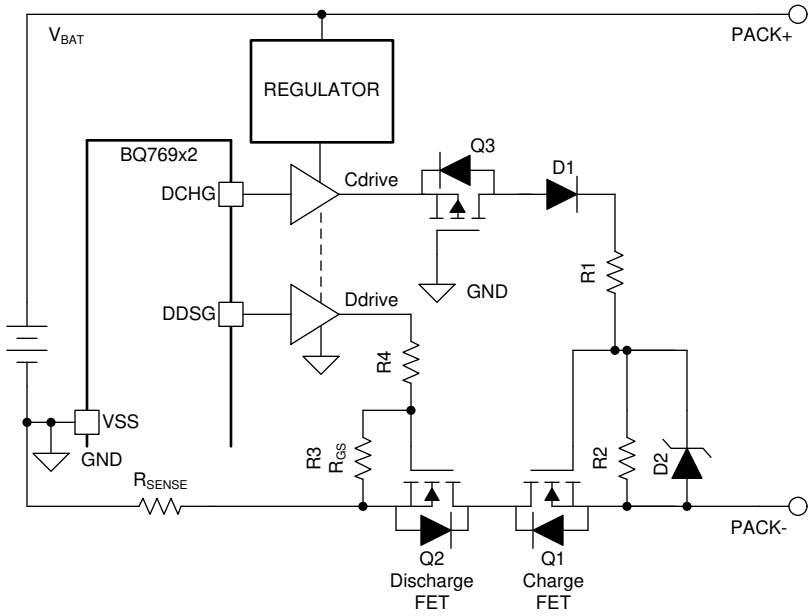

Figure 2-1. Simple Driver Circuit, Resistive Charge Turn Off

When the driver can accept its output being pulled above the supply, a circuit such as Figure 2-2 might be used. D3 limits the voltage to the driver to its safe level and the gate-source voltage of Q3. R1 provides a limited current bypass past D1 so that the driver can help pull down the gate; it must limit the current back into D3 when PACK- is at its maximum voltage. So turn off will still be slow, and once Q1 begins to turn off and PACK- falls, it is R2 which completes turn off of the charge FET Q1. Since most IC drivers have an ABS MAX output of the driver voltage, a special driver is required for this type implementation.

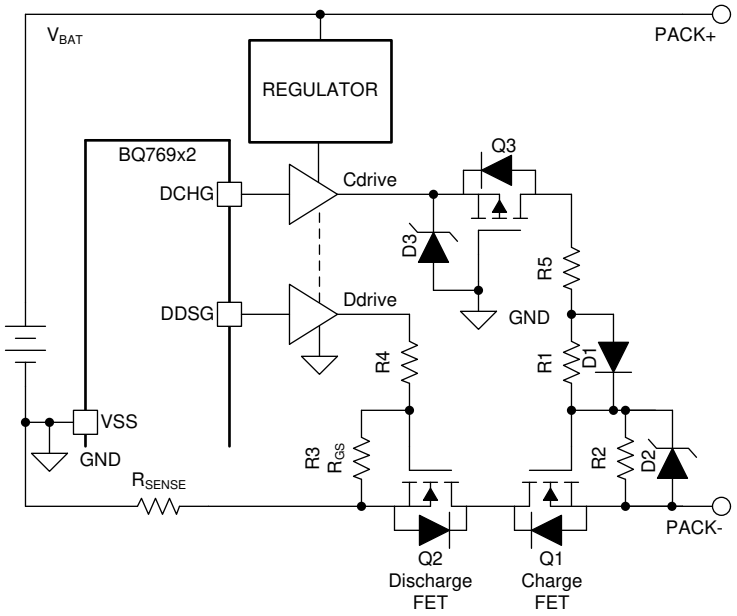

Figure 2-2. Driver with Limited Turn Off Current

Figure 2-3 shows a concept where the charge FET Q1 is driven on by the driver or is clamped off by Q4. This technique could be very effective at turning off Q1, but would require continuous current whether the charge FET was on or off.

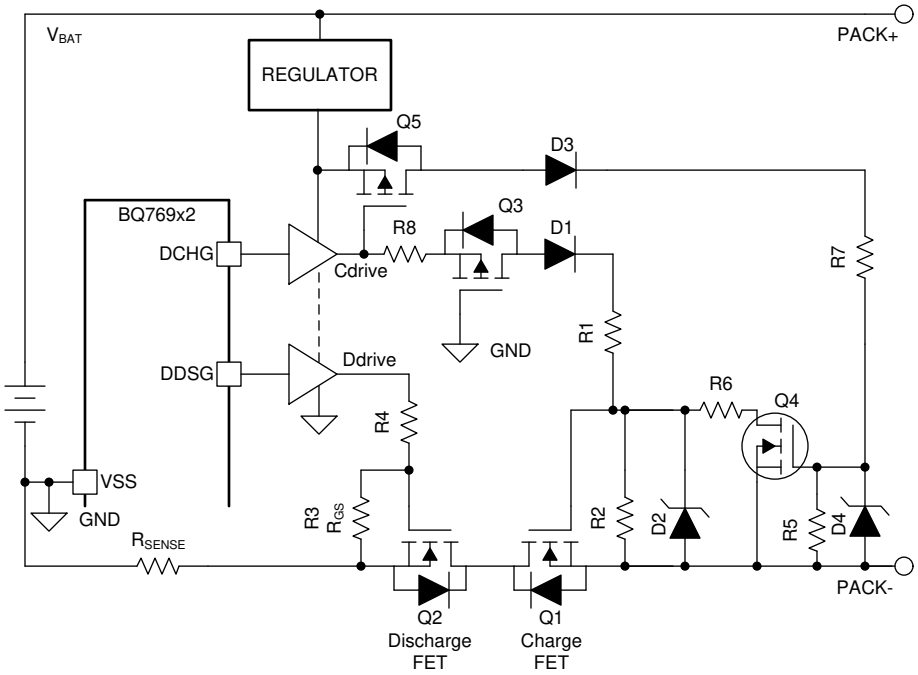

Figure 2-3. Driver with Charge FET Driven Clamp

Figure 2-4 is much like the simple driver circuit but with a gain circuit to help turn off the charge FET more quickly than with R2 alone. This circuit is powered by the Q1 gate voltage and Q4 will be on while voltage is present even as PACK- drops below GND. Either a PNP or P-channel FET could be used for Q4, the FET would be voltage controlled requiring less current, but V_{GSth} may be larger than the V_{BE} of the PNP transistor. The additional diode D3 keeps the base of Q4 above the emitter when the driver is on. The driver must provide current for both the R_{GS} resistor R2 and the base resistor R5, so more current is required than the simple driver circuit while the FET is on.

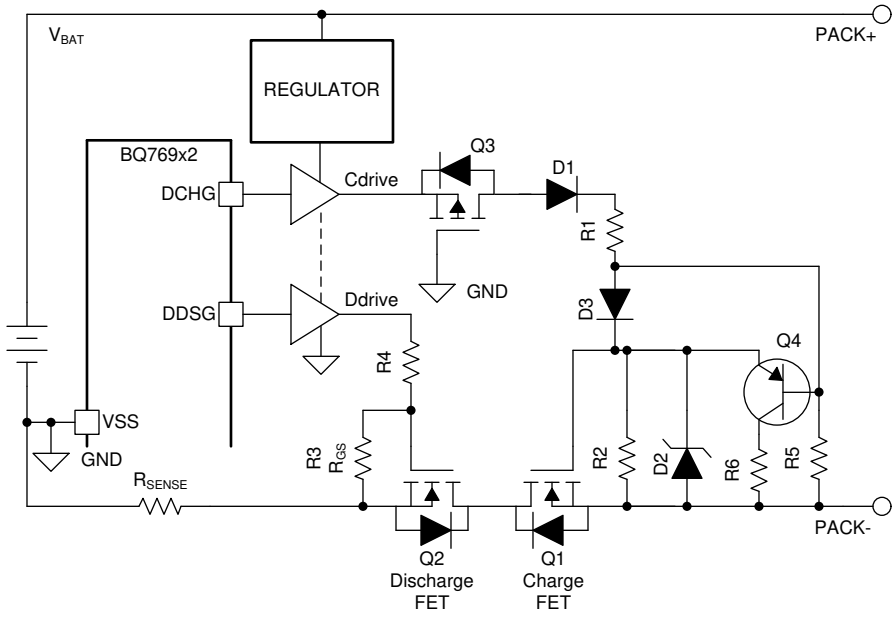

Figure 2-4. Charge FET Driver with PNP Turn Off

A high performance option would be to use an isolated gate driver for the charge path as represented in Figure 2-5. The isolated driver would be very effective at driving the charge FET gate high or low as needed regardless of the PACK- voltage, but would require an isolated power supply.

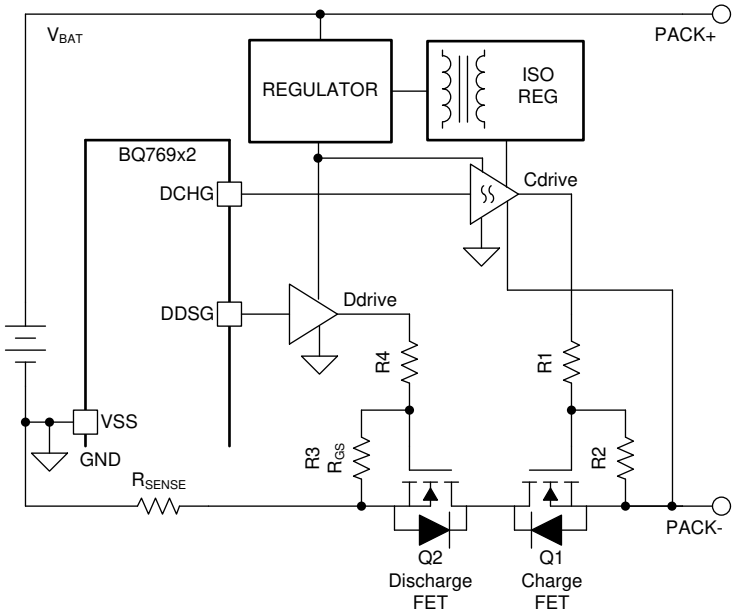

Figure 2-5. Isolated Driver

Test circuits in this application report use the simple driver concept of Figure 2-1 and the PNP circuit of Figure 2-4.

3 Configuration

Data memory configuration must be set to use low-side FETs with the BQ769x2 devices. By default the FET drivers are off in the data memory, but the charge pump is enabled. DDSG and DCHG are also disabled. The Settings:FET:FET Options[FET_CTRL_EN] bit is set by default and must remain set for the BQ769x2 to control DCHG and DDSG. Changes will include:

- Turn off the charge pump.
- Enable REG1 to an appropriate voltage.
- Enable the pre-regulator if used.
- Set the DCHG and DDSG pins for output with the proper polarity for the drivers used.
- Enable the FETs by setting data memory or with the FET_ENABLE command when desired.

The following settings show an example of changes for basic low-level testing with 3.3-V REG1 and DCHG and DDSG high when on.

```
Settings:Configuration:REG12 Config     0x0D
Settings:Configuration:REG0 Config      0x01
Settings:Configuration:DCHG Pin Config  0xA2
Settings:Configuration:DDSG Pin Config  0xA2
Settings:FET:Chg Pump Control           0x00
```

Additional configuration for cells used and the desired device operation are needed. In testing for this application report additional changes were made for protection conditions. FETs were enabled as needed, SLEEP was generally disabled so the CHG would not switch with SLEEP.

An example circuit configuration for the BQ76952 is shown in Figure 3-1, this circuit is common for the driver options described in this application report. The charge pump is not used and CP1 is tied to BAT, so the BQ769x2 will draw the extra current noted in the data sheeet until the charge pump is disabled in the configuration. DSG and CHG are not used and are left open. PACK is pulled up with 10 kΩ. Both regulators are shown connected although only REG1 is used in testing. DDSG and DCHG are used for output and are not available for other functions. The schematic shows 16 cell support but should be configured for the cell count required. Testing for this application report was conducted at 40 V.

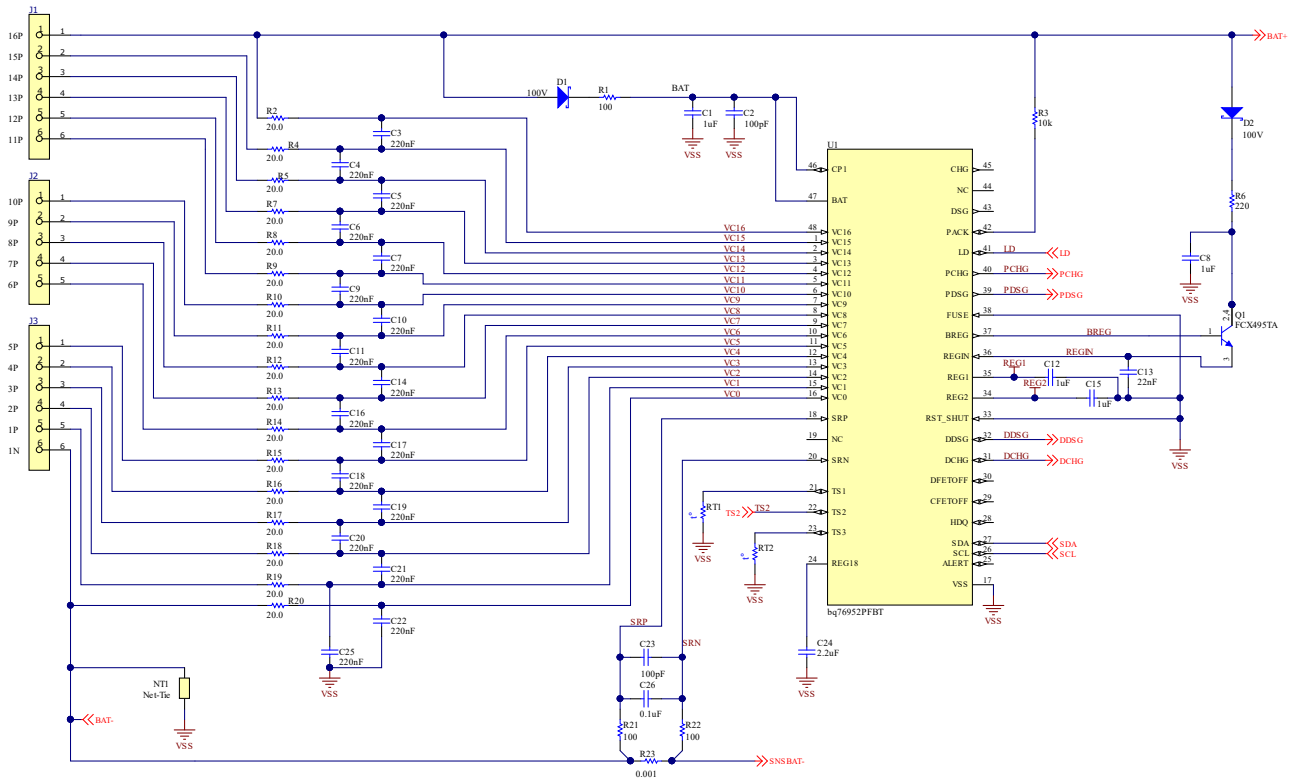

Figure 3-1. BQ76952 Monitor Schematic for Low-Side Switching

4 Logic Level FETs

Some designers will recognize that REG1 can be set to 5 V and may want to consider the use of logic level FETs controlled directly by the DDSG and DCHG outputs. DDSG and DDCHG provide the switching function and 5 V as the V_{FETON} level. Test conditions for the digital outputs show V_{OH} and V_{OL} with 5-mA source or sink current which is encouraging, but the test condition load is 10 pF and no rise or fall time is specified.

Data memory configuration would change for REG1 at 5 V.

```
Settings:Configuration:REG12 Config     0x0F
```

While a designer might buffer the signals with a more capable 5-V driver, this application report shows examples of direct drive of the FETs with the digital outputs. CSD18535KCS FETs are used which have a R_{DSON} specification at 4.5 V. Figure 4-1 shows an example schematic for driving FETs with the DDSG and DCHG signals. The 51-Ω resistors are used to isolate the gates from each other when using parallel FETs to avoid high frequency oscillation. With a single FET the 51-Ω resistors were retained in this test circuit and add to the drive resistance.

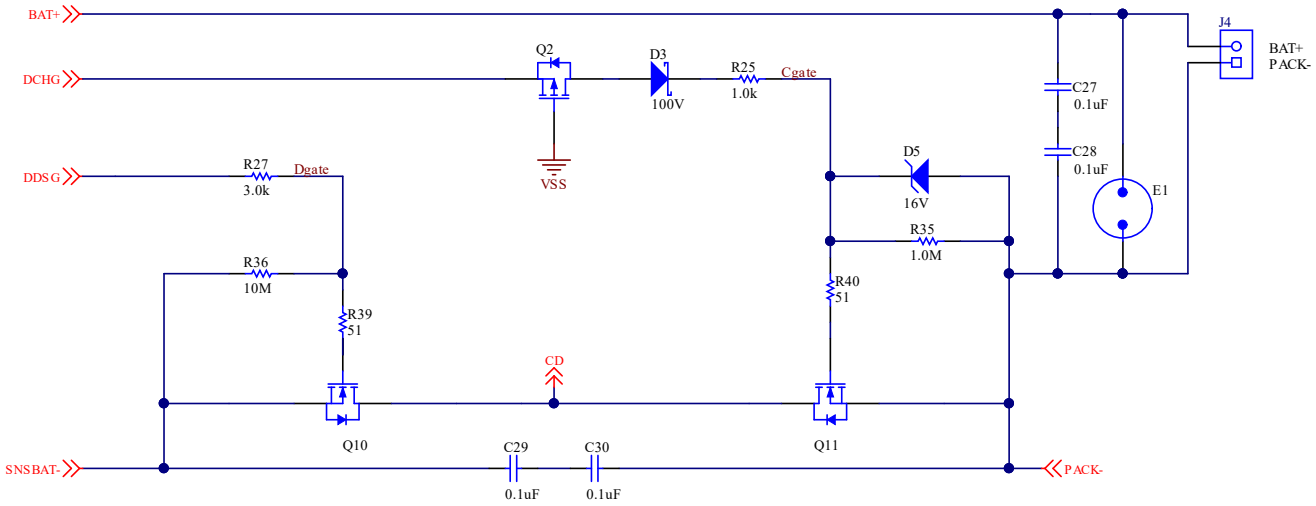

Figure 4-1. DDSG and DCHG as Drivers with Logic Level FETs Schematic

When driving a single discharge FET with a 1-kΩ gate resistance R27, ringing of the driver was observed in Figure 4-2. This is an effect of the FET used, the trace parasitics, and the inability of the driver to maintain a suitable drive current for the FET. With four FETs the additional load on the driver from the additional Ciss slows the turn on and avoids the ringing. Figure 4-3 shows however that the load pulls down the regulator voltage temporarily. If this is undesired the capacitor on REG1 can be increased. The test waveforms in this section do not include an increased REG1 capacitance.

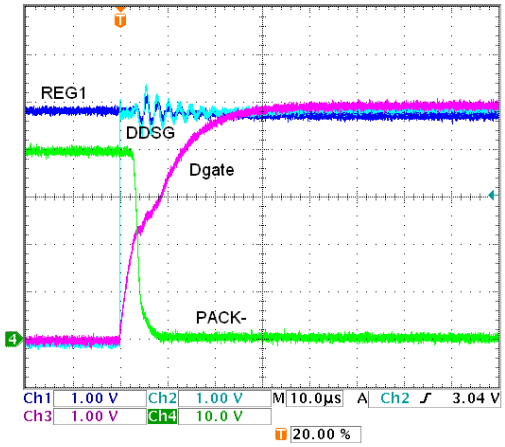

Figure 4-2. Discharge FET Turn On with One FET, 1-kΩ Gate Resistance

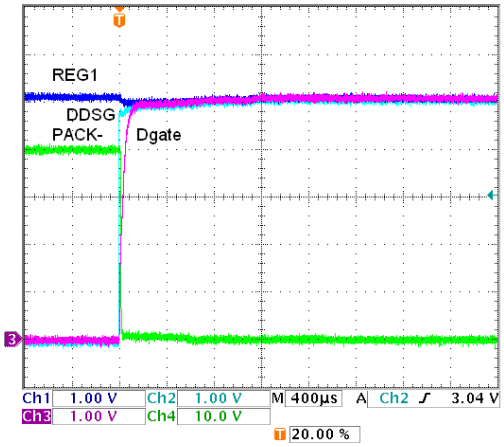

Figure 4-3. Discharge FET Turn On with Four FETs, 1 kΩ, REG1 Droop

With the board topology established, the adjustment available to the designer to avoid gate ringing is the gate resistor R27. Increasing the resistance slows the FET turn on and avoids the ringing. A 3-kΩ value was selected, turn on and turn off with a single FET is shown in Figure 4-4 and Figure 4-5.

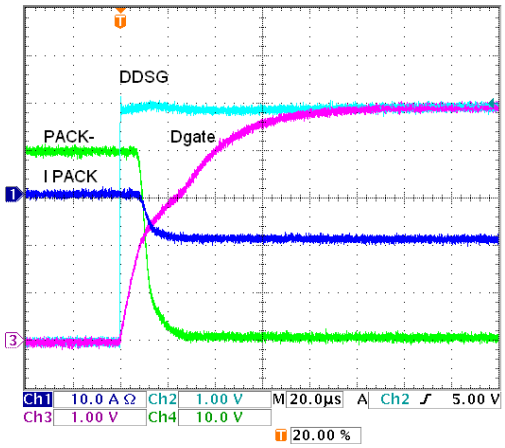

Figure 4-4. DDSG Drive, One FET, On, 3-kΩ Gate Resistor

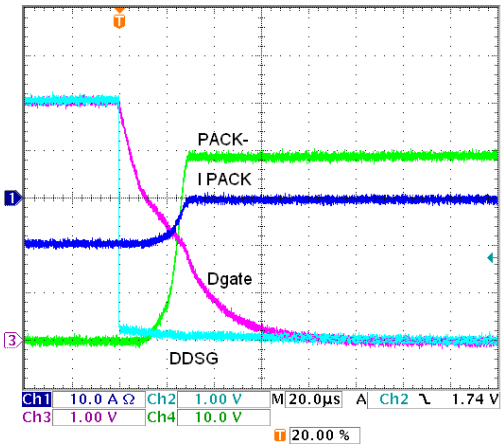

Figure 4-5. DDSG Drive, One FET, Off, 3-kΩ Gate Resistor

When the charge FET is off, the charger is free to pull the PACK- terminal below the battery negative which is GND. When DCHG goes high the charge FET will turn on. Voltage swing is small in this case and driver ringing was not observed in this test. An example of single charge FET turn on using a 1-kΩ gate resistor is shown in Figure 4-6. Turn off is shown in Figure 4-7. Note that DCHG goes low quickly since it does not drive the gate, current is blocked to the driver by D3. The gate-source resistor R35 turns off the FET, in this test it is 1 MΩ so turn off is slow. Also notice that the 10M scope probe pulls up on the Cgate signal creating a voltage divider and holding the gate slightly above the PACK- signal.

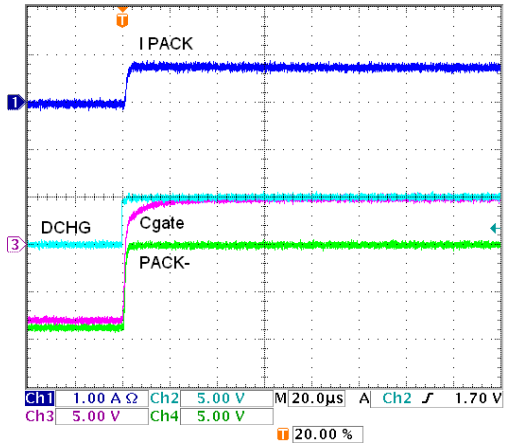

Figure 4-6. DCHG Drive, One FET, On

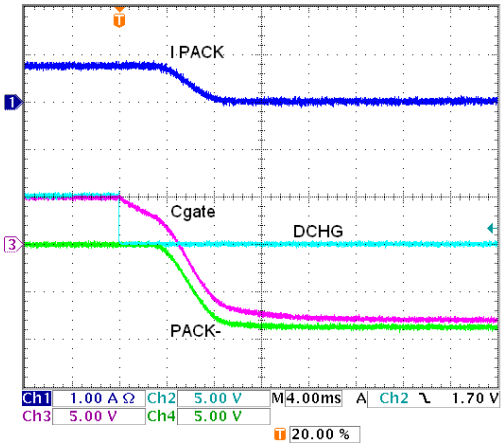

Figure 4-7. DCHG Drive, One FET, Off

Figure 4-8 shows a schematic with four FETs. With the larger combined gate capacitance a 1-kΩ resistor is used for R27. Since a slow turn off is undesired for discharge due to the higher discharge currents expected, a Schottky diode is used to provide a parallel resistance path with R28 for turn off . The diode D6 blocks current to the gates during turn on but allows the DDSG to pull current from the gates through both R27 and R28 during turn off.

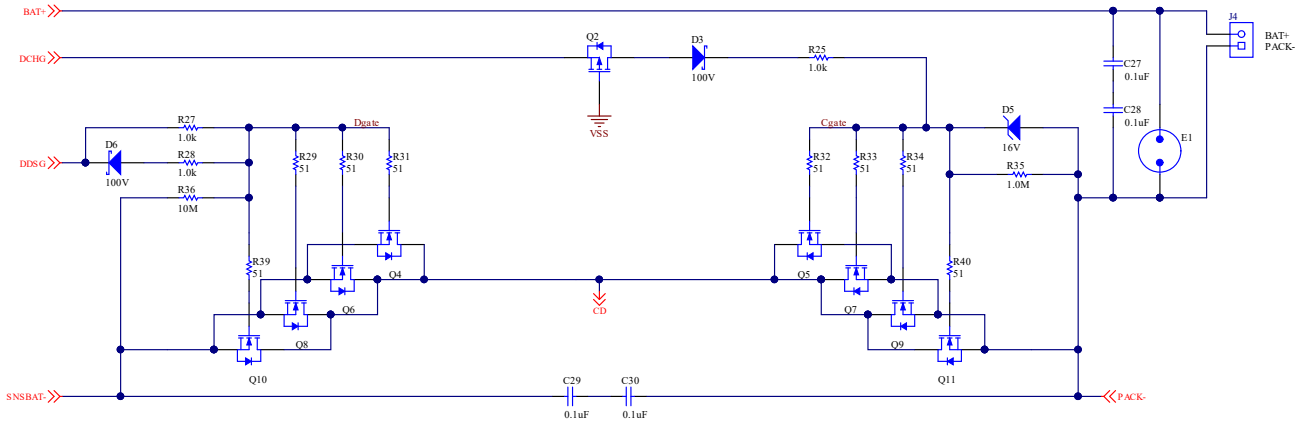

Figure 4-8. DDSG and DCHG as Drivers with Four Logic Level FETs Schematic

With four FETs and a 1-kΩ drive resistance the DDSG does not ring in this test. A droop can be seen in the DDSG in Figure 4-9 as the FETs come on. Figure 4-10 shows turn off with the added D6 Schottky and R28 1-kΩ path of Figure 4-8. R28 could be made smaller for faster turn off , or a PNP transistor circuit would require only control current from DDSG.

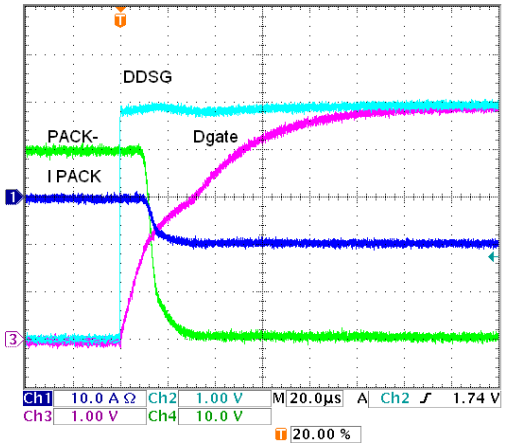

Figure 4-9. DDSG Drive, Four FETs, On, 1 kΩ, Schottky

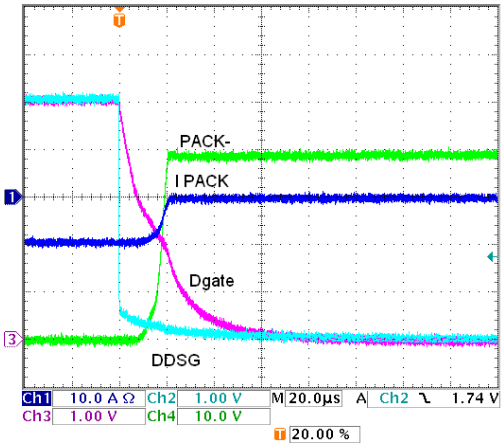

Figure 4-10. DDSG Drive, Four FETs, Off, 1 kΩ, Schottky

Turning on CHG with four FETs is shown in Figure 4-11. Turning off the four FETs accomplished by the 1-MΩ R_{GS} is shown in Figure 4-12. Turn off is slow due to that large resistance used to limit current while the FET is on.

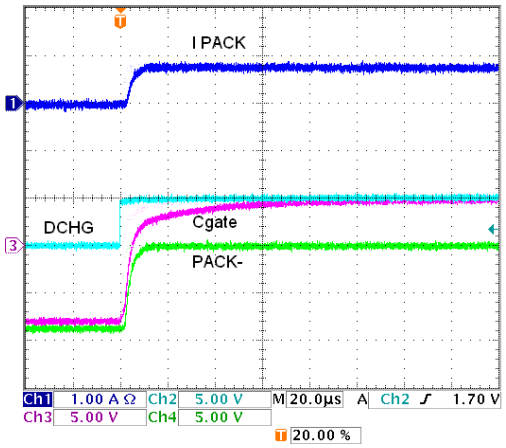

Figure 4-11. DCHG Drive, Four FETs, On, 1 kΩ, 1-MΩ R_{GS}

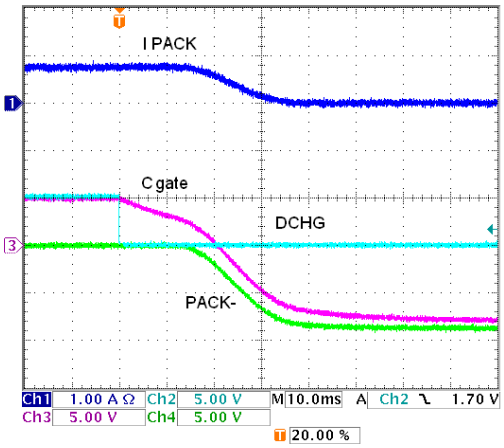

Figure 4-12. DCHG Drive, Four FETs, Off, 1 kΩ, 1-MΩ R_{GS}

When faster turn off is desired, there is little voltage margin for circuits with the REG1 voltage and logic level FETs. One solution is to use a smaller R_{GS} resistor R35. Using a 91-kΩ R_{GS} is shown in Figure 4-13 and Figure 4-14. Turn on is similar to the larger R_{GS} waveform, while turn off is much faster. With the 5-V supply this solution requires approximately 50 µA additional current while the charge FET is on.

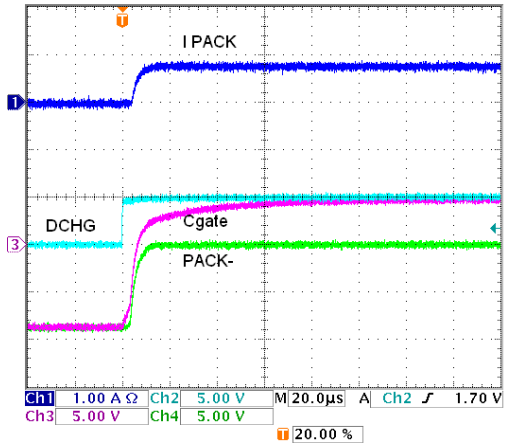

Figure 4-13. DCHG Drive, Four FETs, On, 91-kΩ R_{GS}

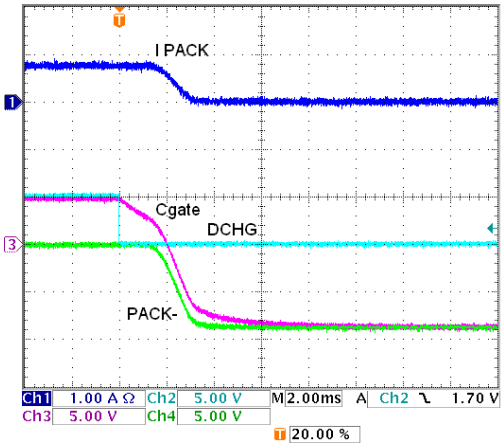

Figure 4-14. DCHG Drive, Four FETs, Off, 91-kΩ R_{GS}

When considering a logic level FET solution a designer should perform a tolerance analysis. With the tolerance on REG1 and the Schottky diode at D3, a sufficiently low R_{GSON} FET should be used.

5 FET Driver Implementation

An IC FET driver will provide the level shift from logic level signals to an appropriate gate drive level with a suitable output stage. The implementation in Figure 5-1 uses the UCC27524 dual noninverting FET driver. One driver is used for turn on and off of the discharge FET, the other for turn on of the charge FET. Turn off of the charge FET is provided by R_{GS} or a circuit on the gate. The UCC27524 is a very capable driver designed to switch gates very quickly in switching regulator or other applications. Here as a load switch a series resistor will be needed to slow gate switching to avoid a large inductive response during turn off of a high current event such as overcurrent or short circuit protection. U2 is a linear regulator used in this test, it is blocked from discharging during a battery short circuit by D12, and the input is filtered with R68 and its input capacitors. Another suitable source could be used if available in an application. A circuit with four discharge and charge FETs is shown in Figure 5-2. The circuit configuration is much like the logic level FET circuit but the diode D3 is a conventional diode since there is more voltage available from the driver. Test circuits in this application report with high voltage drive options use CSD19536KCS FETs.

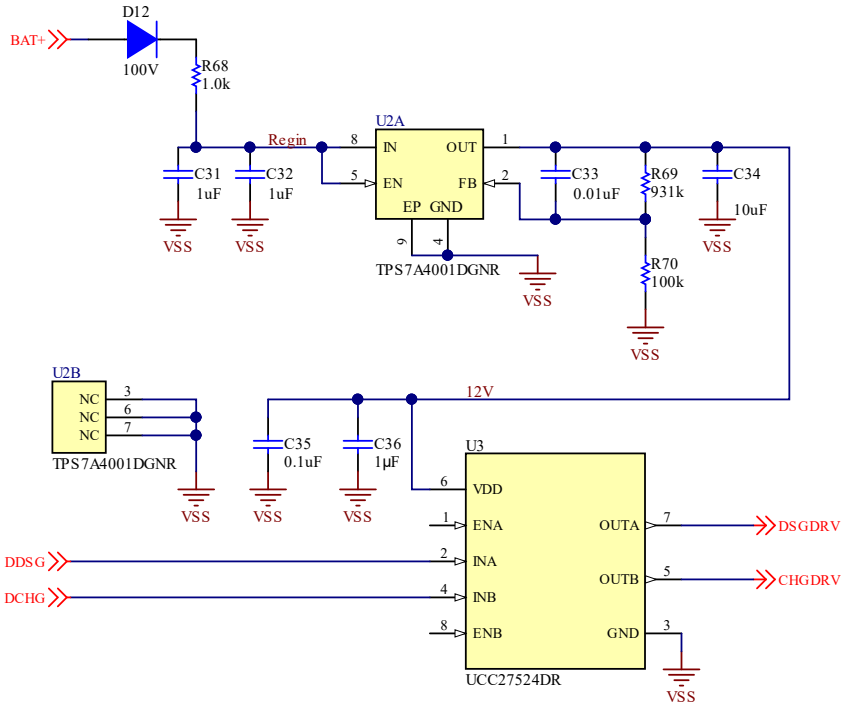

Figure 5-1. IC FET Driver with Regulator Schematic

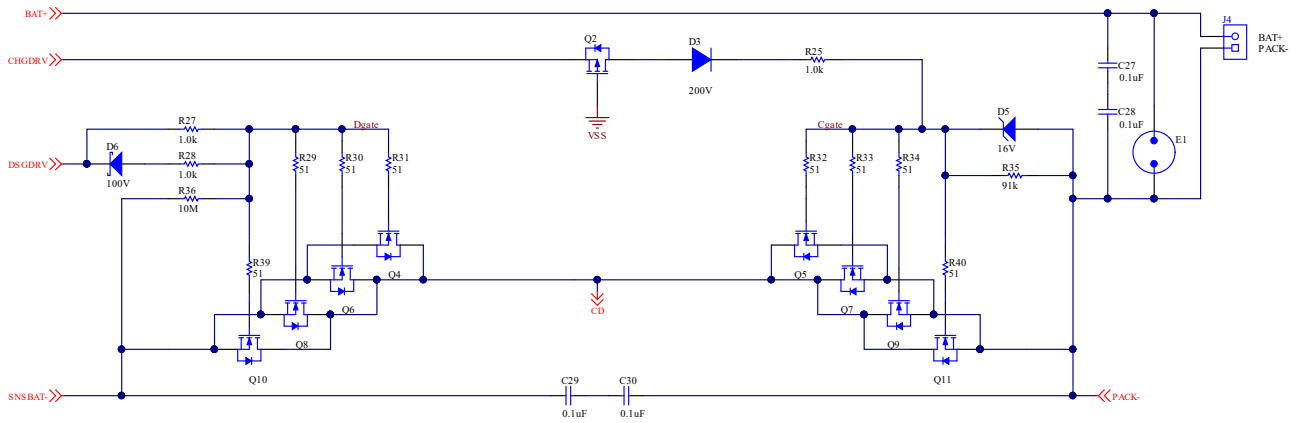

Figure 5-2. Four Discharge and Charge FETs For Driver Schematic

Figure 5-3 and Figure 5-4 show the very capable response of the driver, and the discharge FET switching without D6 and R28 in Figure 5-2. The gate voltage is slowed by the R-C response of the series resistor to the gates and the gate capacitance. Since the threshold voltage of the FETs is closer to GND than to the drive level note the delay between the DSGDRV signal fall and the current transition. Adding D6 and R28 does not change the turn on which is shown in more detail in Figure 5-5, but speeds up the turn off as shown in Figure 5-6. The R28 value may be adjusted for faster turn off. Switching of the charge FETs is shown in Figure 5-7 and Figure 5-8.

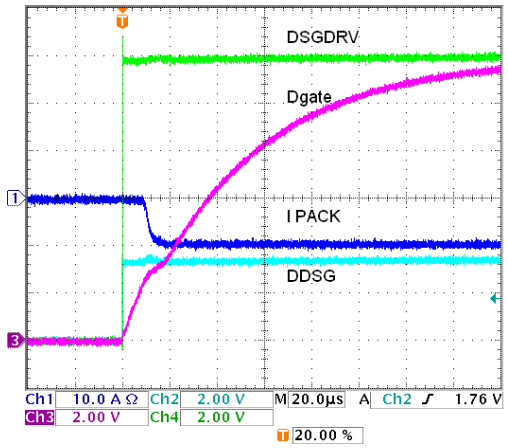

Figure 5-3. IC FET Driver, Four Discharge FETs, On

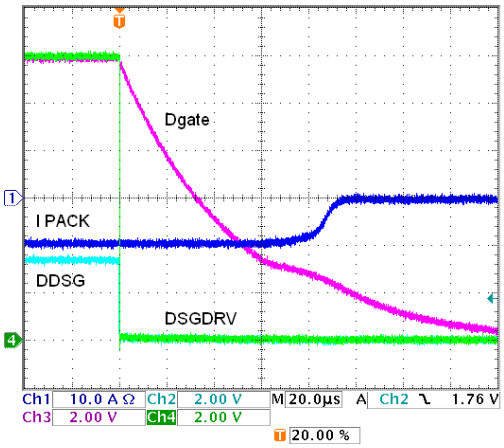

Figure 5-4. IC FET Driver, Four Discharge FETs, Off

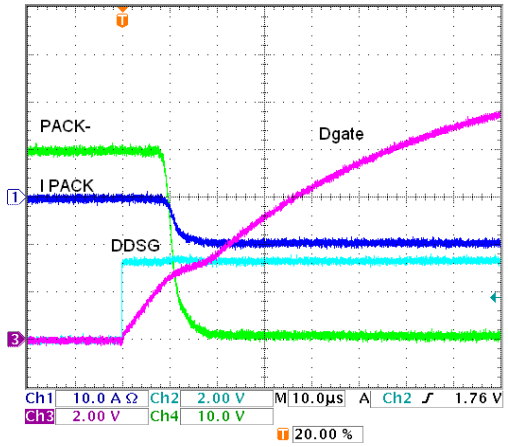

Figure 5-5. IC FET Driver, Four Discharge FETs, Schottky, On

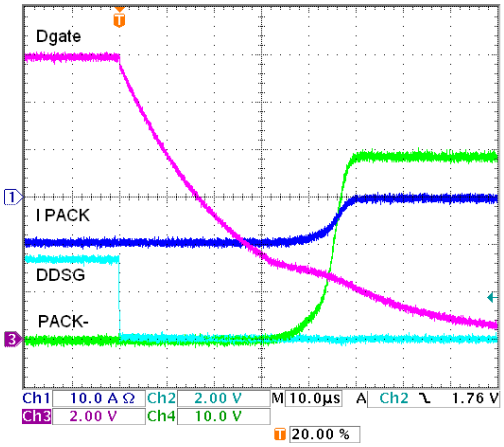

Figure 5-6. IC FET Driver, Four Discharge FETs, Schottky, Off

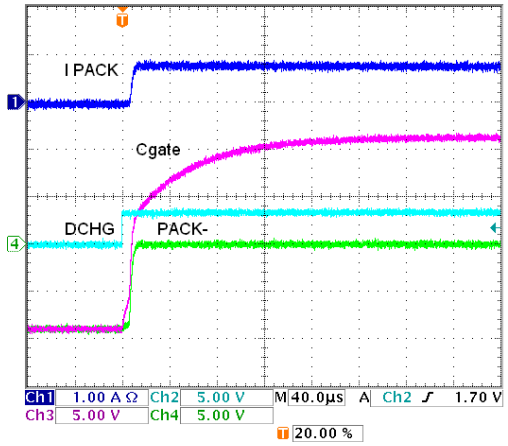

Figure 5-7. IC FET Driver, Four Charge FETs, On

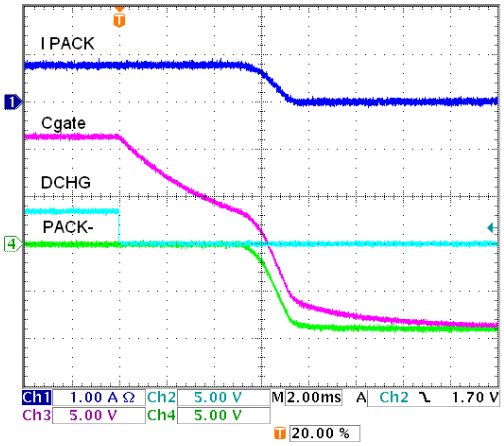

Figure 5-8. IC FET Driver, Four Charge FETs, Off, 91 kΩ

An implementation with 12 discharge and charge FETs is shown in Figure 5-9. With 12 FETs the total capacitance of the gates is larger. For DSG a smaller resistor is used. The individual gate resistors such as R29 are no longer a small part of the total resistance to the gate, so it may be more appropriate to replace these with ferrite beads, however testing used the 51-Ω resistors. In the charge path the PNP transistor is added to aid in turn off to avoid a small resistor which would be biased while CHG is on. Results are shown in Figure 5-10 and the following figures. Notice that with the PNP turn off circuit even though there are more FETs the charge FETs are off earlier in Figure 5-13 than with the pulldown resistor only in Figure 5-8. Turn off could be adjusted with the R24 base resistor value.

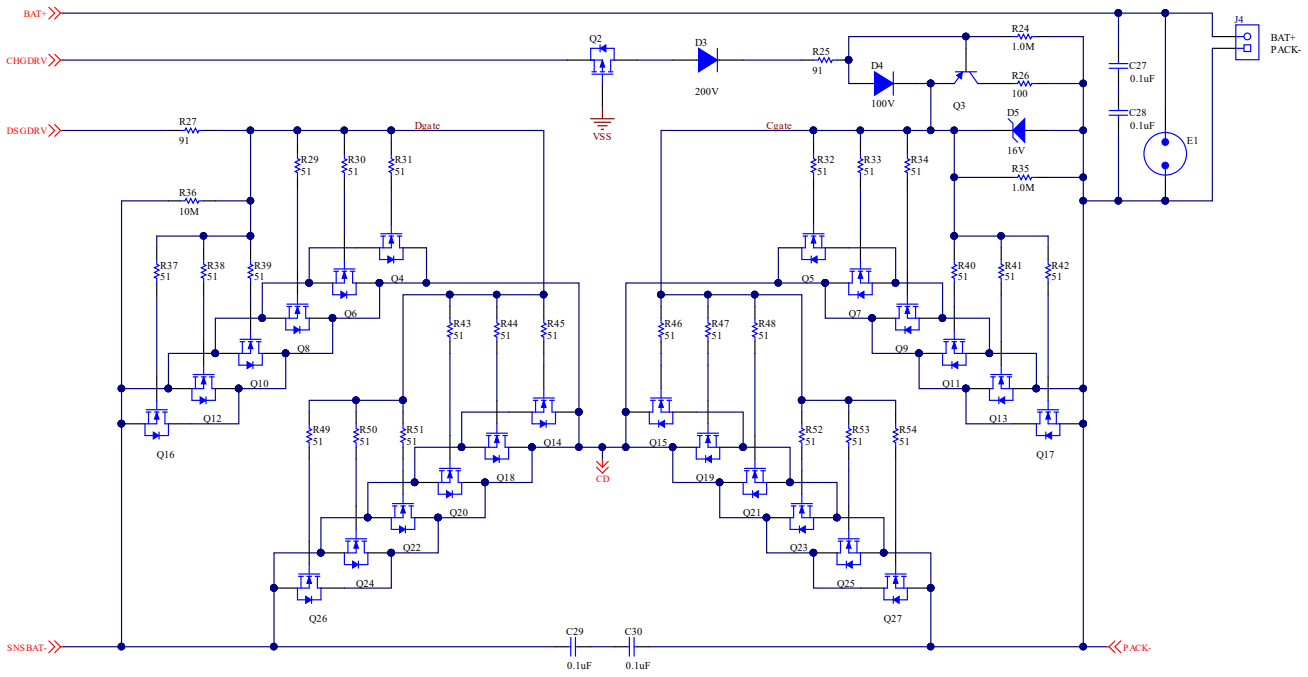

Figure 5-9. 12 Discharge and Charge FETs For IC FET Driver Schematic

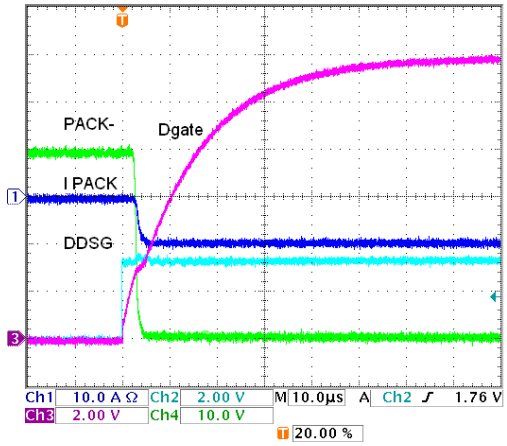

Figure 5-10. IC FET Driver, 12 Discharge FETs, On

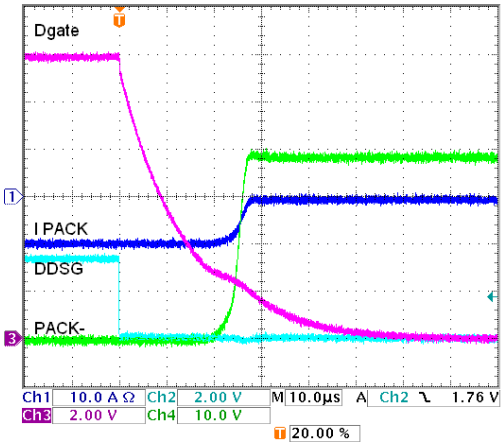

Figure 5-11. IC FET Driver, 12 Discharge FETs, Off

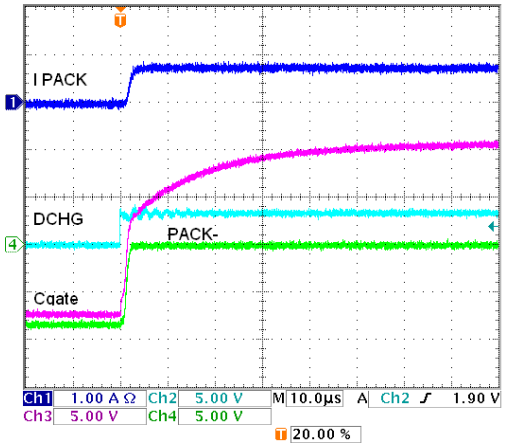

Figure 5-12. IC FET Driver, 12 Charge FETs, On

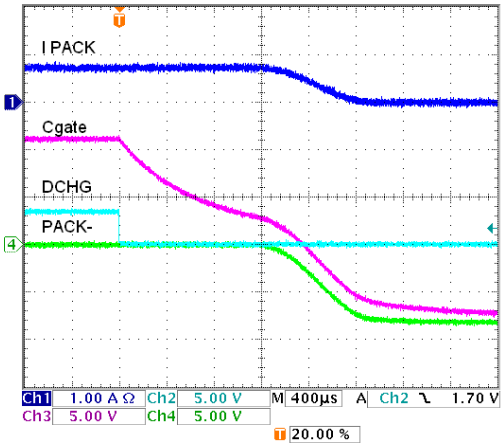

Figure 5-13. IC FET Driver, 12 Charge FETs, Off

When switching multiple FETs it is important to check the supply during the switching. Figure 5-14 shows the 12-V regulator output when the 24 FETs are turned on. The current pulls down the regulator input which is made up over time. The regulator has sufficient headroom so that the dip is not significant, the regulated voltage remains constant.

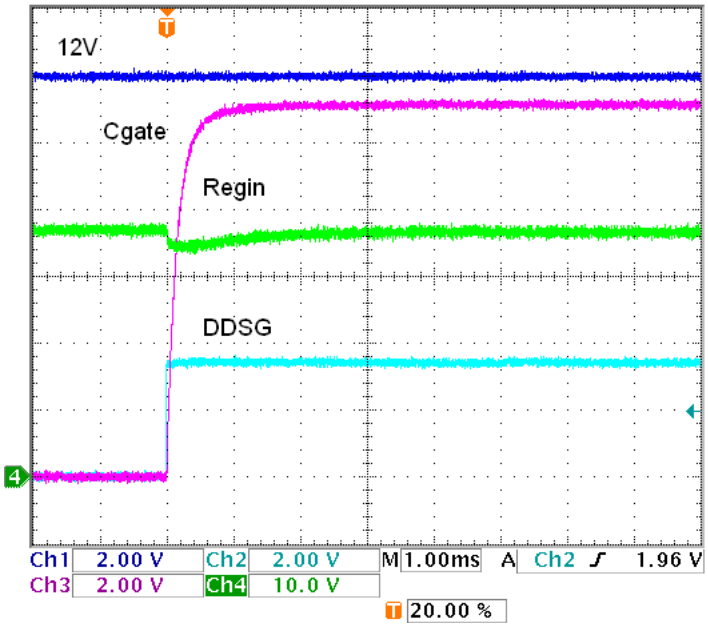

Figure 5-14. 12-V Power When 24 FETs Switch On

6 Transistor Driver Implementation

While an IC FET driver is very capable, there are instances where the user does not need the high performance of the integrated driver and may choose to implement a driver with transistors. The same voltage ranges for the power FET gates must be supported by the circuit. The logic level of the DDSG and DCHG signals must be translated to the higher gate voltage for the power FETs. Many transistor designs are possible. If the input polarity for the transistor drivers are different, adjust the polarity of the DDSG and DCHG in the BQ769x2 configuration as needed. An example test circuit is shown in Figure 6-1. This circuit also uses a simple regulator with a Zener to a NPN emitter follower for the "12 V" driver voltage VFET. R71 and C68 filter transients on the BAT+ to avoid possible coupling to the VFET output. The VFET load is typically small, but select the R71 value and power rating for the continuous and surge currents selected for the design. While the circuit implementation is simple, the 280 uA at 40 V to bias the Zener may lead a designer to a more sophisticated design. The discharge driver uses a single FET Q36 to provide level shifting to the VFET voltage level. Since Q36 inverts the signal, its input is biased high so that the driver is off when VFET voltage is present but the DDSG signal is not configured. DDSG must not go above its ABS MAX of 6 V, so a voltage divider is used. The driver requires a bias current in R74 when the driver is off. The level shifted signal at the Q36 drain drives the FET gates through emitter followers Q34 and Q37. The emitter follower configuration will drive current through the FET switching area but will limit the voltage from reaching the VFET and GND levels.

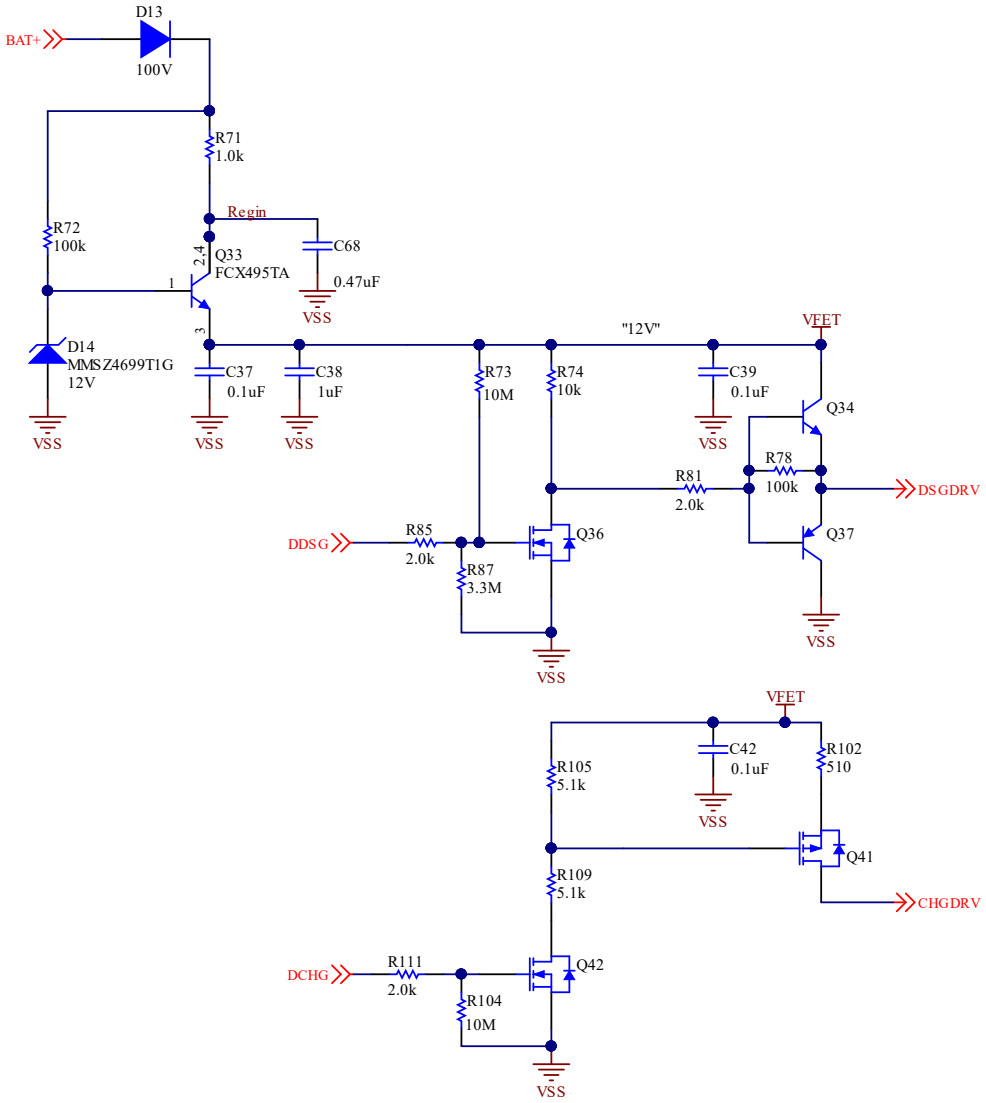

Figure 6-1. Transistor Driver Example Schematic

With the inverted discharge driver the DDSG polarity must be inverted for this driver.

```
Settings:Configuration:DCHG Pin Config  0x22
```

The charge driver is noninverting and does not drive low since a blocking diode is used. When DCHG is high Q42 turns on Q41 to provide the VFET voltage for the charge power FET gates. Output current is limited by R102. When DCHG is low Q42 is off, R105 turns off Q41, and the power FET R_{GS} resistor or an additional gate circuit will pull the power FET gate low.

Figure 6-2 shows a single discharge and charge FET circuit structure controlled by the transistor FET driver. The P-channel device Q2 is not included with the FETs since its function is provided by the transistor driver circuit Q41.

CSD19536KCS FETs were used for the testing of the transistor driver circuit. Results for switching the single FETs are shown in Figure 6-3 to Figure 6-6. The ripple in the discharge turn on indicates the layout may be sensitive to this turn on speed and a larger R27 or circuit improvement may be desired.

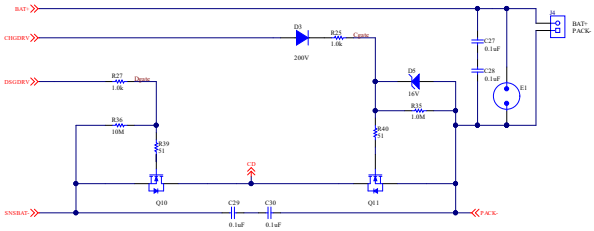

Figure 6-2. Single Discharge and Charge FETs Used with Transistor Driver Schematic

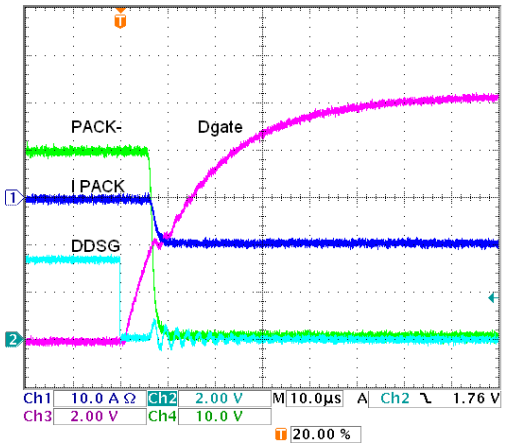

Figure 6-3. Transistor FET Drive, One Discharge FET, On

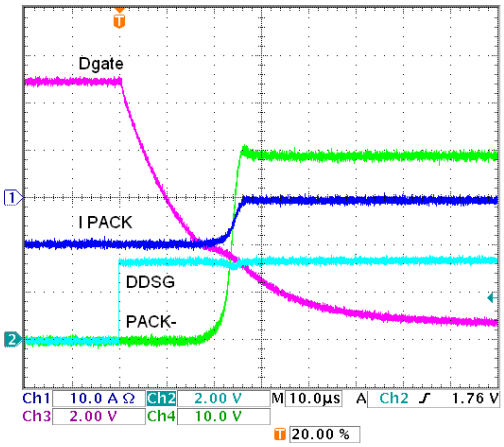

Figure 6-4. Transistor FET Drive, One Discharge FET, Off

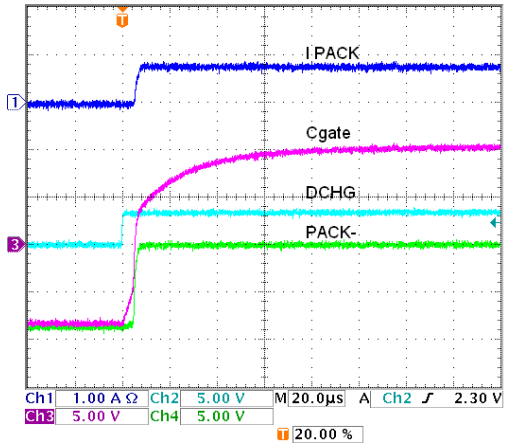

Figure 6-5. Transistor FET Drive, One Charge FET, On

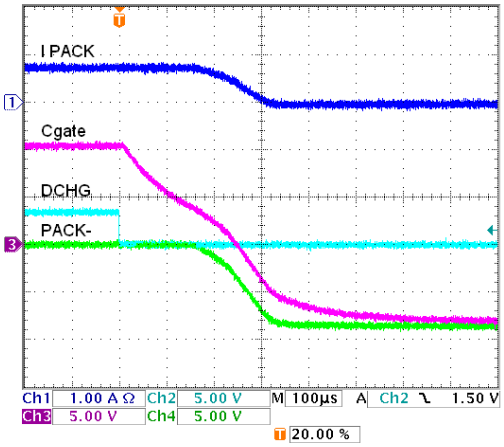

Figure 6-6. Transistor FET Drive, One Charge FET, Off

With many FETs just as with the IC FET driver resistances will need to be reduced to the gate to provide suitable switching. Figure 6-7 shows a test circuit with 12 each discharge and charge FETs used with the transistor driver. The circuit is much like the IC FET driver circuit but Q2 is removed since the transistor charge driver has a P-channel output device. Figure 6-8 to Figure 6-12 show the test results. Figure 6-13 shows the improved switching of reducing R24 to 91 kΩ for faster charge turn off.

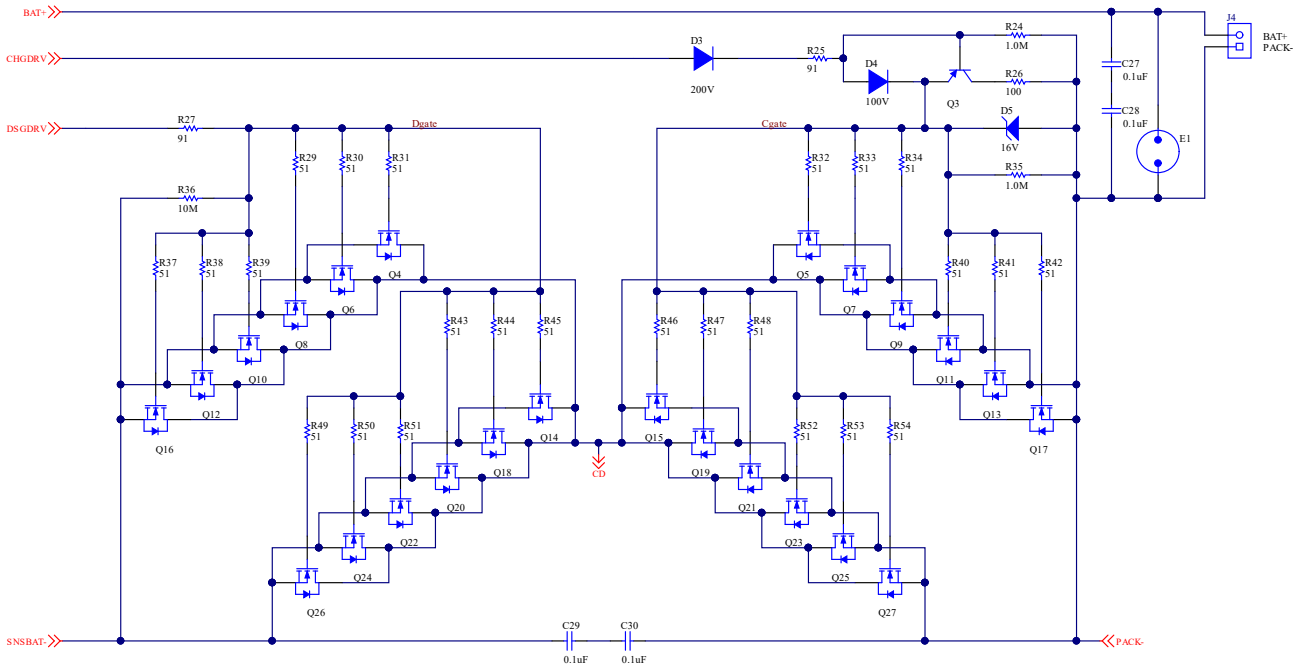

Figure 6-7. Twelve Discharge and Charge FETs Used with Transistor Driver Schematic

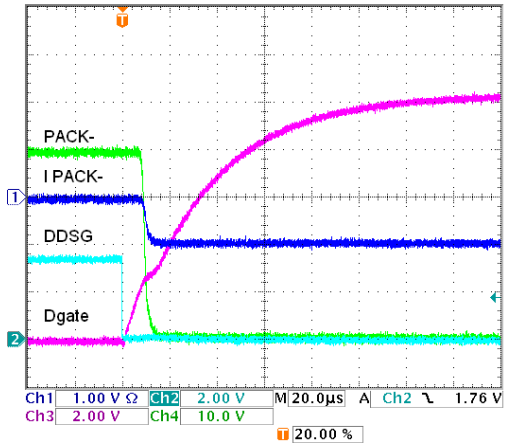

Figure 6-8. Transistor FET Drive, 12 Discharge FETs, On

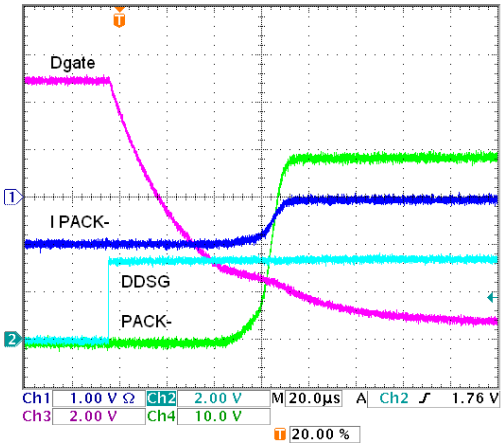

Figure 6-9. Transistor FET Drive, 12 Discharge FETs, Off

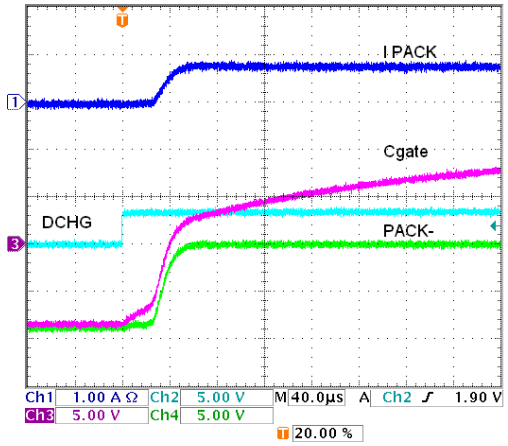

Figure 6-10. Transistor FET Drive, 12 Charge FETs, On, Detail

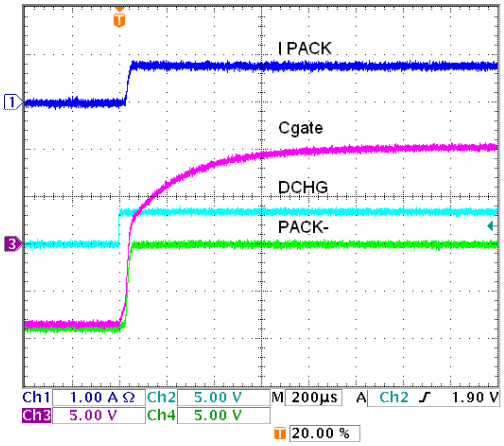

Figure 6-11. Transistor FET Drive, 12 Charge FETs, On

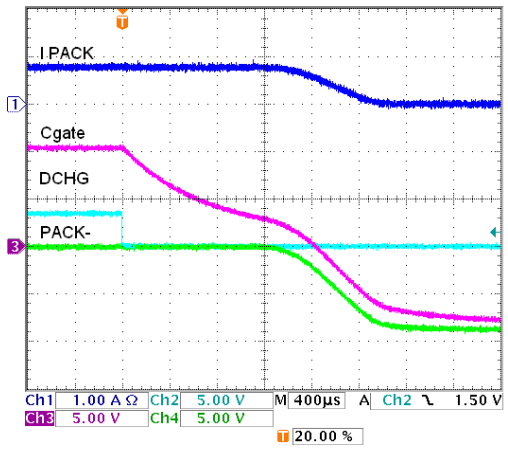

Figure 6-12. Transistor FET Drive, 12 Charge FETs, Off, PNP, 1 MΩ

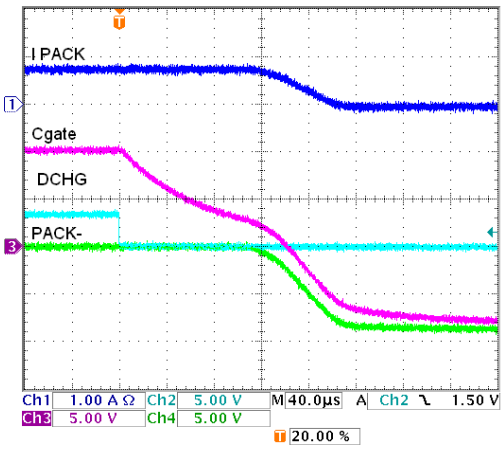

Figure 6-13. Transistor FET Drive, 12 Charge FETs, Off, PNP, 91 kΩ

Again checking the "12 V" VFET supply during switching the 24 FETs on, a dip is observed during turn on as shown in Figure 6-14. The DC level of the "12 V" VFET voltage is below 12 V due to tolerance of the Zener and the base-emitter drop of the transistor Q33.

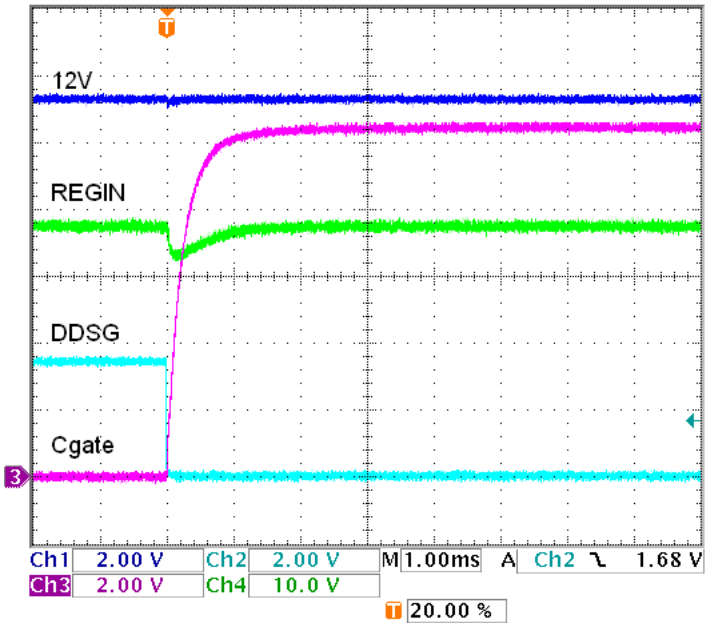

Figure 6-14. 12-V Emitter Follower with 24 FETs Turn On

The circuit above has an inverting driver for DSG and biases the input at all times. The emitter follower structure does not drive to the full voltage or GND. Other topologies are possible. Figure 6-15 shows an alternate discharge driver using a push-pull driver. This uses the DDSG polarity high when on and requires bias current on when the driver is on. It does have a shoot through current during switching. In this case switching is infrequent and shoot through current is limited by R101. Example switching of two discharge FETs is shown in Figure 6-16 and Figure 6-17.

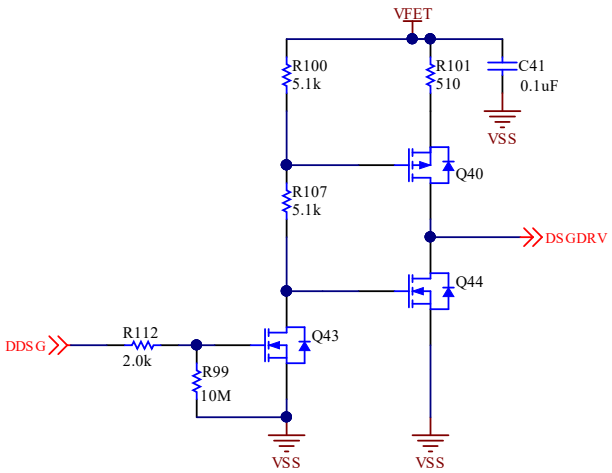

Figure 6-15. Alternate DSG Transistor FET Driver Example Schematic

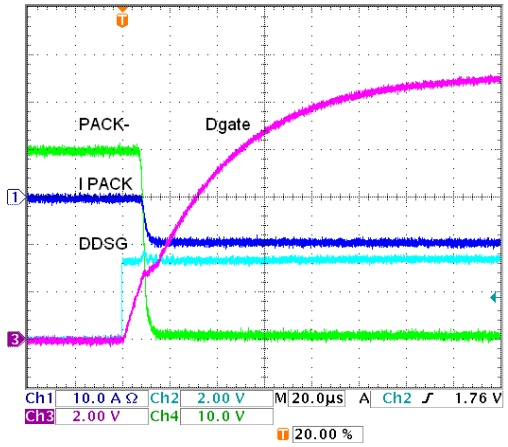

Figure 6-16. Transistor FET Drive, Two Discharge FETs, On

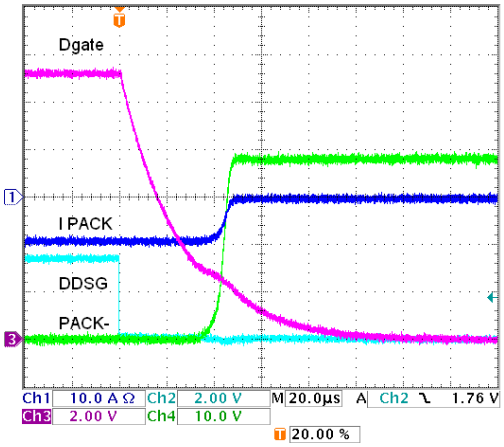

Figure 6-17. Transistor FET Drive, Two Discharge FETs, Off

The load of the driver on the "12 V" VFET can be observed at the filtered input Regin. Shoot through current of the alternate driver is provided by the capacitors and is not apparent in the waveforms of Figure 6-18 and Figure 6-19.

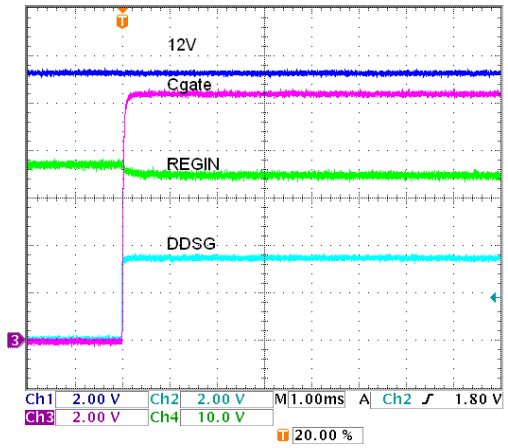

Figure 6-18. 12-V with Push-Pull Driver Turn On

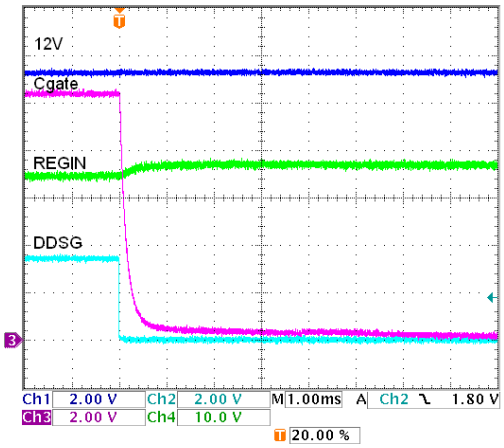

Figure 6-19. 12-V with Push-Pull Driver Turn Off

7 Controlling LD

With a high-side FET design the LD pin will normally connect to PACK+ and is used for a drive reference for DSG, for a wake-up signal, and for current recovery if selected. The data sheet indicates that when the driver is not used LD may be tied to PACK+ through a resistor or may be pulled to VSS. If pulled high it will prevent the part from entering shutdown. If connected to VSS it cannot be used to control current recovery. An MCU could recover the OCD event using the host command. Since the device provides a pullup to test for load removal, a circuit can be designed to control LD if desired. The MCU could control the circuit if not providing recovery by command, or if no MCU is available it could be controlled by the PACK- pin level as shown in Figure 7-1. When a load is present on the PACK terminals after a fault which holds the PACK- near PACK+, LD is held low. If configured appropriately recovery from the current fault is prevented. The circuit provides a pulldown on the PACK-, if the load is removed such that this pulldown can turn off the signal FET Q32, LD will be released and the BQ769x2 will pull LD high allowing current recovery. Note that the circuit will provide a pulldown on PACK- which will tend to keep the PACK voltage near normal levels, this will be a leakage on the battery while the load is present on the PACK terminals. When CHG remains on, the gate drive voltage will pull up the PACK- voltage and may prevent turn off of Q32 depending on the values of the R66 and R67 resistors.

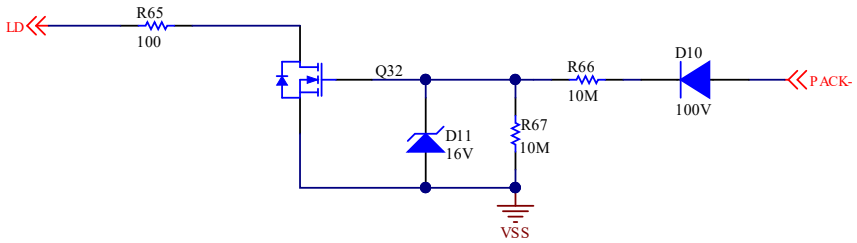

Figure 7-1. LD Circuit for Load Sensing Schematic

Figure 7-2 shows an OCD event with the test circuit. DDSG is turned off, the load pulls PACK- up, LD is pulled down by the circuit. The charge FET gate Cgate is also pulled up by PACK- and discharges to the PACK- level over time. When the load is released but the part stays awake with DCHG on, the driver biases up PACK- to near the driver level. Depending on the divider resistors selected for R66 and R67 the circuit may hold LD low, and recovery will not occur until a charger is attached as shown in Figure 7-3. When the BQ769x2 is asleep, if CHG is off during sleep the PACK- can fall after the load is removed and recovery may happen quickly as shown in Figure 7-4. If the load is removed after the current stops after the Protections:Load Detect:Active Time, the part will retry after the Protections:Load Detect:Retry Delay as shown in Figure 7-5. If necessary the part will retry until the Protections:Load Detect:Timeout.

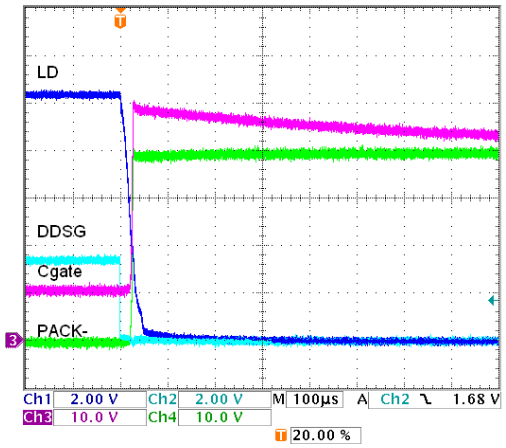

Figure 7-2. OCD with LD Controlled

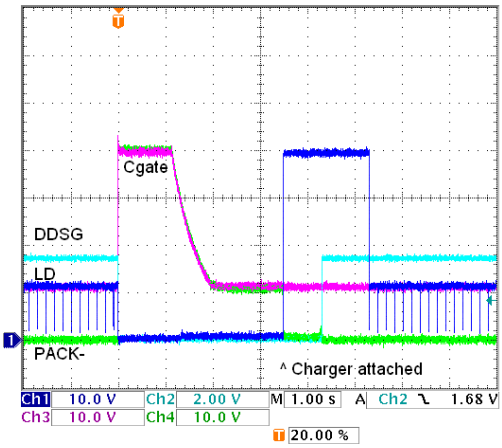

Figure 7-3. OCD with Recovery From Charger Connection

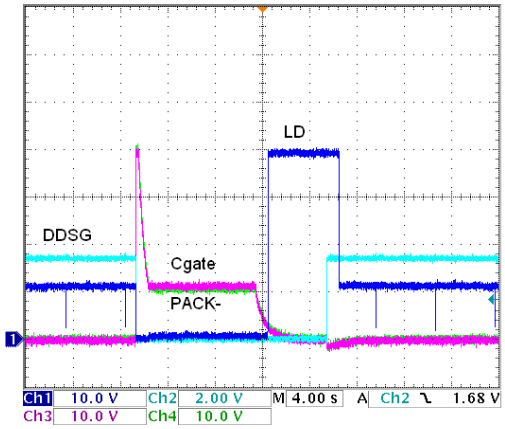

Figure 7-4. OCD During Sleep with Recovery

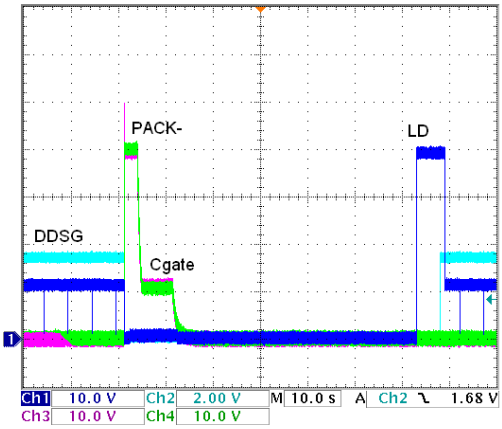

Figure 7-5. OCD During Sleep with Recovery On Retry

With low-side switching and LD tied to VSS or LD controlled by the cirucit above, wake-up will need to come from TS2. A simple circuit to do this is shown in Figure 7-6. When the "Wake" signal is pulled up toward PACK+, TS2 is pulled down causing the BQ769x2 to wake up. If the WAKE signal is connected to PACK+ directly, the circuit will provide a continuous drain on the battery. Adjust the value of R80 and provide transient protection as needed or use an alternate circuit suitable for the application.

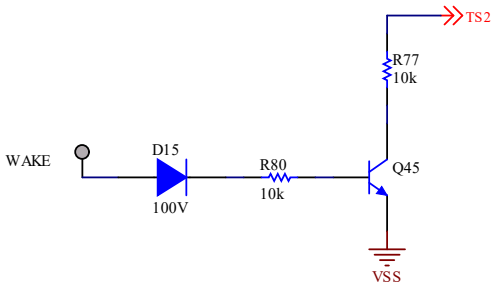

Figure 7-6. Wake Circuit Example Schematic

8 Precharge and Predischarge for Low-Side FETs

The DDSG and DCHG outputs from the BQ769x2 combine the pre and main FET drive signals. If the designer wants precharge and or predischarge features, options include controlling the precharge or predischarge path from the host and using logic to inhibit the main FET driver when the presignal is applied. When using the host, the predischarge and precharge FET drivers may look like the main FET drivers described in earlier sections.

The precharge and predischarge outputs of the BQ769x2 are only referenced to the BAT voltage, a digital version referenced to VSS is not available. To use precharge and predischarge with a low-side implementation a circuit is needed to translate the voltage from the high side to the low-side FETs, an example is shown in Figure 8-1. P-channel signal FETs (Q28, Q29) are used to create a current which will flow to resistors (R51, R52) at the low side to turn on the FETs. Zener diodes (D8, D9) limit the voltage to the FET gates. Resistors in the drain path (R58, R60) drop the voltage to the Zener diodes limiting the drain current. If desired current could be limited by resistors in the source path. The current will vary across the battery voltage. The ratio of the resistors will determine the voltage for the gate of the low-side FET. The lower resistor must also be sized for turn off. Since PACK- can swing below GND and above PACK+, a diode (D7) is included to avoid current through these components.

The circuit in Figure 8-1 shows the signal translation circuit and precharge and predischarge FETs with 4.7-kΩ resistor-limited current paths for precharge and predischarge. This is not a complete system solution since logic is not included to allow these circuits to operate without the main FETs coming on at the same time. For example the main discharge FET would be enabled only when DDSG is active and the PDSGgate signal was low. The 4.7-kΩ resistors would also need to be adjusted for the desired current and allowed power in the design.

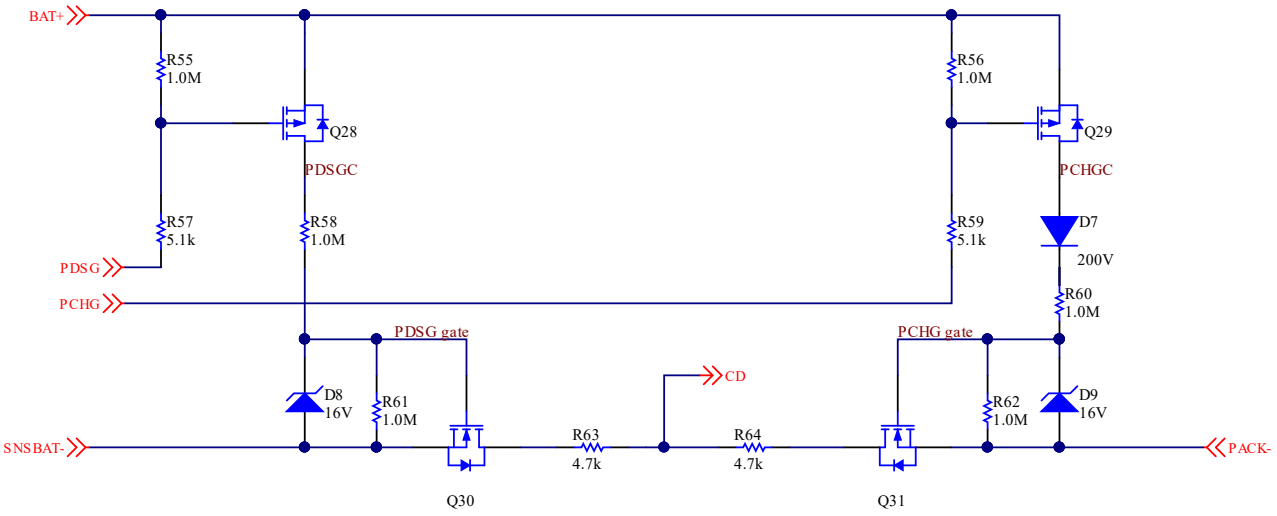

Figure 8-1. Precharge and Predischarge Test Circuit Schematic

PDSG and PCHG are high impedance when off and pulled up by R55 and R57 for PDSG and R56 and R59 for PCHG. When PDSG and PCHG are active they pull to a voltage below the BAT level turning on Q28 and Q29 when appropriate. Connecting a scope probe to observe the PDSG and PCHG will generally pull down the signals and turn on the FETs, so these signals are not shown in the figures.

Basic operation of the level shift circuit is shown in Figure 8-2 and Figure 8-3 for the precharge circuit. In this circuit the level shift controls the FET directly. In these waveforms DCHG is disconnected so the main charge FET remains off and PACK- remains below GND. The PCHG signal is not shown on the waveform since loading of the scope probe will pull down the high impedance output turning on the external FET. When the CHG signal goes low, the P-channel FET pulls up the PCHGC signal to the battery voltage raising the PCHG gate signal to the limit of the Zener. Since the path is current limited the charger voltage remains below the battery- voltage, the probe reference in the figures. With large resistors to keep the current small switching is slow, most notably on turn off. With reduced current in the path the slow switching may be suitable for the FET although small FETs are often used due to the low current. Use an appropriate technique for your design. When generating a logic level signal to control the main charge driver remember the switching speed as well as the large voltage variation of PACK-. Use a path referenced to VSS for logic controls. Also when considering this circuit remember

that PCHG and PDSG are referenced to the filtered BAT pin of the BQ769x2. If transients exist on the BAT+, consider filtering or limiting the V_{GS} voltage for Q28 and Q29 and consider the effect of glitches on logic circuits.

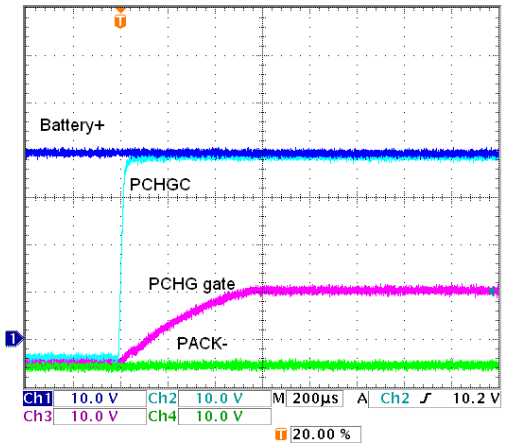

Figure 8-2. Precharge Turn On

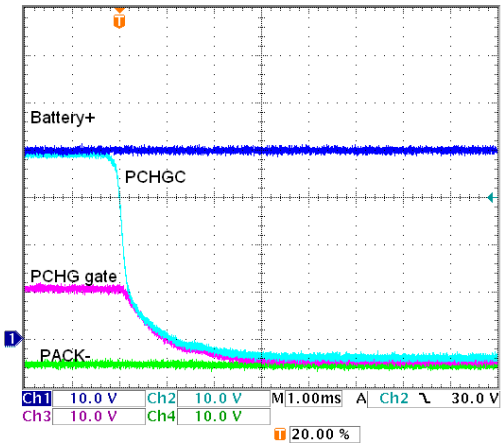

Figure 8-3. Precharge Turn Off

The predischarge path shown in Figure 8-1 is referenced to the sense resistor which will not move much from VSS and is accommodated by the FET gate threshold. Figure 8-4 shows the limitation of the test circuit without the logic control of the main discharge FET. PDSG turns on the PDSGC signal which turns on the PDSGgate and the predischarge path, but DDSG also goes high which turns on the main discharge FET pulling PACK- down immediately rather than with the current limited predischarge path. The level change in PACK- while low is from a temporary turn off of the DCHG signal during the predischarge cycle. The main discharge FET would need to be disabled by logic during the predischarge time for predischarge to be effective.

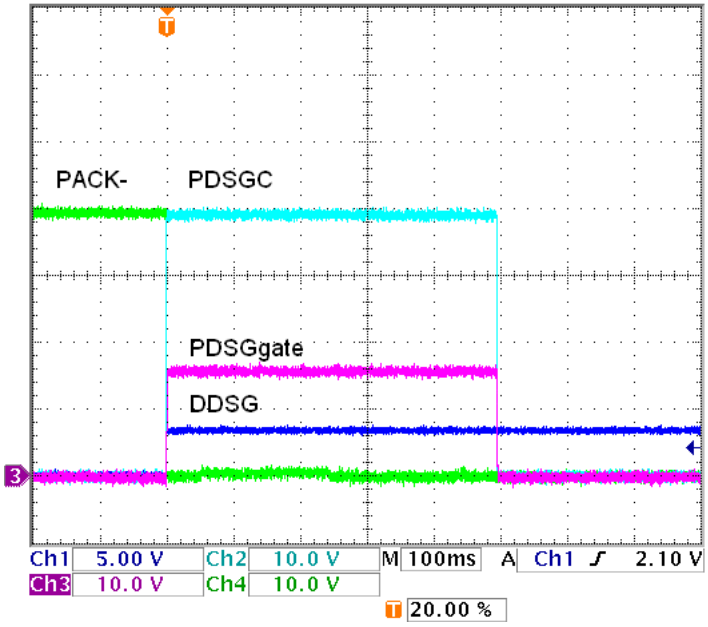

Figure 8-4. Predischarge Turn On

9 Summary

DDSG and DCHG are available for control when designing with low-side FETs and the BQ769x2 monitor devices. The designer has a variety of options in drivers depending on the need. DDSG and DCHG are logic signals not intended to drive FETS, but in limited cases the desiger may have success with an implementation. IC FET drivers are very capable but the designer may choose a transistor driver implementation with similar success. PDSG and PCHG are included in the DDSG and DCHG timing, if the user wants precharge and predischarge controlled by the BQ76952 some work must be done to separate the FET controls. The examples in this application report will help a designer select an approach for their low-side battery implementation.

10 References

- Texas Instruments, *BQ76952 3S-16S Battery Monitor and Protector Data Sheet*
- Texas Instruments, *BQ769142 3S-14S Battery Monitor and Protector Data Sheet*
- Texas Instruments, *BQ76942 3S-10S Battery Monitor and Protector Data Sheet*
- Texas Instruments, *BQ76952 Technical Reference Manual*
- Texas Instruments, *BQ769142 Technical Reference Manual*
- Texas Instruments, *BQ76942 Technical Reference Manual*
- Texas Instruments, *BQ76952EVM User's Guide*
- Texas Instruments, *BQ76942EVM User's Guide*
- Texas Instruments, *CSD18535KCS 60-V, N-Channel NexFET™ Power MOSFET*
- Texas Instruments, *CSD19536KCS 100-V, N-Channel NexFET™ Power MOSFET*
- Texas Instruments, *UCC2752x Dual 5-A High-Speed, Low-Side Gate Driver*
- Texas Instruments, *Fundamentals of MOSFET and IGBT Gate Driver Circuits*

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (January 2021) to Revision A (February 2022)	Page
• Revised title, added BQ769142 to Abstract	1
• Added to circuit descriptions in Section 2	6
• Added to description in Section 3	9
• Corrected FET direction in Figure 4-8, added to description in Section 4	11
• Corrected FET direction in Figure 5-2 and Figure 5-9	16
• Added resistor description to Section 6, corrected FET direction in Figure 6-7	21
• Added signal description to Section 8	29
• Add BQ769142 documents to Section 10	32

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