TPS92682-Q1 (HTSSOP) Functional Safety FIT Rate, FMD and Pin FMA

1 Overview

This document contains information for TPS92682-Q1 (HTSSOP package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1 and Figure 2 show the device functional block diagrams for reference.

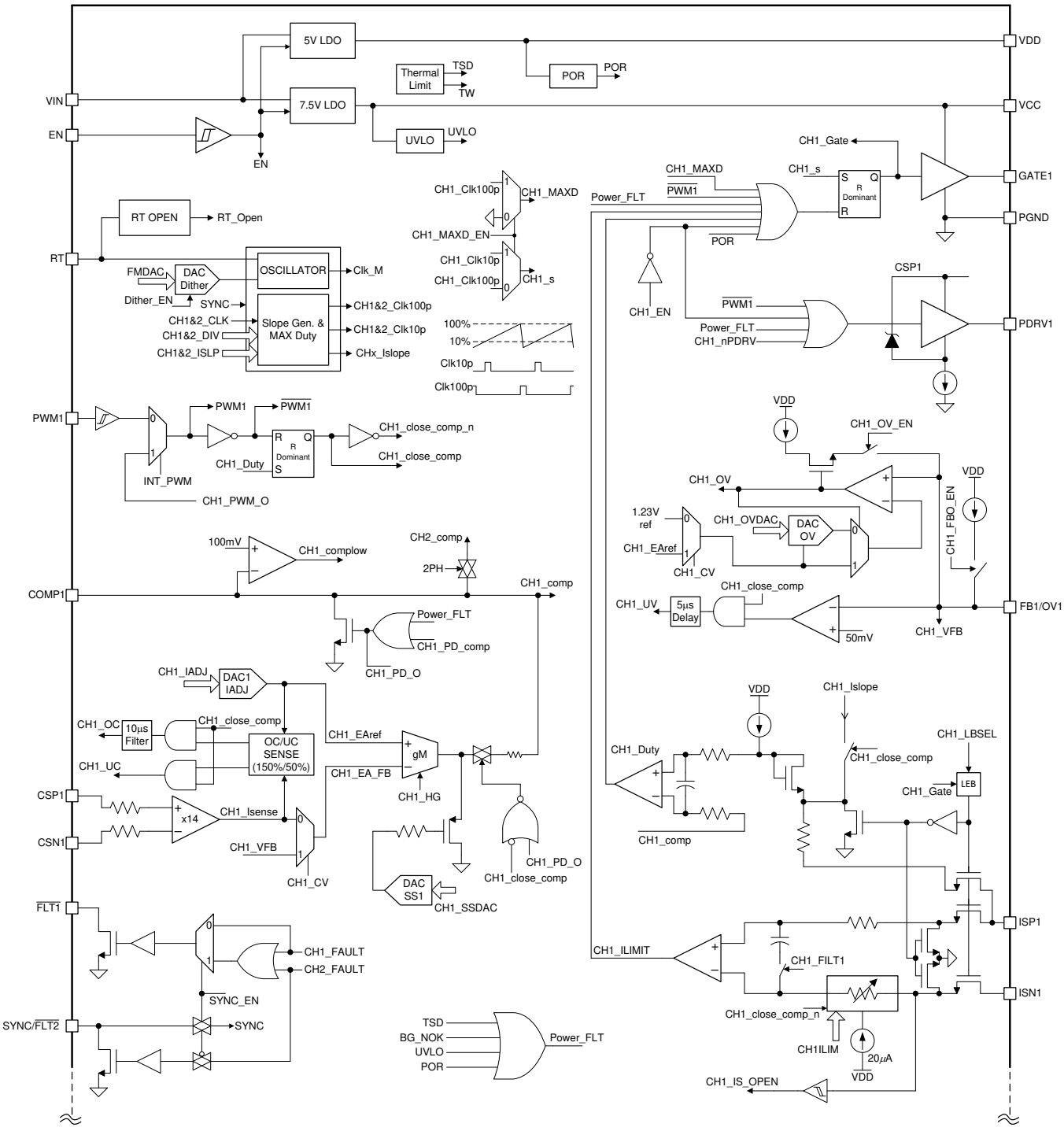

Figure 1. Functional Block Diagram

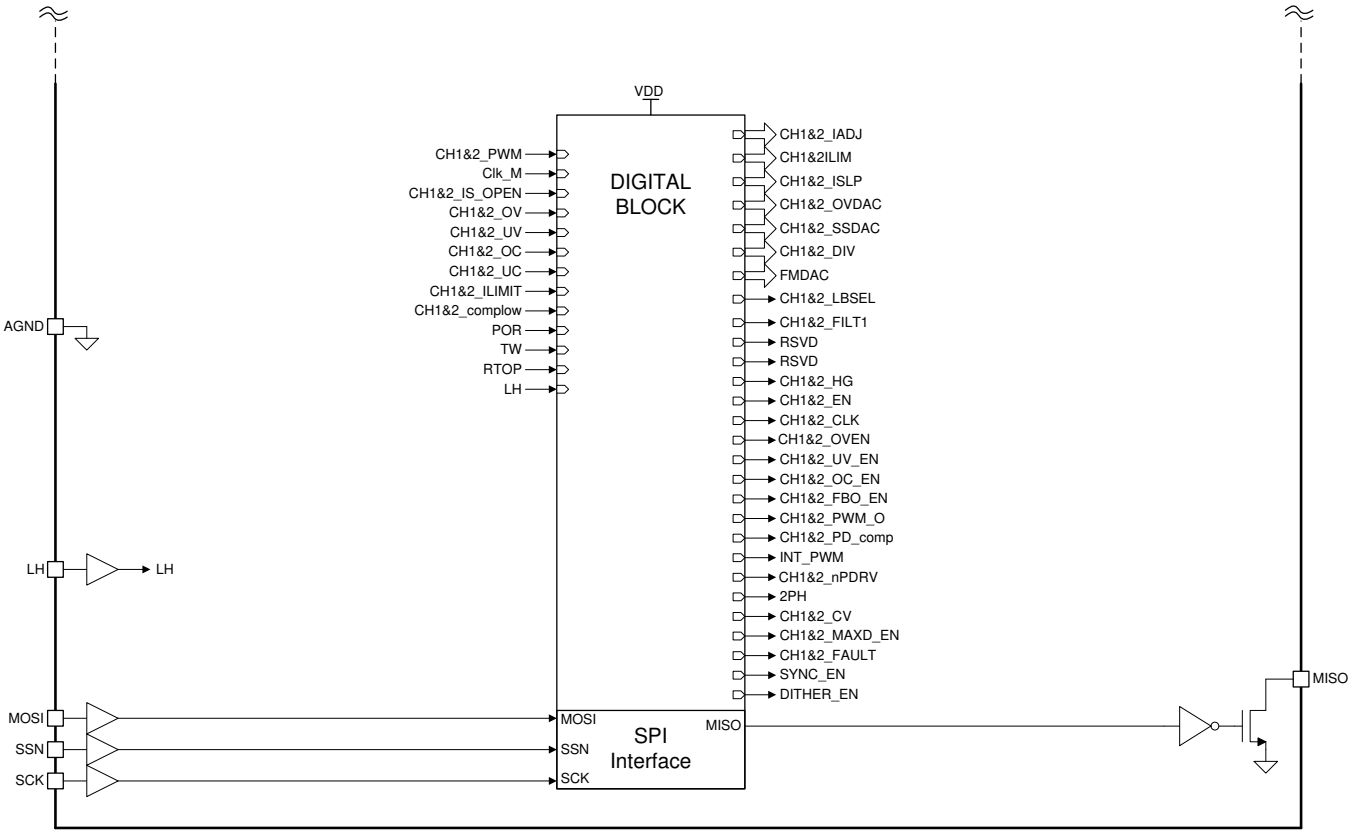

Figure 2. Functional Block Diagram

TPS92682-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for TPS92682-Q1 based on two different industry-wide used reliability standards:

- Table 1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	23
Die FIT Rate	3
Package FIT Rate	20

The failure rate and mission profile information in Table 1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 150 mW
- Climate type: World-wide Table 8
- Package factor lambda 3 Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	60 FIT	70°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPS92682-Q1 in Table 3 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3. Die Failure Modes and Distribution

Die Failure Modes			Failure Mode Distribution (%)
BIAS	Startup Sequence	Device will not be turned on or it is out of spec	4.4%
	TSD	Device operates as it is in thermal shutdown, or the TSD will not be triggered	<0.5%
	TWARN	Device will report thermal warning at lower temperature, or the thermal warning function is disabled	<0.5%
	VDD	Device will not start	3.3%
	VCC	Device will not start	3.7%
	Bandgap	Device will not meet the specs that utilize voltage reference (DACs, OV, UV, Oscillator, SS, UVLO)	1.3%
	UVLO	Device will not start or will not have the UVLO function	<0.5%
	POR	Device will not start or will not have the POR function	<0.5%
	VREF	DAC voltages are out of spec	<0.5%
Oscillator and RAMP generator	Dither DAC	Spread Spectrum will have a wrong frequency modulation	0.7%
	CLOCK	Clock is disabled, or higher or lower clock frequency than programmed	5.9%
	Max Duty and ISLOPE	Max Duty cycle and slope compensation are out of spec	1.2%
SW_ISENSE	Switch current sense circuit	Internal current feedback loop will not function	1.4%
COMP_SHORT_SW	Compensator short switch between CH1 and CH2	The switch may stuck short or open. Two-Phase operation or independent two-channel operation may not work as intended	<0.5%
FAULT_IO	Fault PINs IO	Fault pins will be stuck high or low	1.1%
SPI_IO	SPI interface IO	Communication error	0.5%

Table 3. Die Failure Modes and Distribution (continued)

Die Failure Modes			Failure Mode Distribution (%)
CONTROLLER	PWM PINs IO	PWM dimming is disabled or the channel is disabled	0.6%
	OV and UV functions	The associated channel is disabled. The Over or Under voltage fault does not function as specified	2.6%
	ILED Current Sense Amp	In CC mode the associated channel does not regulate the LED current as expected. The OC and UC fault does not function	15.1%
	Compensator IO and Pull-Down FET	The associated channel is disabled	11.6%
	Error Amplifier	Error Amplifier offset is too high, or IADJ DAC stuck bit. The associated channel does not regulate the output as programmed	3.9%
		CV/CC sense feedback analog MUX failure. The channel ILIM or OV fault is triggered	1.0%
	Soft-start DAC	One step in the soft start DAC ramp will be missed	1.7%
	ILIM Comparator	ILIM fault is always triggered or does not function	1.1%
	PWM Comparator	The channel is disabled or operates at Max Duty Cycle	1.1%
	PFET Gate Driver	In CC mode if external PFET is used, the PWM dimming is disabled or the output is turned off	4.2%
	NFET Gate Driver	The main NFET is fully ON or fully OFF	8.6%
DIGITAL	SPI interface	Communication error	1.9%
	Registers	Device or one of the channels maybe fully disabled	6.2%
	Faults	One of the channels maybe fully disabled or the faults will not be triggered	0.7%
	SYNC	The SYNC function with external clock does not work	0.5%
	FMDAC	Incorrect frequency modulation	<0.5%
	TEST	Device maybe fully disabled	0.7%
ESD	ESD Cells	PIN may short to GND	12.7%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TPS92682-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 5)
- Pin open-circuited (see Table 6)
- Pin short-circuited to an adjacent pin (see Table 7)
- Pin short-circuited to VIN (see Table 8)

Table 5 through Table 8 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4.

Table 4. Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 3 shows the TPS92682-Q1 pin diagram. For a detailed description of the device pins please refer to the '*Pin Configuration and Functions*' section in the TPS92682-Q1 datasheet.

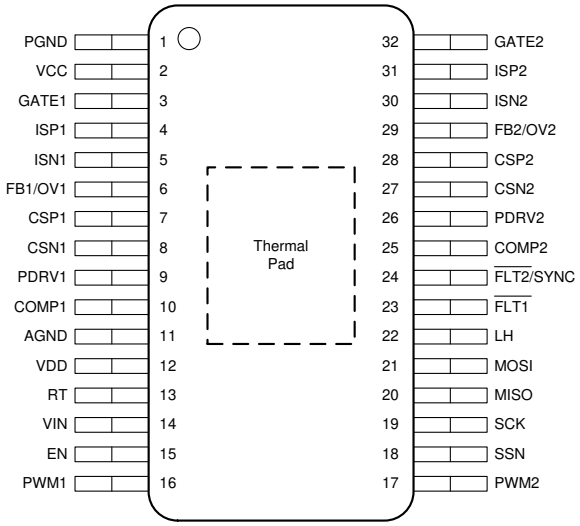

Figure 3. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Channel-1 is configured as coupled inductor CV SEPIC with VOUT = 30 V and POUT = 15 W.
- Channel-2 is configured as coupled inductor CC SEPIC with 6xLED at the output and ILED = 650 mA. External PFET PWM dimming is applied.
- Unless otherwise specified, the voltage applied to the VIN pin is 12 V.

Table 5. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
AGND	11	No effect on the operation of the device	D
COMP1	10	Channel-1 will not start switching	B
COMP2	25	Channel-2 will not start switching	B
CSN1	8	In CV mode, CSN pin is normally connected to GND. This has no effect on the operation of the device	D
CSN2	27	In CC mode, CSN short to GND can damage the device	A
CSP1	7	In CV mode, CSP pin is normally connected to GND. This has no effect on the operation of the device	D
CSP2	28	In CC mode, CSP short to GND will potentially short VIN to GND. This may generate a UVLO and the device will not operate	B
EN	15	Device will be in shutdown mode and will not operate	B
FB1/OV1	6	If UV fault is enabled, CH1UV is triggered and re-starts when MFT expires. If UV fault is not enabled, this condition may damage the external components	B
FB2/OV2	29	If UV fault is enabled, CH2UV is triggered and re-starts when MFT expires. If UV fault is not enabled, this condition may damage the external components	B
$\overline{\text{FLT1}}$	23	The faults on channel-1 cannot be observed on the FLT1 pin.	C
$\overline{\text{FLT2}}$/SYNC	24	The faults on channel-2 cannot be observed on the FLT2 pin. If the part is programed to use SYNC functionality, the part will switch from SYNC clock to the internal clock.	C
GATE1	3	Channel-1 is turned off, VCC may drop below UVLO and the device will not operate	B
GATE2	32	Channel-2 is turned off, VCC may drop below UVLO and the device will not operate	B
ISN1	5	ISN1 is connected to GND by default. This has no effect on the operation of the device	D
ISN2	30	ISN2 is connected to GND by default. This has no effect on the operation of the device	D
ISP1	4	Because of the slope compensation ramp, channel-1 may still operate as in a voltage mode control, but could be unstable.	B
ISP2	31	Because of the slope compensation ramp, channel-2 may still operate as in a voltage mode control, but could be unstable.	B
LH	22	Device cannot enter the Limp-home mode	C
MISO	20	Register read cannot be performed.	C
MOSI	21	Device cannot be turned on.	B
PDRV1	9	In CV mode, PDRV is normally connected to GND. This has no effect on the operation of the device	D
PDRV2	26	In CC mode, channel-2 PFET PWM dimming does not function, device and external PFET could be damaged	A
PWM1	16	If external PWM is used to enable channel-1, this will disable channel-1	B
PWM2	17	If external PWM is used to perform dimming on channel 2, this will disable channel-2	B
PGND	1	This has no effect on the operation of the device	D
RT	13	Device will not function properly	B
SCK	19	Device will not function	B
SSN	18	Device will not function	B
VCC	2	UVLO occurs and the device will not function	B
VDD	12	POR occurs and the device will not function	B
VIN	14	Device will not function	B

Table 6. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
AGND	11	Device may not function	B
COMP1	10	Channel-1 will not operate, or channel-1 maybe unstable and CH1ILIM fault maybe triggered	B
COMP2	25	Channel-2 will not operate, or channel-2 maybe unstable and CH2ILIM, CH2OC faults maybe triggered	B
CSN1	8	In CV mode, this has no effect on the operation of the device	D
CSN2	27	In CC mode, CH2OC or CH2OV may be triggered. Channel-2 will not operate	B
CSP1	7	In CV mode, this has no effect on the operation of the device	D
CSP2	28	In CC mode, CH2OC or CH2OV may be triggered. Channel-2 will not operate	B
EN	15	Device will be in shutdown mode and will not operate	B
FB1/OV1	6	CH1OV fault is triggered	B
FB2/OV2	29	CH2OV fault is triggered	B
$\overline{\text{FLT1}}$	23	The faults on channel-1 cannot be observed on the FLT1 pin	C
$\overline{\text{FLT2}}$/SYNC	24	The faults on channel-2 cannot be observed on the FLT2 pin. If the part is programed to use SYNC functionality, the part will switch from SYNC clock to the internal clock	C
GATE1	3	Channel-1 will not operate	B
GATE2	32	Channel-2 will not operate	B
ISN1	5	CH1ISO is triggered, and channel-1 stops switching	B
ISN2	30	CH2ISO is triggered, and channel-2 stops switching	B
ISP1	4	CH1ILIM is triggered. If the ILIM fault is enabled, channel-1 is either turned off until CH1EN is set via SPI or channel-1 restarts after IFT timer is expired	B
ISP2	31	CH2ILIM is triggered. If the ILIM fault is enabled, channel-2 is either turned off until CH2EN is set via SPI or channel-2 restarts after IFT timer is expired	B
LH	22	Device may enter LH mode, which results the device to operate based on the LH register settings.	B
MISO	20	Register read cannot be performed	C
MOSI	21	Device cannot be turned on	B
PDRV1	9	In CV mode, this has no effect on the operation of the device	D
PDRV2	26	In CC mode, LED load is turned-off and CH2OV fault maybe triggered	B
PWM1	16	If external PWM is used to enable channel-1, this will disable channel-1	B
PWM2	17	If external PWM is used to enable channel-2, this will disable channel-2	B
PGND	1	Device may not function	B
RT	13	Device will not function. RTO fault read bit will be set	B
SCK	19	Device will not function	B
SSN	18	Device will not function	B
VCC	2	The Channels will not be able to regulate the output voltage or current, and different faults maybe triggered	B
VDD	12	Device may not be able to function and channels may not turn on	B
VIN	14	Device will not function	B

Table 7. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
PGND	1	VCC	UVLO is triggered and the device will not operate	B
VCC	2	GATE1	UVLO is triggered and the device will not operate	B
GATE1	3	ISP1	CH1ILIM is triggered and channel-1 stops switching	B
ISP1	4	ISN1	Because of the slope compensation ramp, channel-1 may still operate as in a voltage mode control, but could be unstable	B
ISN1	5	FB1/OV1	If UV fault is enabled, CH1UV is triggered and re-starts when MFT expires. If UV fault is not enabled, this condition may damage the external components	B
FB1/OV1	6	CSP1	In CV mode CSP is normally tied to GND, this will trigger the CH1UV fault (if UV fault is enabled). If UV fault is not enabled, this condition may damage the external components	B
CSP1	7	CSN1	In CV mode, both CSP and CSN are normally connected to GND. This has no effect in the operation of the device	D
CSN1	8	PDRV1	In CV mode, both PDRV and CSN are normally connected to GND. This has no effect in the operation of the device	D
PDRV1	9	COMP1	In CV mode, PDRV is normally connected to GND. This will short COMP1 to GND, and channel-1 will not operate	B
COMP1	10	AGND	Channel-1 will not operate	B
AGND	11	VDD	POR occurs and the device will not function	B
VDD	12	RT	RTO fault is triggered and the device will not function	B
RT	13	VIN	Device will be damaged	A
VIN	14	EN	No effect on the operation of the device, EN is normally tied to VIN	D
EN	15	PWM1	If EN pin is tied to VIN, this will damage the device	A
PWM1	16	PWM2	Corner pin-to-pin short implausible	D
PWM2	17	SSN	Depending on the connection of the PWM2, communication error may occur and the device will not function	B
SSN	18	SCK	Communication error, the device will not function	B
SCK	19	MISO	Communication error, the device will not function	B
MISO	20	MOSI	Communication error, the device will not function	B
MOSI	21	LH	Device will not function	B
LH	22	$\overline{\text{FLT1}}$	If LH is actively pulled low, the faults on channel-1 cannot be observed on the FLT1 pin	C
$\overline{\text{FLT1}}$	23	$\overline{\text{FLT2}}$/SYNC	The faults on channel-1 and channel-2 are ORed together via the two pull-up resistors	C
$\overline{\text{FLT2}}$/SYNC	24	COMP2	Channel-2 will not operate.	B
COMP2	25	PDRV2	In CC mode, this will disrupt the operation of the channel-2	B
PDRV2	26	CSN2	In CC mode, LED load is turned-off and CH2OV fault maybe triggered	B
CSN2	27	CSP2	In CC mode, channel-2 will not operate and CH2ILIM or CH2OV maybe triggered	B
CSP2	28	FB2/OV2	In CC mode, device will be damaged	A
FB2/OV2	29	ISN2	If UV fault is enabled, CH2UV is triggered and re-starts when MFT expires. If UV fault is not enabled, this condition may damage the external components	B
ISN2	30	ISP2	Because of the slope compensation ramp, channel-2 may still operate as in a voltage mode control, but could be unstable	B
ISP2	31	GATE2	CH2ILIM is triggered and channel-2 stops switching	B
GATE2	32	PGND	Corner pin-to-pin short implausible	D

Table 8. Pin FMA for Device Pins Short-Circuited to VIN

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
AGND	11	Device may not function	B
COMP1	10	Device will be damaged	A
COMP2	25	Device will be damaged	A
CSN1	8	In CV mode, CSN is normally connected to GND. Device will not function (VIN short to GND)	B
CSN2	27	In CC mode, channel-2 will not operate	B
CSP1	7	In CV mode, CSP is normally connected to GND. Device will not function (VIN short to GND)	B
CSP2	28	In CC mode, channel-2 will not operate	B
EN	15	No effect on the operation of the device, EN is normally tied to VIN	D
FB1/OV1	6	Device will be damaged	A
FB2/OV2	29	Device will be damaged	A
$\overline{\text{FLT1}}$	23	Device will be damaged	A
$\overline{\text{FLT2}}$/SYNC	24	Device will be damaged	A
GATE1	3	Device will be damaged	A
GATE2	32	Device will be damaged	A
ISN1	5	Device will not function (VIN short to GND)	B
ISN2	30	Device will not function (VIN short to GND)	B
ISP1	4	Device will be damaged	A
ISP2	31	Device will be damaged	A
LH	22	Device will be damaged	A
MISO	20	Device will be damaged	A
MOSI	21	Device will be damaged	A
PDRV1	9	In CV mode, PDRV is normally connected to GND. Device will not function (VIN short to GND)	B
PDRV2	26	In CC mode, this will disrupt the operation of the device and external PFET can be damaged.	A
PWM1	16	If PWM1 pin are not connected to GND, this may damage the device	A
PWM2	17	If PWM2 pin are not connected to GND, this may damage the device	A
PGND	1	Device will not function (VIN short to GND)	B
RT	13	Device will be damaged	A
SCK	19	Device will be damaged	A
SSN	18	Device will be damaged	A
VCC	2	Device will be damaged	A
VDD	12	Device will be damaged	A
VIN	14	No effect on the operation of the device	D

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