Functional Safety Information

UCC27284-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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1 Functional Safety FIT Rate, FMD and Pin FMA

1.1 Overview

This document contains information for UCC27282-Q1 UCC27284-Q1(SOIC and VSON package) to aid in a functional safety system design. Information provided are:

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- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
-
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

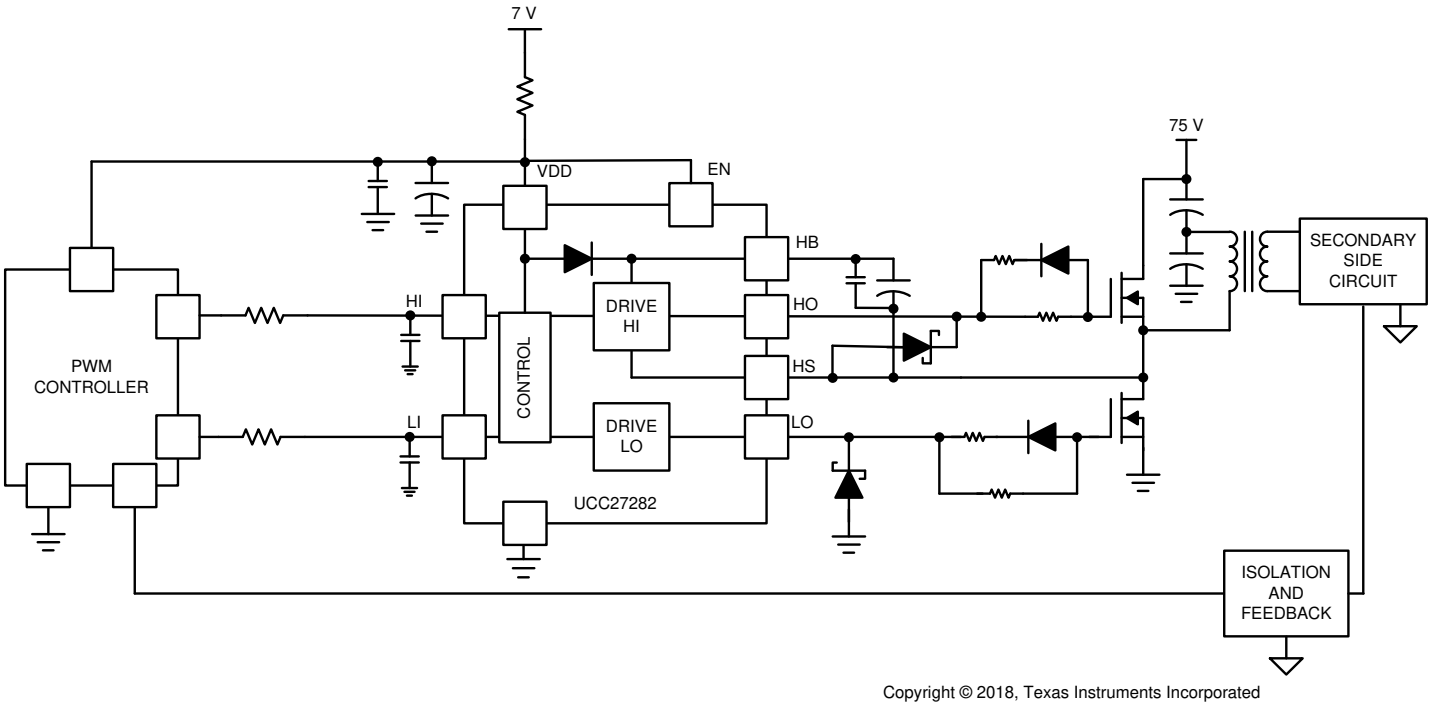

Figure 1-1. UCC27282-Q1 application Block diagram

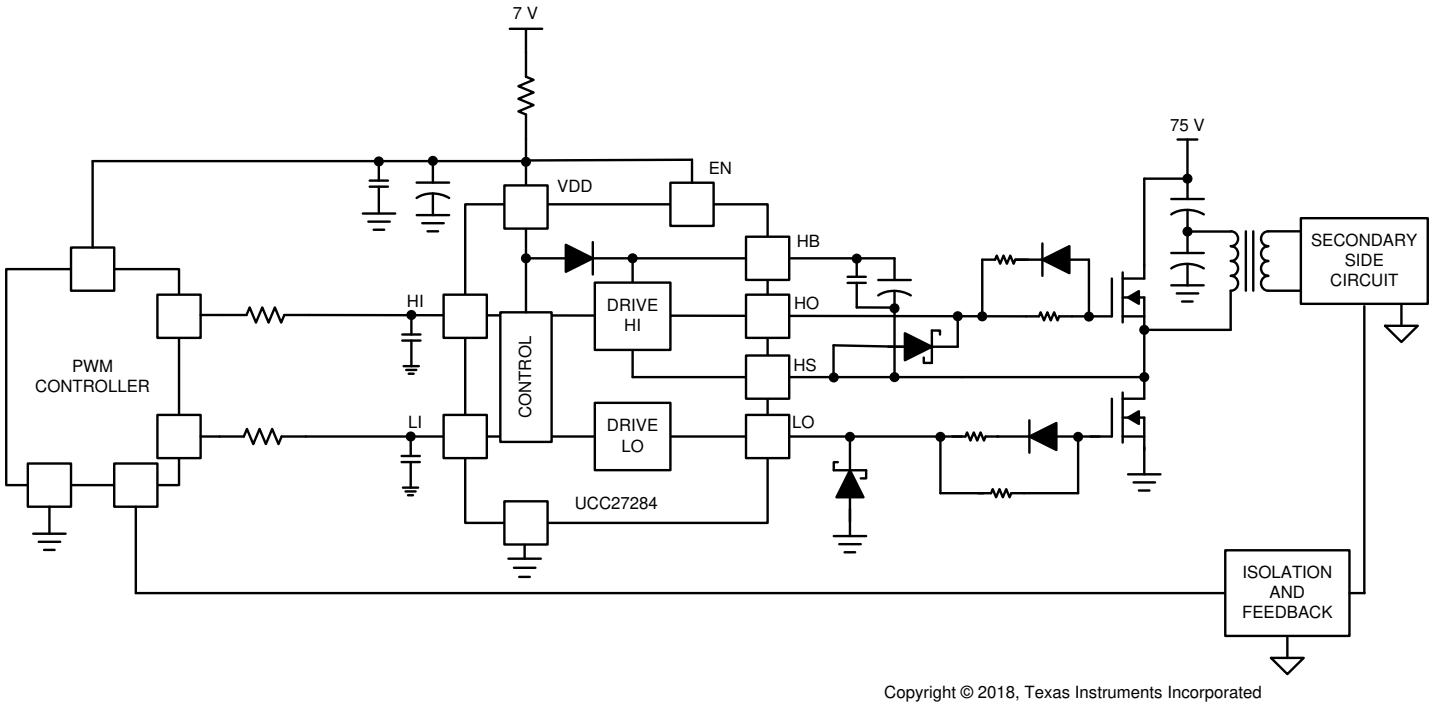

Figure 1-2. UCC27284-Q1 application Block diagram

UCC27282-Q1 UCC27284-Q1 were developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

1.2 Functional Safety Failure In Time (FIT) Rates

1.2.1 SOIC Package

This section provides Functional Safety Failure In Time (FIT) rates for the SOIC package of UCC27282-Q1 UCC27284-Q1 based on two different industry-wide used reliability standards:

- *Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11* provides FIT rates based on IEC TR 62380 / ISO 26262 part 11

Table 1-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate (Power dissipation:10 mW, 100 mW, 500 mW)	13,14,28
Die FIT Rate (Power dissipation: 10 mW, 100 mW, 500 mW)	2,3,14
Package FIT Rate (Power dissipation:10 mW,100mW, 500mW)	11,11,14

The failure rate and mission profile information in *Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11* comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 10 mW, 100 mW, 500 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 1-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS, Digital, analog /mixed	20 FIT	55°C

1.2.1.1 Failure Mode Distribution (FMD)

The failure mode distribution estimation for UCC27282-Q1 UCC27284-Q1 in *Die Failure Modes and Distribution* comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 1-3. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
HO stuck high	16.3%,16.5% (UCC27284-Q1)
HO stuck low	16.3%,16.5% (UCC27284-Q1)
HO voltage out of specified range	16.3%,16.5% (UCC27284-Q1)
LO stuck high	16.3%,16.5%v (UCC27284-Q1)
LO stuck low	16.3%,16.5% (UCC27284-Q1)
LO voltage out of specified range	16.3%,16.5% (UCC27284-Q1)
UVLO not functional (UCC27284-Q1)	1%
UVLO not functional or Interlock not functional (UCC27282-Q1)	1%

1.2.2 VSON Package

This section provides Functional Safety Failure In Time (FIT) rates for the VSON package of UCC27282-Q1 based on two different industry-wide used reliability standards:

- *Component Failure Rates per IEC TR 62380 / ISO 26262 Part 1* provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- *Component Failure Rates per Siemens Norm SN 29500-2* provides FIT rates based on the Siemens Norm SN 29500-2

Table 1-4. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate (Power dissipation:10 mW,100mW, 500mW)	10,12,25
Die FIT Rate (Power dissipation:10 mW,100mW, 500mW)	2,3,14
Package FIT Rate (Power dissipation:10 mW,100mW, 500mW)	8,9,11

The failure rate and mission profile information in *Component Failure Rates per IEC TR 62380 / ISO 26262 Part 1* comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 10 mW,100mW, 500mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 1-5. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS, Digital, analog /mixed	20 FIT	55°C

1.2.2.1 Failure Mode Distribution (FMD)

The failure mode distribution estimation for UCC27282-Q1 in *Die Failure Modes and Distribution* comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 1-6. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
HO stuck high	16.5%
HO stuck low	16.5%
HO voltage out of specified range	16.5%
LO stuck high	16.5%
LO stuck low	16.5%
LO voltage out of specified range	16.5%
UVLO not functional or Interlock not functional	1%

1.3 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the UCC27282-Q1 (SOIC and VSON package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 1-8 and Table 1-12)
- Pin open-circuited (see Table 1-9 and Table 1-13)
- Pin short-circuited to an adjacent pin (see Table 1-10 and Table 1-14)
- Pin short-circuited to supply (see Table 1-11 and Table 1-15)

Table 1-8 through Table 1-15 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 1-7.

Table 1-7. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- SOIC :Pin#1-4, Short to VDD is considered.
- SOIC :Pin#5-6. Short to 5v such as MCU or controller I/O supply is considered.
- SOIC :VSS is assumed to be a ground plane.
- VSON :Pin#1-5 and 10, Short to VDD is considered.
- VSON :Pin#6-8. Short to 5v such as MCU or controller I/O supply is considered.
- VSON :VSS is assumed to be a ground plane.

1.3.1 SOIC Package

Figure 1-3 shows the UCC27282-Q1 UCC27284-Q1pin diagram for the SOIC package. For a detailed description of the device pins please refer to the '*Pin Configuration and Functions*' section in the UCC27282-Q1 UCC27284-Q1 datasheet.

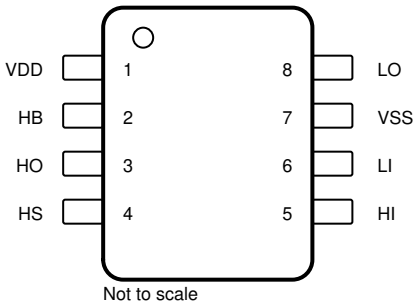

Figure 1-3. Pin Diagram (SOIC Package)

Table 1-8. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VDD	1	LO will remain low. HO will remain low.	B
HB	2	Device may be damaged with unknown LO/HO state	A
HO	3	Device may be damaged with unknown LO/HO state	A
HS	4	Device may be damaged with unknown LO/HO state	A
HI	5	HO will be in a low state	B
LI	6	LO will be a low state	B
VSS	7	N/A	D
LO	8	Device may be damaged with unknown LO/HO state	A

Table 1-9. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VDD	1	LO will remain low. HO will remain low.	B
HB	2	HO will be pulled to HS potential	B
HO	3	HO terminal not connected to the system	D
HS	4	HO will be pulled to HB potential	B
HI	5	HO will be in a low state	B
LI	6	LO will be in a low state	B
VSS	7	HO will be in a low state LO will be pulled to VDD	B
LO	8	LO terminal not connected to the system	D

Table 1-10. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to (PIN#+1)	Description of Potential Failure Effect(s)	Failure Effect Class
VDD	1	HB	Device may be damaged. LO/HO may be damaged with unknown state.	A
HB	2	HO	Device may be damaged with unknown HO state	A
HO	3	HS	Device may be damaged with unknown LO/HO state	A
HS	4	N/A		-
HI	5	LI	HO/LO will be in a low state	B
LI	6	VSS	LO will be a low state	B
VSS	7	LO	Device may be damaged with unknown LO/HO state	A
LO	8	N/A		-

Table 1-11. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VDD	1	No effect	D
HB	2	Device may be damaged with unknown LO/HO state	A
HO	3	Device may be damaged with unknown LO/HO state	A
HS	4	Device may be damaged with unknown LO/HO state	A
HI	5	Short to 5V (Power supply of the Microcontroller) LO/HO will follow the interlock truth table depending on LI/HI	B
LI	6	Short to 5V (Power supply of the Microcontroller) LO/HO will follow the interlock truth table depending on LI/HI	B
VSS	7	HO will be in a low state LO will be pulled to VDD	B
LO	8	Device may be damaged with unknown LO/HO state	A

1.3.2 VSON Package

Figure 1-4 shows the UCC27282-Q1 pin diagram for the VSON package. For a detailed description of the device pins please refer to the '*Pin Configuration and Functions*' section in the UCC27282-Q1 data sheet.

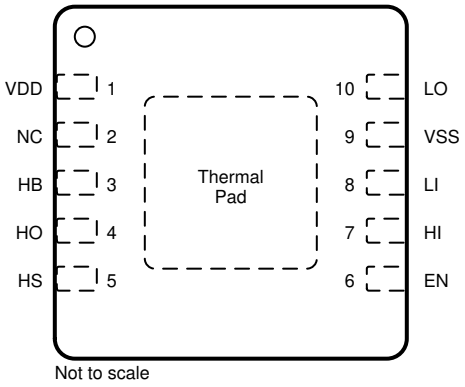

Figure 1-4. Pin Diagram (VSON Package)

Table 1-12. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VDD	1	LO will remain low. HO will remain low.	B
NC	2	No effect	D
HB	3	Device may be damaged with unknown LO/HO state	A
HO	4	Device may be damaged with unknown LO/HO state	A
HS	5	Device may be damaged with unknown LO/HO state	A
EN	6	LO will remain low. HO will remain low.	B
HI	7	HO will be in a low state	B
LI	8	LO will be a low state	B
VSS	9	No effect	D
LO	10	Device may be damaged with unknown LO/HO state	A

Table 1-13. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VDD	1	LO will remain low. HO will remain low.	B
NC	2	No effect	D
HB	3	HO will be pulled to HS potential	B
HO	4	HO terminal not connected to the system	D
HS	5	HO will be pulled to HB potential	B
EN	6	LO will remain low. HO will remain low.	B
HI	7	HO will be in a low state	B
LI	8	LO will be in a low state	B
VSS	9	HO will be in a low state LO will be pulled to VDD	B
LO	10	LO terminal not connected to the system	D

Table 1-14. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to (PIN#+1)	Description of Potential Failure Effect(s)	Failure Effect Class
VDD	1	NC	No effect	D
NC	2	HB	No effect	D
HB	3	HO	Device may be damaged with unknown HO state	A
HO	4	HS	Device may be damaged with unknown LO/HO state	A
HS	5	N/A	-	-
EN	6	HI	LO/HO will follow the logic truth table per datasheet with EN in the same logic state as HI	B
HI	7	LI	HO/LO will be in a low state	B
LI	8	VSS	LO will be a low state	B
VSS	9	LO	Device may be damaged with unknown LO/HO state	A
LO	10	N/A	-	-

Table 1-15. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VDD	1	No effect	D
NC	2	No effect	D
HB	3	Device may be damaged with unknown LO/HO state	A
HO	4	Device may be damaged with unknown LO/HO state	A
HS	5	Device may be damaged with unknown LO/HO state	A
EN	6	Short to 5V (I.E Power supply of the Microcontroller). LO/HO will follow the logic truth table per datasheet with EN stuck in a high state.	B
HI	7	Short to 5V (I.E Power supply of the Microcontroller) LO/HO will follow the interlock truth table depending on LI/HI	B
LI	8	Short to 5V (I.E Power supply of the Microcontroller) LO/HO will follow the interlock truth table depending on LI/HI	B
VSS	9	HO will be in a low state LO will be pulled to VDD	B
LO	10	Device may be damaged with unknown LO/HO state	A

2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (October 2022) to Revision B (November 2022)	Page
• Updated failure mode distribution	4
• Updated failure mode distribution	5

Changes from Revision * (September 2022) to Revision A (October 2022)	Page
• Added Pin Failure Mode Analysis (Pin FMA) data	6

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265