Application Report
SLUAA39A–April 2020–Revised April 2020

TPS92682-Q1 (VQFN) Functional Safety FIT Rate, FMD and Pin FMA

1 Overview

This document contains information for TPS92682-Q1 (VQFN package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1 and Figure 2 show the device functional block diagrams for reference.

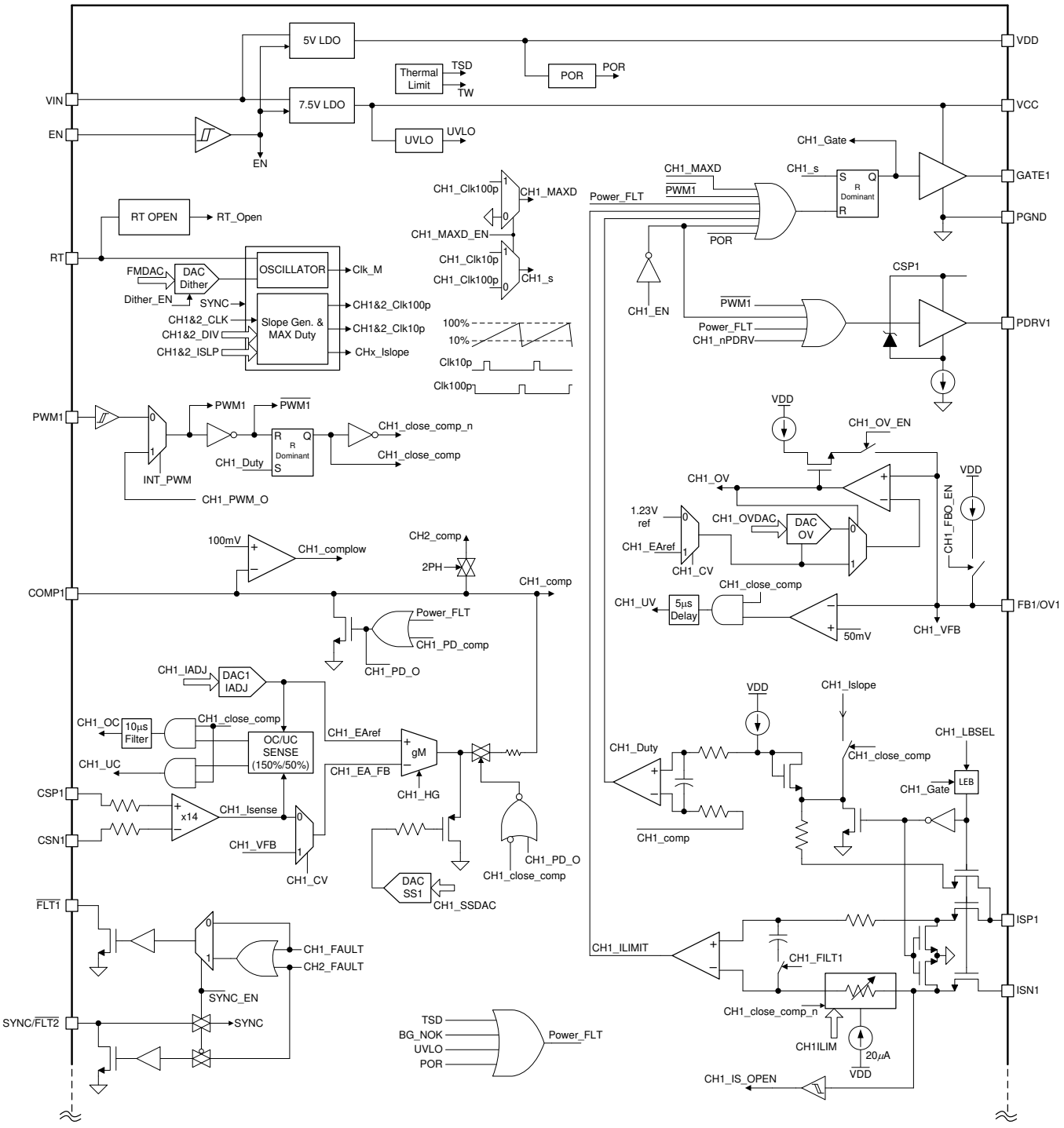

Figure 1. Functional Block Diagram

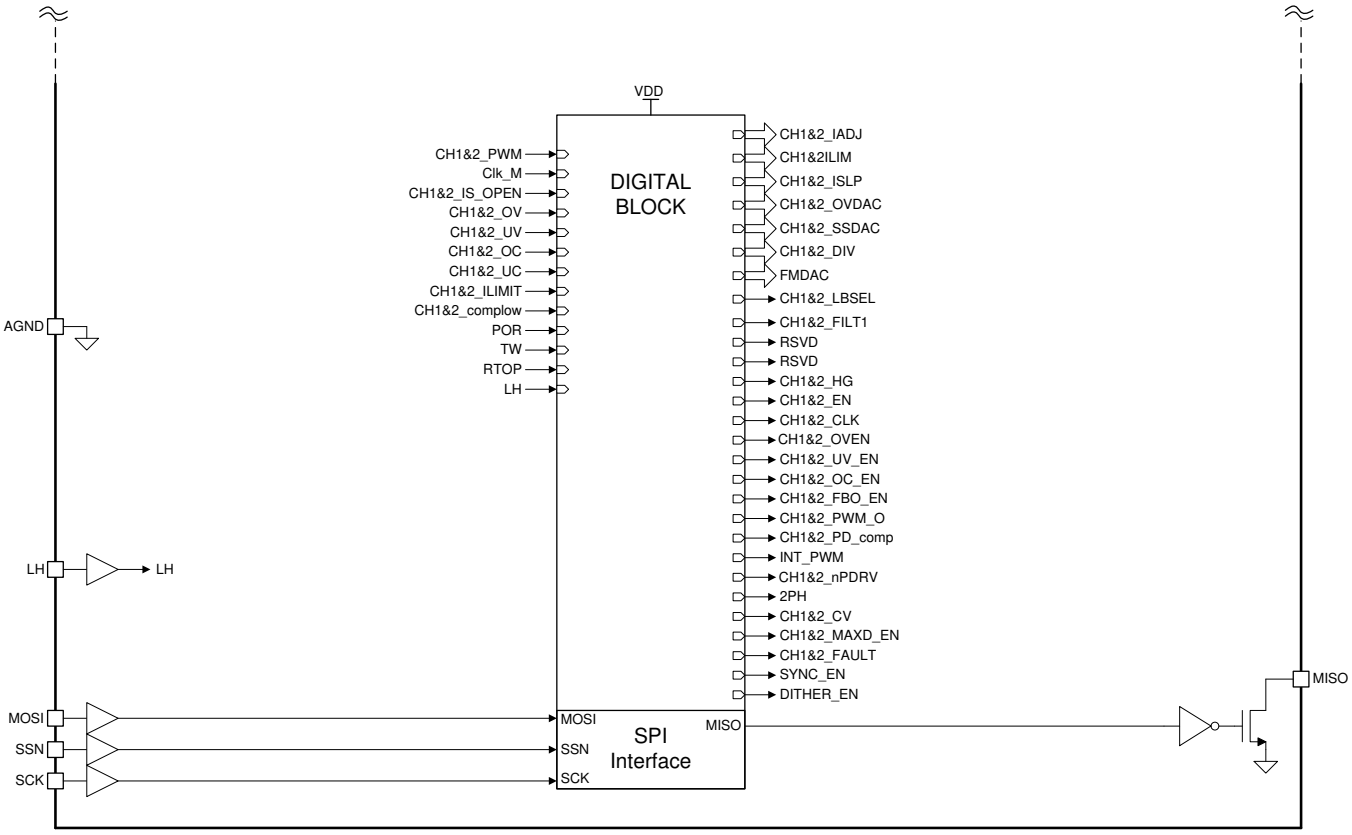

Figure 2. Functional Block Diagram

TPS92682-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for TPS92682-Q1 based on two different industry-wide used reliability standards:

- Table 1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	18
Die FIT Rate	3
Package FIT Rate	15

The failure rate and mission profile information in Table 1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 150 mW
- Climate type: World-wide Table 8
- Package factor lambda 3 Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	60 FIT	70°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPS92682-Q1 in Table 3 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3. Die Failure Modes and Distribution

Die Failure Modes			Failure Mode Distribution (%)
BIAS	Startup Sequence	Device will not be turned on or it is out of spec	4.4%
	TSD	Device operates as it is in thermal shutdown, or the TSD will not be triggered	<0.5%
	TWARN	Device will report thermal warning at lower temperature, or the thermal warning function is disabled	<0.5%
	VDD	Device will not start	3.3%
	VCC	Device will not start	3.7%
	Bandgap	Device will not meet the specs that utilize voltage reference (DACs, OV, UV, Oscillator, SS, UVLO)	1.3%
	UVLO	Device will not start or will not have the UVLO function	<0.5%
	POR	Device will not start or will not have the POR function	<0.5%
	VREF	DAC voltages are out of spec	<0.5%
Oscillator and RAMP generator	Dither DAC	Spread Spectrum will have a wrong frequency modulation	0.7%
	CLOCK	Clock is disabled, or higher or lower clock frequency than programmed	5.9%
	Max Duty and ISLOPE	Max Duty cycle and slope compensation are out of spec	1.2%
SW_ISENSE	Switch current sense circuit	Internal current feedback loop will not function	1.4%
COMP_SHORT_SW	Compensator short switch between CH1 and CH2	The switch may stuck short or open. Two-Phase operation or independent two-channel operation may not work as intended	<0.5%
FAULT_IO	Fault PINs IO	Fault pins will be stuck high or low	1.1%
SPI_IO	SPI interface IO	Communication error	0.5%

Table 3. Die Failure Modes and Distribution (continued)

Die Failure Modes			Failure Mode Distribution (%)
CONTROLLER	PWM PINs IO	PWM dimming is disabled or the channel is disabled	0.6%
	OV and UV functions	The associated channel is disabled. The Over or Under voltage fault does not function as specified	2.6%
	ILED Current Sense Amp	In CC mode the associated channel does not regulate the LED current as expected. The OC and UC fault does not function	15.1%
	Compensator IO and Pull-Down FET	The associated channel is disabled	11.6%
	Error Amplifier	Error Amplifier offset is too high, or IADJ DAC stuck bit. The associated channel does not regulate the output as programmed	3.9%
		CV/CC sense feedback analog MUX failure. The channel ILIM or OV fault is triggered	1.0%
	Soft-start DAC	One step in the soft start DAC ramp will be missed	1.7%
	ILIM Comparator	ILIM fault is always triggered or does not function	1.1%
	PWM Comparator	The channel is disabled or operates at Max Duty Cycle	1.1%
	PFET Gate Driver	In CC mode if external PFET is used, the PWM dimming is disabled or the output is turned off	4.2%
	NFET Gate Driver	The main NFET is fully ON or fully OFF	8.6%
DIGITAL	SPI interface	Communication error	1.9%
	Registers	Device or one of the channels maybe fully disabled	6.2%
	Faults	One of the channels maybe fully disabled or the faults will not be triggered	0.7%
	SYNC	The SYNC function with external clock does not work	0.5%
	FMDAC	Incorrect frequency modulation	<0.5%
	TEST	Device maybe fully disabled	0.7%
ESD	ESD Cells	PIN may short to GND	12.7%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TPS92682-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 5 for CV BOOST and Table 6 for CC BOOST configuration)
- Pin open-circuited (see Table 7 for CV BOOST and Table 8 for CC BOOST configuration)
- Pin short-circuited to an adjacent pin (see Table 9 for CV BOOST and Table 10 for CC BOOST configuration)

Table 5 through Table 10 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4.

Table 4. Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 3 shows the TPS92682-Q1 pin diagram. For a detailed description of the device pins please refer to the '*Pin Configuration and Functions*' section in the TPS92682-Q1 datasheet.

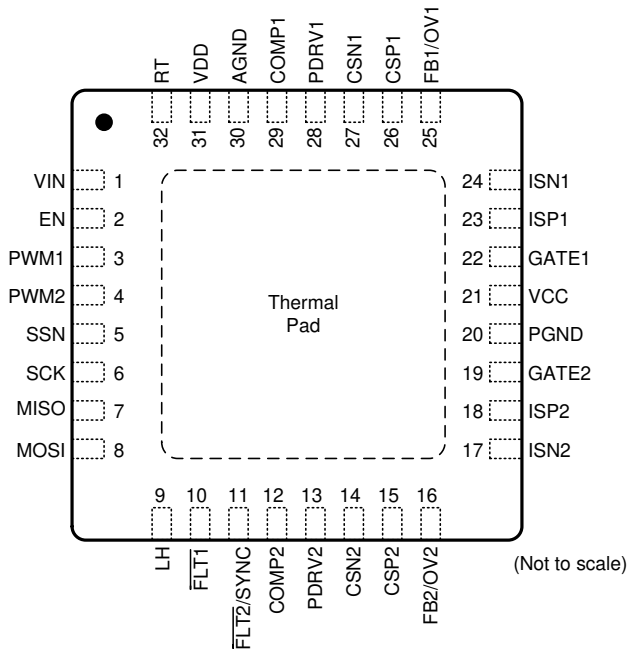

Figure 3. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- In CC mode, BOOST configuration is used with 12xLED at the output. External PFET PWM dimming is applied.
- In CV mode, BOOST configuration is used with VOUT = 50 V.
- Unless otherwise specified, the voltage applied to the VIN pin is 12 V.

Table 5. Pin FMA for Device Pins Short-Circuited to Ground in CV BOOST

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
AGND	30	No effect on the operation of the device	D
COMP1	29	Channel-1 will not start switching	B
COMP2	12	Channel-2 will not start switching	B
CSN1	27	In CV mode, CSN1 pin is connected to GND. This has no effect on the operation of the device	D
CSN2	14	In CV mode, CSN2 pin is connected to GND. This has no effect on the operation of the device	D
CSP1	26	In CV mode, CSP1 pin is connected to GND. This has no effect on the operation of the device	D
CSP2	15	In CV mode, CSP2 pin is connected to GND. This has no effect on the operation of the device	D
EN	2	Device will be in shutdown mode and will not operate	B
FB1/OV1	25	If UV fault is enabled, CH1UV is triggered and re-starts when MFT expires. If UV fault is not enabled, this condition may damage the external components	B
FB2/OV2	16	If UV fault is enabled, CH2UV is triggered and re-starts when MFT expires. If UV fault is not enabled, this condition may damage the external components	B
$\overline{\text{FLT1}}$	10	The faults on channel-1 cannot be observed on the FLT1 pin.	C
$\overline{\text{FLT2}}$/SYNC	11	The faults on channel-2 cannot be observed on the FLT2 pin. If the part is programed to use SYNC functionality, the part will switch from SYNC clock to the internal clock.	C
GATE1	22	Channel-1 is turned off, VCC may drop below UVLO and the device will not operate	B
GATE2	19	Channel-2 is turned off, VCC may drop below UVLO and the device will not operate	B
ISN1	24	ISN1 is connected to GND by default. This has no effect on the operation of the device	D
ISN2	17	ISN2 is connected to GND by default. This has no effect on the operation of the device	D
ISP1	23	Because of the slope compensation ramp, channel-1 may still operate as in a voltage mode control, but could be unstable.	B
ISP2	18	Because of the slope compensation ramp, channel-2 may still operate as in a voltage mode control, but could be unstable.	B
LH	9	Device cannot enter the Limp-home mode	C
MISO	7	Register read cannot be performed.	C
MOSI	8	Device cannot be turned on.	B
PDRV1	28	In CV mode, PDRV1 is normally connected to GND. This has no effect on the operation of the device	D
PDRV2	13	In CV mode, PDRV2 is normally connected to GND. This has no effect on the operation of the device	D
PWM1	3	If external PWM is used to enable channel-1, this will disable channel-1	B
PWM2	4	If external PWM is used to enable channel-2, this will disable channel-2	B
PGND	20	This has no effect on the operation of the device	D
RT	32	Device will not function properly	B
SCK	6	Device will not function	B
SSN	5	Device will not function	B
VCC	21	UVLO occurs and the device will not function	B
VDD	31	POR occurs and the device will not function	B
VIN	1	Device will not function	B

Table 6. Pin FMA for Device Pins Short-Circuited to Ground in CC BOOST

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
AGND	30	No effect on the operation of the device	D
COMP1	29	Channel-1 will not start switching	B
COMP2	12	Channel-2 will not start switching	B
CSN1	27	Device can be damaged	A
CSN2	14	Device can be damaged	A
CSP1	26	CSP1 short to GND will potentially short VIN to GND. This may generate a UVLO and the device will not operate	B
CSP2	15	CSP2 short to GND will potentially short VIN to GND. This may generate a UVLO and the device will not operate	B
EN	2	The device will be in shutdown mode and will not operate	B
FB1/OV1	25	If UV fault is enabled, CH1UV is triggered and re-starts when MFT expires. If UV fault is not enabled, this condition may damage the external components	B
FB2/OV2	16	If UV fault is enabled, CH2UV is triggered and re-starts when MFT expires. If UV fault is not enabled, this condition may damage the external components	B
$\overline{\text{FLT1}}$	10	The faults on channel-1 cannot be observed on the FLT1 pin.	C
$\overline{\text{FLT2}}$/SYNC	11	The faults on channel-2 cannot be observed on the FLT2 pin. If the part is programed to use SYNC functionality, the part will switch from SYNC clock to the internal clock.	C
GATE1	22	Channel-1 is turned off, VCC may drop below UVLO and the device will not operate	B
GATE2	19	Channel-2 is turned off, VCC may drop below UVLO and the device will not operate	B
ISN1	24	ISN1 is connected to GND by default. This has no effect on the operation of the device	D
ISN2	17	ISN2 is connected to GND by default. This has no effect on the operation of the device	D
ISP1	23	Because of the slope compensation ramp, channel-1 may still operate as in a voltage mode control, but could be unstable.	B
ISP2	18	Because of the slope compensation ramp, channel-2 may still operate as in a voltage mode control, but could be unstable.	B
LH	9	Device cannot enter the Limp-home mode	C
MISO	7	Register read cannot be performed	C
MOSI	8	Device cannot be turned on	B
PDRV1	28	Channel-1 PFET PWM dimming does not function, device and external PFET could be damaged	A
PDRV2	13	Channel-2 PFET PWM dimming does not function, device and external PFET could be damaged	A
PWM1	3	If external PWM is used to perform dimming on channel 1, this will disable channel-1	B
PWM2	4	If external PWM is used to perform dimming on channel 2, this will disable channel-2	B
PGND	20	This has no effect on the operation of the device	D
RT	32	Device will not function properly	B
SCK	6	Device will not function	B
SSN	5	Device will not function	B
VCC	21	UVLO occurs and the device will not function	B
VDD	31	POR occurs and the device will not function	B
VIN	1	Device will not function	B

Table 7. Pin FMA for Device Pins Open-Circuited in CV BOOST

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
AGND	30	Device may not function	B
COMP1	29	Channel-1 will not operate, or channel-1 maybe unstable	B
COMP2	12	Channel-2 will not operate, or channel-2 maybe unstable	B
CSN1	27	In CV mode, this has no effect on the operation of the device	D
CSN2	14	In CV mode, this has no effect on the operation of the device	D
CSP1	26	In CV mode, this has no effect on the operation of the device	D
CSP2	15	In CV mode, this has no effect on the operation of the device	D
EN	2	Device will be in shutdown mode and will not operate	B
FB1/OV1	25	CH1OV fault is triggered	B
FB2/OV2	16	CH2OV fault is triggered	B
$\overline{\text{FLT1}}$	10	The faults on channel-1 cannot be observed on the FLT1 pin	C
$\overline{\text{FLT2}}$/SYNC	11	The faults on channel-2 cannot be observed on the FLT2 pin. If the part is programed to use SYNC functionality, the part will switch from SYNC clock to the internal clock	C
GATE1	22	Channel-1 will not operate	B
GATE2	19	Channel-2 will not operate	B
ISN1	24	CH1ISO is triggered, and channel-1 stops switching	B
ISN2	17	CH2ISO is triggered, and channel-2 stops switching	B
ISP1	23	CH1ILIM is triggered. If the ILIM fault is enabled, channel-1 is either turned off until CH1EN is set via SPI or channel-1 restarts after IFT timer is expired	B
ISP2	18	CH2ILIM is triggered. If the ILIM fault is enabled, channel-2 is either turned off until CH2EN is set via SPI or channel-2 restarts after IFT timer is expired	B
LH	9	Device may enter LH mode, which results the device to operate based on the LH register settings.	B
MISO	7	Register read cannot be performed	C
MOSI	8	Device cannot be turned on	B
PDRV1	28	This has no effect on the operation of the device	D
PDRV2	13	This has no effect on the operation of the device	D
PWM1	3	If external PWM is used to enable channel-1, this will disable channel-1	B
PWM2	4	If external PWM is used to enable channel-2, this will disable channel-2	B
PGND	20	Device may not function	B
RT	32	Device will not function. RTO fault read bit will be set	B
SCK	6	Device will not function	B
SSN	5	Device will not function	B
VCC	21	The Channels will not be able to regulate the output voltage, and different faults maybe triggered	B
VDD	31	Device may not be able to function and channels may not turn on	B
VIN	1	Device will not function	B

Table 8. Pin FMA for Device Pins Open-Circuited in CC BOOST

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
AGND	30	Device may not function	B
COMP1	29	Channel-1 will not operate, or channel-1 maybe unstable and CH1ILIM, CH1OC faults maybe triggered	B
COMP2	12	Channel-2 will not operate, or channel-2 maybe unstable and CH2ILIM, CH2OC faults maybe triggered	B
CSN1	27	CH1OC or CH1OV may be triggered. Channel-1 will not operate	B
CSN2	14	CH2OC or CH2OV may be triggered. Channel-2 will not operate	B
CSP1	26	CH1OC or CH1OV may be triggered. Channel-1 will not operate	B
CSP2	15	CH2OC or CH2OV may be triggered. Channel-2 will not operate	B
EN	2	Device will be in shutdown mode and will not operate	B
FB1/OV1	25	CH1OV fault is triggered	B
FB2/OV2	16	CH2OV fault is triggered	B
$\overline{\text{FLT1}}$	10	The faults on channel-1 cannot be observed on the FLT1 pin	C
$\overline{\text{FLT2}}$/SYNC	11	The faults on channel-2 cannot be observed on the FLT2 pin. If the part is programed to use SYNC functionality, the part will switch from SYNC clock to the internal clock	C
GATE1	22	Channel-1 will not operate	B
GATE2	19	Channel-2 will not operate	B
ISN1	24	CH1ISO is triggered, and channel-1 stops switching	B
ISN2	17	CH2ISO is triggered, and channel-2 stops switching	B
ISP1	23	CH1ILIM is triggered. If the ILIM fault is enabled, channel-1 is either turned off until CH1EN is set via SPI or channel-1 restarts after IFT timer is expired	B
ISP2	18	CH2ILIM is triggered. If the ILIM fault is enabled, channel-2 is either turned off until CH2EN is set via SPI or channel-2 restarts after IFT timer is expired	B
LH	9	Device may enter LH mode, which results the device to operate based on the LH register settings.	B
MISO	7	Register read cannot be performed	C
MOSI	8	Device cannot be turned on	B
PDRV1	28	LED load is turned-off and CH1OV fault maybe triggered	B
PDRV2	13	LED load is turned-off and CH2OV fault maybe triggered	B
PWM1	3	If external PWM is used to enable channel-1, this will disable channel-1	B
PWM2	4	If external PWM is used to enable channel-2, this will disable channel-2	B
PGND	20	Device may not function	B
RT	32	Device will not function. RTO fault read bit will be set	B
SCK	6	Device will not function	B
SSN	5	Device will not function	B
VCC	21	The Channels will not be able to regulate the output voltage, and different faults maybe triggered	B
VDD	31	Device may not be able to function and channels may not turn on	B
VIN	1	Device will not function	B

Table 9. Pin FMA for Device Pins Short-Circuited to Adjacent Pin in CV BOOST

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
VIN	1	EN	No effect on the operation of the device, EN is normally tied to VIN	D
EN	2	PWM1	If EN pin is tied to VIN, this may cause damage to the device	A
PWM1	3	PWM2	In CV mode, PWM1 and PWM2 are normally both tied to VDD	D
PWM2	4	SSN	Depending on the connection of the PWM, communication error may occur and the device will not function	B
SSN	5	SCK	Communication error, the device will not function	B
SCK	6	MISO	Communication error, the device will not function	B
MISO	7	MOSI	Communication error, the device will not function	B
MOSI	8	LH	Corner pin-to-pin short implausible	D
LH	9	$\overline{\text{FLT1}}$	If LH is actively pulled low, the faults on channel-1 cannot be observed on the FLT1 pin	C
$\overline{\text{FLT1}}$	10	$\overline{\text{FLT2}}$/SYNC	The faults on channel-1 and channel-2 are ORed together via the two pull-up resistors	C
$\overline{\text{FLT2}}$/SYNC	11	COMP2	If external clock via SYNC is used, this will disturb the operation of the device	B
COMP2	12	PDRV2	In CV mode, PDRV2 is normally connected to GND. In that case, channel-2 will not operate	B
PDRV2	13	CSN2	In CV mode, PDRV2, CSP2 and CSN2 are normally connected to GND. This has no effect in the operation of the device	D
CSN2	14	CSP2	In CV mode, PDRV2, CSP2 and CSN2 are normally connected to GND. This has no effect in the operation of the device	D
CSP2	15	FB2/OV2	In CV mode CSP2 is normally tied to GND, this will trigger the UV fault on channel-2 (if UV fault is enabled)	B
FB2/OV2	16	ISN2	Corner pin-to-pin short implausible	D
ISN2	17	ISP2	Because of the slope compensation ramp, channel-2 may still operate as in a voltage mode control, but could be unstable	B
ISP2	18	GATE2	CH2ILIM is triggered and channel-2 stops switching	B
GATE2	19	PGND	Channel-2 is turned off, VCC may drop below UVLO and the device will not operate	B
PGND	20	VCC	UVLO is triggered and the device will not operate	B
VCC	21	GATE1	UVLO is triggered and the device will not operate	B
GATE1	22	ISP1	CH1ILIM is triggered and channel-1 stops switching	B
ISP1	23	ISN1	Because of the slope compensation ramp, channel-1 may still operate as in a voltage mode control, but could be unstable	B
ISN1	24	FB1/OV1	Corner pin-to-pin short implausible	D
FB1/OV1	25	CSP1	In CV mode CSP1 is normally tied to GND, this will trigger the UV fault on channel-1 (if UV fault is enabled)	B
CSP1	26	CSN1	In CV mode, PDRV1, CSP1 and CSN1 are normally connected to GND. This has no effect in the operation of the device	D
CSN1	27	PDRV1	In CV mode, PDRV1, CSP1 and CSN1 are normally connected to GND. This has no effect in the operation of the device	D
PDRV1	28	COMP1	In CV mode, PDRV1 is normally connected to GND. In that case, channel-1 will not operate	B
COMP1	29	AGND	Channel-1 will not operate	B
AGND	30	VDD	POR occurs and the device will not function	B
VDD	31	RT	RTO fault is triggered and the device will not function	B
RT	32	VIN	Corner pin-to-pin short implausible	D

Table 10. Pin FMA for Device Pins Short-Circuited to Adjacent Pin in CC BOOST

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
VIN	1	EN	No effect on the operation of the device, EN is normally tied to VIN	D
EN	2	PWM1	If EN pin is tied to VIN, this may cause damage to the device	A
PWM1	3	PWM2	If internal PWM is used, this has no effect on the operation of device	D
PWM2	4	SSN	Depending on the connection of the PWM, communication error may occur and the device will not function	B
SSN	5	SCK	Communication error, the device will not function	B
SCK	6	MISO	Communication error, the device will not function	B
MISO	7	MOSI	Communication error, the device will not function	B
MOSI	8	LH	Corner pin-to-pin short implausible	D
LH	9	$\overline{\text{FLT1}}$	If LH is actively pulled low, the faults on channel-1 cannot be observed on the FLT1 pin	C
$\overline{\text{FLT1}}$	10	$\overline{\text{FLT2}}$/SYNC	The faults on channel-1 and channel-2 are ORed together via the two pull-up resistors	C
$\overline{\text{FLT2}}$/SYNC	11	COMP2	If external clock via SYNC is used, this will disturb the operation of the device	B
COMP2	12	PDRV2	This will disrupt the operation of the channel-2	B
PDRV2	13	CSN2	LED load is turned-off and CH2OV fault maybe triggered	B
CSN2	14	CSP2	Channel-2 will not operate and CH2ILIM or CH2OV maybe triggered	B
CSP2	15	FB2/OV2	Device will be damaged	A
FB2/OV2	16	ISN2	Corner pin-to-pin short implausible	D
ISN2	17	ISP2	Because of the slope compensation ramp, channel-2 may still operate as in a voltage mode control, but could be unstable	B
ISP2	18	GATE2	CH2ILIM is triggered and channel-2 stops switching	B
GATE2	19	PGND	Channel-2 is turned off, VCC may drop below UVLO and the device will not operate	B
PGND	20	VCC	UVLO is triggered and the device will not operate	B
VCC	21	GATE1	UVLO is triggered and the device will not operate	B
GATE1	22	ISP1	CH1ILIM is triggered and channel-1 stops switching	B
ISP1	23	ISN1	Because of the slope compensation ramp, channel-1 may still operate as in a voltage mode control, but could be unstable	B
ISN1	24	FB1/OV1	Corner pin-to-pin short implausible	D
FB1/OV1	25	CSP1	Device will be damaged	A
CSP1	26	CSN1	Channel-1 will not operate and CH1ILIM or CH1OV maybe triggered	B
CSN1	27	PDRV1	LED load is turned-off and CH1OV fault maybe triggered	B
PDRV1	28	COMP1	This will disrupt the operation of the channel-1	B
COMP1	29	AGND	Channel-1 will not operate	B
AGND	30	VDD	POR occurs and the device will not function	B
VDD	31	RT	RTO fault is triggered and the device will not function	B
RT	32	VIN	Corner pin-to-pin short implausible	D

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (April 2020) to A Revision	Page
• Changed multiple instances of channel-1 to channel-2	1

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