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Selection Considerations for Output Capacitors of Multiphase Voltage Regulators Part 1

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ABSTRACT

This application note describes the selection considerations of output capacitors, based on load transient and output impedance of processors power rails. Presently, there are no specific tools available for non-Intel processor output capacitors selection in multiphase designs. In Part 1, the minimum required output capacitance to meet low repetitive rate load transient specifications is discussed. Part 2 will describe capacitor types and value to meet output impendence requirements, and also high rate repetitive load transient specifications. Analytical and experimental results show that output capacitors selection is optimized for load transient and output impedance, to fulfill non-Intel processor requirements.

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D-CAP+ is a trademark of Texas Instruments.

1 Introduction

High-performance microprocessors require low voltage and high current voltage regulator modules(VRM). The large supply current not only poses a stringent challenge on efficiency, but also heavily burdens the transient response. To ensure fast load transient, output capacitors and output impedance should be optimized.

In multiphase voltage regulators based on interleaved buck topology, the inductor selection of L is decided by current ripple, reflecting trade-off between inductor volume and power losses. Then, the output capacitance C_o is based on both steady-state ripple and load transient specification(undershoot v_{ud} and overshoot v_{ov}). In most of the cases, not steady-state ripple but load transient of output voltage is the major limiting factor for output capacitance selection.

For a buck converter, some equations were provided to calculate output capacitance based on load transient, but they are under perfectly ideal cases, without taking specific load step characteristics, loop response influence, controller limitations and multiphase features into consideration. Actually, shown in Figure 2, load step characteristics like slew rate k, amplitude A, and repetitive rate (or called frequency) will highly decide how the controller responses to the load transient.

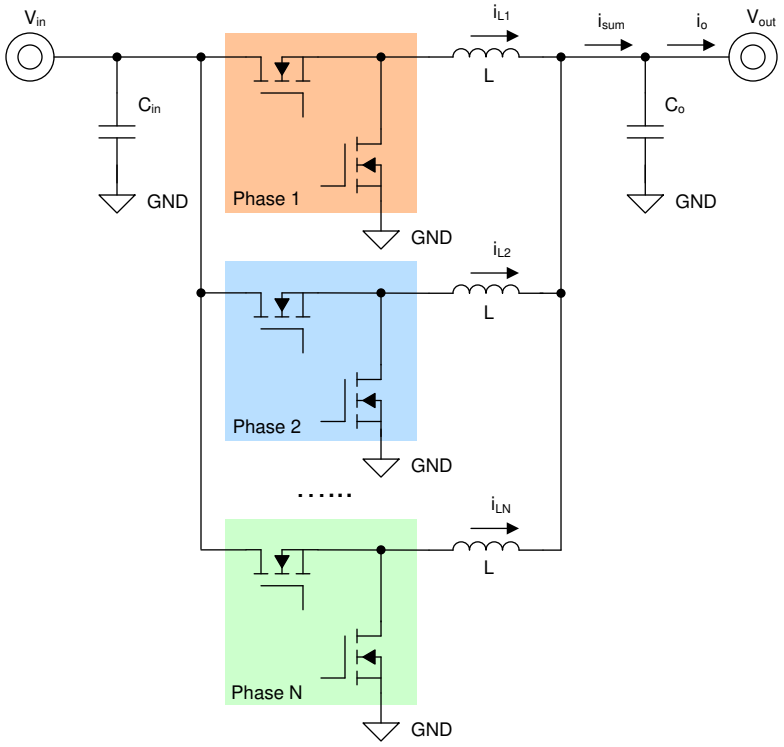

Figure 1. Multiphase Voltage Regulator Diagram

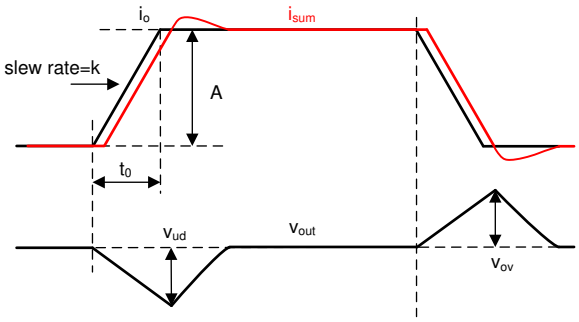

Figure 2. Undershoot and Overshoot of Load Transient

When closed loop adjusts automatically, it may go into saturation as equivalent duty cycle goes to zero or maximum, with load disturbance.

Whether saturated or not, the control loop will have a key impact on load transient performance. With analysis of frequency domain bode plot, as well as system type and bandwidth, load transient with unsaturated loop can be completely described by a linear system transfer function. While the control loop is saturated, load transient should be taken over by physics, including controller limitations, and parameters like inductance and capacitance.

To clearly research on how TI controller with D-CAP+™ control would respond in non-Intel application, analysis will be done by assuming DC load-line(DCLL)=0, and dynamic phase shedding(DPS) and non-linear features(like OSR) disabled. USR feature is automatically inactive when DPS is disabled.

2 Current Transfer Function $G_{ii\_CL}(s)$ of Load Current to Inductor Current

From Figure 1, the summation of all inductor current is called I_{sum}, undershoot and overshoot occur when I_{sum} cannot track I_o quickly. To calculate undershoot and overshoot without DCLL, based on unbalanced electric discharges and charges of output capacitors, the relationship of I_{sum} and I_o needs to be clarified. Thus, it's important to know how inductor current I_L(I_{sum} in multiphase application) responds when load current I_o varies rapidly.

Based on small-signal model of a multiphase buck converter, and the D-CAP+ control modeling, we can derive small-signal transfer functions both in open loop and closed loop, of any input to any output within the system, shown in Figure 3.

All open-loop small-signal transfer functions based on D-CAP+ control mode are listed below:

Table 1. Open-loop Small-signal Transfer Functions in D-CAP+ Control Mode

Transfer Functions	Explanations
$G_{ii\_OP}(s)$	From input I_o to output I_L/I_{sum}
$Z_{o\_OP}(s)$	From input I_o to output v_{out}
$G_{vi\_OP}(s)$	From input v_{in} to output I_L/I_{sum}
$G_{vv\_OP}(s)$	From input v_{in} to output v_{out}
$G_{c2iL}(s)$	From input v_c to output I_L/I_{sum}
$G_{c2vo}(s)$	From input v_c to output v_{out}
$H_{comp}(s)$	Loop compensation

For example, from input I_o to output v_{out}, the transfer function is named $Z_{o\_OP}(s)$, representing how I_o variation affects v_{out} in open loop, also called open-loop output impendence from physical meaning.

Inside the dot line at bottom below, is the common closed-loop control loop called loop gain $L(s)=H_{comp}(s)*G_{c2vo}(s)$. All closed-loop transfer functions can be calculated based on open-loop transfer functions and loop gain together, with signal-flow diagram transformation in Figure 3.

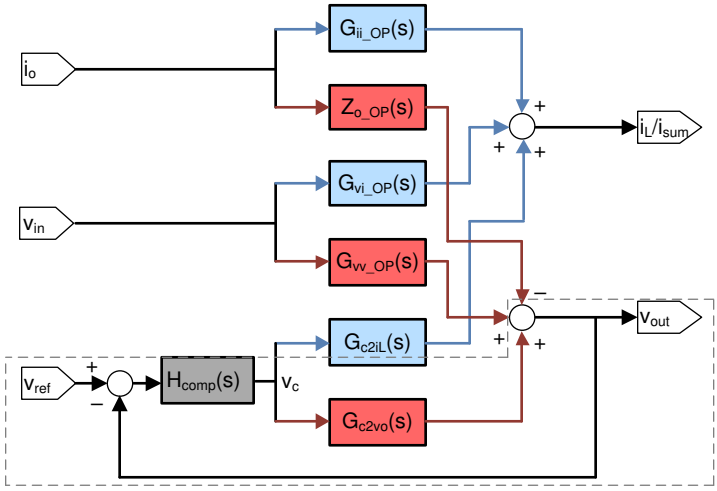

Figure 3. Signal-Flow Diagram of Small-Signal Model of D-CAP+ Control

Load current I_o to inductor current I_L (I_{sum} in multiphase application), as current transfer functions, are our interests here. For clarity, we define symbols as below:

- $G_{ii\_OP}(s)$ is open-loop transfer function of I_o to I_{sum}
- $G_{ii\_CL}(s)$ is closed-loop transfer function of I_o to I_{sum}

They describe how I_o will affect I_{sum} with specific expression, under open-loop and D-CAP+ closed-loop control in frequency domain.

Taking parameters in Table 5 as an example, the bode plot of loop gin L(s) is shown in Figure 4 with results of both simulation and bench test. We can find these two match well with cross frequency f_c=~100kHz.

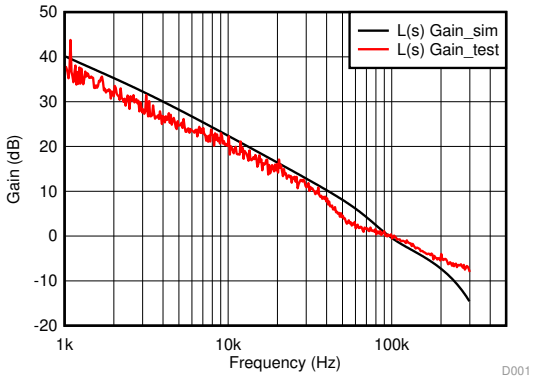

Figure 4. Bode Plot of Loop Gain L(s) in Simulation and Bench Test

The good matching result can direct us to extend the usage of simulation tool to estimate other transfer functions. By performing signal-flow diagram transformation in Figure 3, we get the closed-loop equation of $G_{ii\_CL}(s)$:

$$G_{ii\_CL}(s) = G_{ii\_OP}(s) - \frac{Z_{o\_OP}(s)H_{comp}(s)G_{c2iL}(s)}{1 + H_{comp}(s)G_{c2vo}(s)} = G_{ii\_OP}(s) - \frac{Z_{o\_OP}(s)H_{comp}(s)G_{c2iL}(s)}{1 + L(s)} \quad (1)$$

In Figure 5, simulation shows what $G_{ii\_CL}(s)$ looks like, when compared with $G_{ii\_OP}(s)$ and L(s) together.

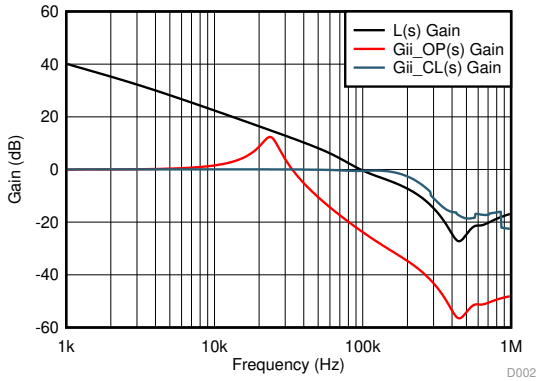

Figure 5. Bode Plot of $G_{ii\_CL}(s)$, $G_{ii\_OP}(s)$ and L(s) in Simulation

In conclusion, by D-CAP+ closed-loop control, we can strongly increase the bandwidth of the $G_{ii\_OP}(s)$ to much higher, and improve dynamic response of I_{sum}, ensuring itself to follow I_o load step as quick as possible. From Figure 5, we can approximately take $G_{ii\_CL}(s)$ as a first-order system with corner frequency $f_{ci}=1.5f_c=\sim150kHz$.

Figure 6 is one simulated example showing that real response of I_{sum}, matches very well with emulated response of the approximate first-order system, under a given ramp-step input.

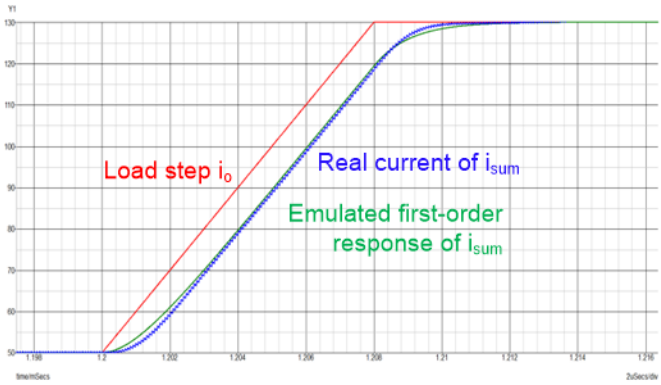

Figure 6. Response of Approximate First-Order System

We will use the response of this approximate $G_{ii\_CL}(s)$ to emulate real response of I_{sum}, under a given ramp-step load step, in a linear system without saturation.

3 Output Capacitance Calculation Based on Load Transient

3.1 Steady-state Output Ripple

Steady-state output voltage ripple is a function of capacitance, capacitor equivalent series resistance (ESR), and inductor ripple current. In multiphase applications, effective inductor current ripple is used to calculate V_{out} ripple, not per phase current ripple.

For single phase application, inductor current ripple:

$$i_{L\_rp} = \frac{V_{out}(1-D)}{f_{SW}L} \quad (2)$$

Where D is steady – state duty cycle,

f_{sw} is switching frequency

In multiphase application, in most of the cases, voltage drop ratio is high and not particular many phases are used for interleaving, as there are no overlaps between any two PWM waveforms of each phase, the effective ripple of I_{sum}:

$$i_{sum\_rp} = \frac{V_{out}\left(1 - (N \times D)\right)}{f_{SW}L}$$

Where N is phase number (3)

If effective ESR and ESL are neglected, the output voltage ripple is as follow:

$$v_{o\_rp} = \frac{V_{out}\left(1 - (N \times D)\right)}{8C_o f_{sw}{}^2 L} \quad (4)$$

But in most of the cases, the output capacitance should be decided by load transient specification.

3.2 Load Step Transient Response

Each time of load transient can be described with one output current trapezoid wave. Only low repetitive rate load transient will be discussed here, which means we can assume each upward and downward pulse of trapezoid wave will have a long time gap. Each pulse of load transient has enough time to wait for v_{out} transition to a new steady state.

Taking undershoot as example, I_o ramps up fast with a certain slew rate k, while I_{sum} will follow as fast as possible, but the difference always happens and comes with electric discharges of output capacitors, causing v_{out} to drop. Overshoot is completely similar with this undershoot situation.

Depending on load step slew rate k and amplitude A, low repetitive load transient can be divided into two cases below.

Table 2. Two Cases of Load Transient

Case Number	Loop Status	Triggering Conditions
Case 1	Unsaturated loop(small-signal linear operation)	Light load step, with small slew rate k and small amplitude A
Case 2	Partially or fully saturated loop(large-signal non-linear operation)	Heavy load step, with large slew rate k and large amplitude A

These two cases will cause different corresponding behaviors of the control loop and the controller.

3.2.1 Case 1: Small-signal Transient with Unsaturated Loop

In **Case 1**, we assume that control loop never goes into saturation during transition period, the response of I_{sum} will strictly follow the law of $G_{ii\_CL}(s)$ linear system, and also the form of the input signal. Using $f_{ci}=1.5f_c$ as corner frequency, $G_{ii\_CL}(s)$ can be estimated as a first-order system:

$$G_{ii\_CL}(s) \approx \frac{1}{1+\tau s} = \frac{1}{1+\frac{1}{\omega_{ci}}s} = \frac{1}{1+\frac{1}{2\pi f_{ci}}s} = \frac{1}{1+\frac{1}{3\pi f_c}s}$$

Where τ is time constant for this first−order system (5)

Figure 7 shows current waveforms of given input ramp-step signal I_o and output response I_{sum}, by taking unsaturated undershoot as example.

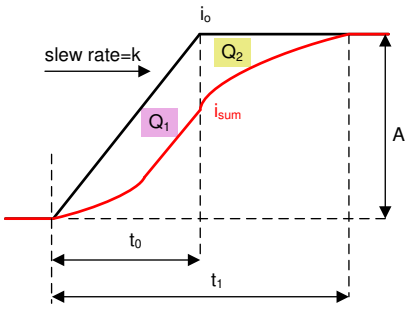

Figure 7. Current Waveforms of I_o and I_{sum} in Case 1

Load step current can be expressed below:

$$i_o(t) = \begin{cases} k \times t & 0 < t < t_0 \\ k \times t_0 & t_0 < t < t_1 \end{cases} \quad (6)$$

By using Laplace and inv-Laplace transformation, we can get equations of I_{sum}:

$$i_{sum}(t) = \begin{cases} \frac{k}{\omega_{ci}}\left(\omega_{ci} t + e^{-\omega_{ci} t} - 1\right) & 0 < t < t_0 \\ \frac{k}{\omega_{ci}}\left(\omega_{ci} t_0 + e^{-\omega_{ci} t} - e^{\omega_{ci}(t_0 - t)}\right) & t_0 < t < t_1 \end{cases} \quad (7)$$

The total discharges of capacitors can be expressed by:

$$Q = Q_1 + Q_2 = \int_0^{t0} \left(i_o - i_{sum}\right) dt + \int_{t0}^{t1} \left(i_o - i_{sum}\right) dt = \frac{kt_0}{\omega_{ci}} = \frac{kt_0}{3\pi f_c} \quad (8)$$

Thus, the undershoot(overshoot is the same) should be:

$$V_{ud} = V_{ov} = \frac{Q}{C_o} = \frac{kt_0}{3\pi f_c C_o} = \frac{A}{3\pi f_c C_o} \quad (9)$$

From formulas above, when the loop is unsaturated, for given output capacitance and loop bandwidth, undershoot(also overshoot) is decided by the bandwidth of loop gain, and the amplitude of load transient.

Experimental results of 150A load step can also prove that, the slew rate k of load step will hardly affect the undershoot value. Only if the slew rate k is very low, less than 0.01V difference can be found in this case. When k goes up to higher, almost no difference can be observed.

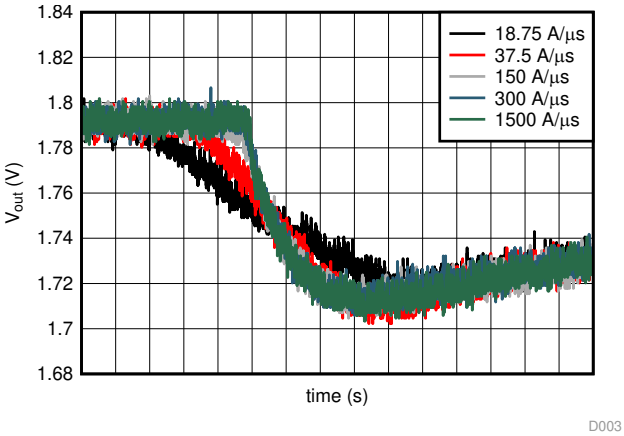

Figure 8. 150A Load Transient with Different Slew Rate k in Case 1

Please note, loop bandwidth is related to output capacitance. When calculating, we are supposed to consider that they are coupled.

3.2.2 Case 2: Large-signal Transient with Saturated Loop

In **Case 2** (Figure 9), we assume that the control loop will go into partial or full saturation during transition period, the response of I_{sum} will be limited by the controller itself and circuit parameters. During a heavy transient, the voltage loop saturates and demands pulses as fast as possible, which means only blanking time will be between each rising edge of PWM pulse. This feature is helpful to high repetitive transient response, for example in short duration of load transient, all phases turn-on would generate too much energy and cause big overshoot. "Over-compensation" can be avoided by adding blanking time.

Blanking time prevents double pulsing of PWM, but at the same time limits the maximum capability of I_{sum} rising. Based on this feature, minimum per-phase switching period T_{sat} is limited to $N*t_{blank}$.

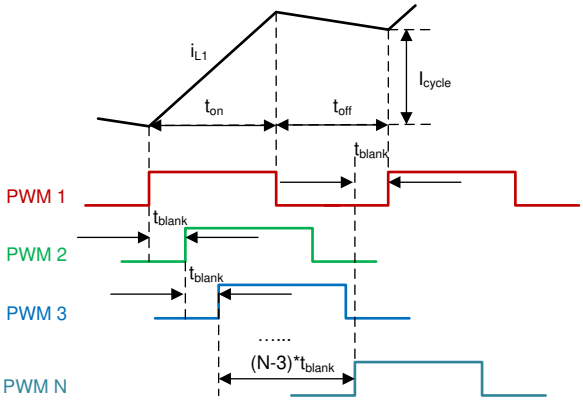

Figure 9. Phase 1 Current I_{L1} in Case 2

Looking into current I_{L1} of phase 1 for example, shown in Figure 9. The effective switching cycle T_{sat} under saturation, and on/off time are calculated below:

$$T_{sat} = N \times t_{blank} \tag{10}$$

$$t_{on} = \frac{V_{out}}{V_{in} f_{sw}} \tag{11}$$

$$t_{off} = N \times t_{blank} - t_{on} \tag{12}$$

The effective current rising I_{cycle} in each phase, during one cycle is:

$$I_{cycle} = t_{on} \frac{V_{in} - V_{out}}{L} - t_{off} \frac{V_{out}}{L} \tag{13}$$

I_{sum} is rising with efforts of all phase current, during full loop saturation, representing the maximum ability of I_{sum} rising, this slew rate is:

$$k_{max\_up} = N \frac{I_{cycle}}{T_{sat}} = \frac{I_{cycle}}{t_{blank}} \tag{14}$$

Loop delay time will become critical for undershoot and overshoot when loop is saturated. It means how much time needed for I_{sum} to respond to rising or falling I_o. This delay time is defined as t_{d_ud} and t_{d_ov} here, and affected by loop dynamic response, but typically 3 to 5 extra pulses if loop compensation is designed appropriately. Assume n_{ex} is number of extra pulses, we use $t_{d\_ud}/t_{d\_ov}=n_{ex}*t_{on}$ to estimate roughly.

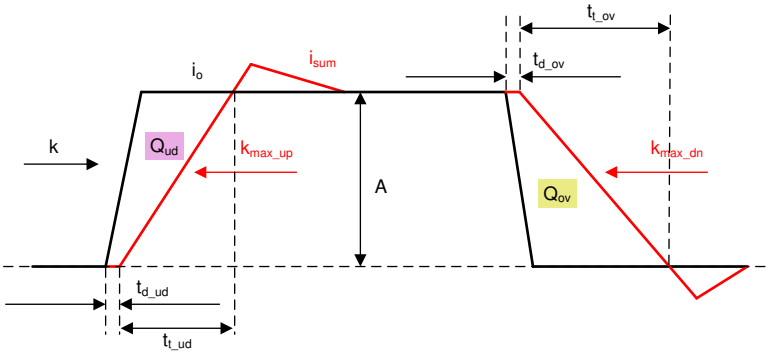

Figure 10. Undershoot and Overshoot Calculation in Case 2

Figure 10 shows waveforms of how current difference contributes to undershoot and overshoot. With knowing I_{cycle} each cycle when current is rising, we can easily know how many cycles and also time duration, to make I_{sum} and I_o equal.

$$n_{pulse} = \frac{A}{NI_{cycle}} \tag{15}$$

$$t_{t\_ud} = n_{pulse} \times Nt_{blank} \tag{16}$$

The discharges and undershoot are as follows:

$$Q_{ud} = \frac{1}{2}\left(2t_{d\_ud} + t_{t\_ud} - \frac{A}{k}\right)A \tag{17}$$

$$v_{ud} = \frac{Q_{ud}}{C_o} \tag{18}$$

When I_{sum} is falling during full loop saturation, there is no pulse until steady state. Similarly, we have the following equations:

$$k_{max\_dn} = \frac{nV_{out}}{L} \tag{19}$$

$$t_{t\_ov} = \frac{A}{k_{max\_dn}} \tag{20}$$

$$Q_{ov} = \frac{1}{2}\left(2t_{d\_ov} + t_{t\_ov} - \frac{A}{k}\right)A \tag{21}$$

$$v_{ov} = \frac{Q_{ov}}{C_o} \tag{22}$$

From formulas above, reducing inductance can surly lower undershoot/overshoot under saturated loop, but at the expense of efficiency with more current ripple. Also, when the loop is fully saturated, the output capacitance required will be affected by almost all the variations of load step characteristics, loop delay time, controller settings, and component parameters.

3.2.3 Criteria for Loop Saturation

Judgement for loop saturation depends on the relationship of desired slew rate of I_{sum} rising/falling and maximum supported slew rate for I_{sum} rising/falling, under the assumption of unsaturated loop (linear system response).

The maximum desired slew rate of I_{sum} named k_{de_max}, is decided by the nature response of $G_{ii\_CL}(s)$ emulated first-order system, while the maximum supported slew rate for I_{sum} named k_{max}, is decided by controller limitations and circuit parameters together. Upward and downward load step have different k_{max} value.

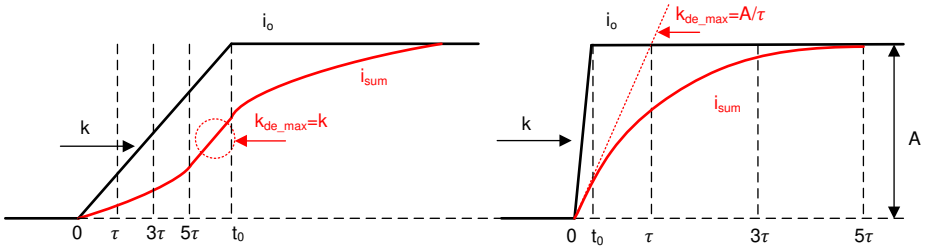

Figure 11. Nature Response of $G_{ii\_CL}(s)$ Linear System

Below tables are used to simply but roughly judge, what status the response should be like, under linear system assumption.

Table 3. Criteria for Slew Rate Relationship

	Condition 1	Condition 2	Condition 3
t_0	t_0<<τ	Somewhere in between	t_0>3~5τ
Response waveform in Figure 11	Right	Somewhere in between	Left
Desired max slew rate: k_{de_max}	A/τ	Somewhere in between	k

Table 4. Criteria for Loop Saturation

Slew Rate Comparison	Loop Status
k_{max}>k_{de_max}	Unsaturated
k_{max}<k_{de_max}	Partially or fully saturated

4 Analytical Calculations and Experimental Verification

See Table 5 for bench test conditions.

Table 5. Bench Test Conditions

Parameters	Value
Input voltage: V_{in}	12V
Output voltage: V_{out}	1.8V
Load resistor(as processor leakage): R_{load}	0.1Ohm
Phase number: N	7
Inductance: L	120nH
Switching frequency: f_{sw}	800kHz
Effective output capacitance: C_o	2550μF
Measured cross frequency of loop gain: f_c	100kHz
Estimated cross frequency of $G_{ii\_CL}(s)$: f_{ci}	150kHz
Selected blanking time: t_{blank}	60ns

In Figure 12, both undershoot and overshoot are unsaturated.

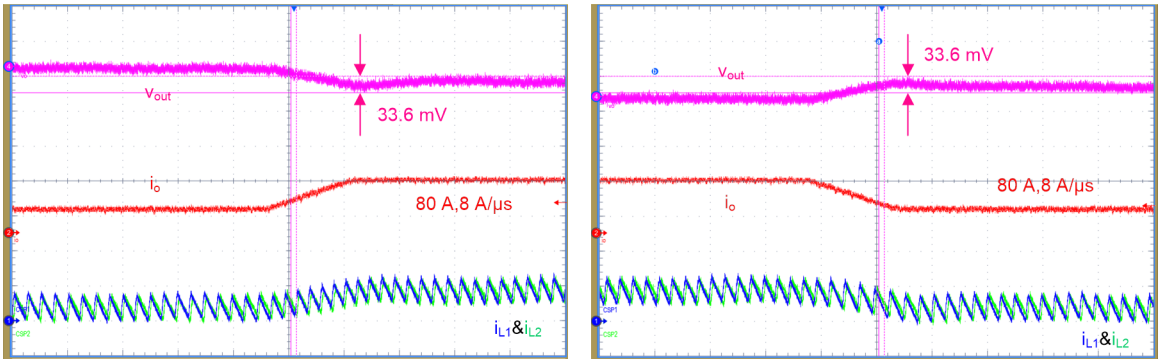

Figure 12. Load Transient Waveforms of Example 1

In this situation, load transient is "light" to both upward and downward load step, the response of emulated first-order linear system caused by load step, can be followed very well by real current, unsaturated undershoot and overshoot are symmetrical.

In Figure 13, undershoot is unsaturated while overshoot is saturated.

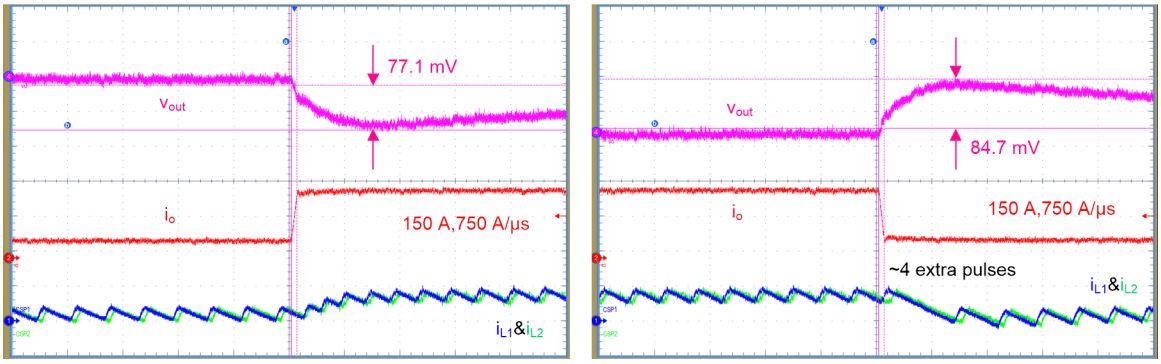

Figure 13. Load Transient Waveforms of Example 2

In this situation, load transient is still "light" to upward load step, but "heavy" to downward load step, linear system response can be followed upwards, but cannot be followed downwards due to physical limitation, causing overshoot higher than undershoot.

In Figure 14, both undershoot and overshoot are saturated.

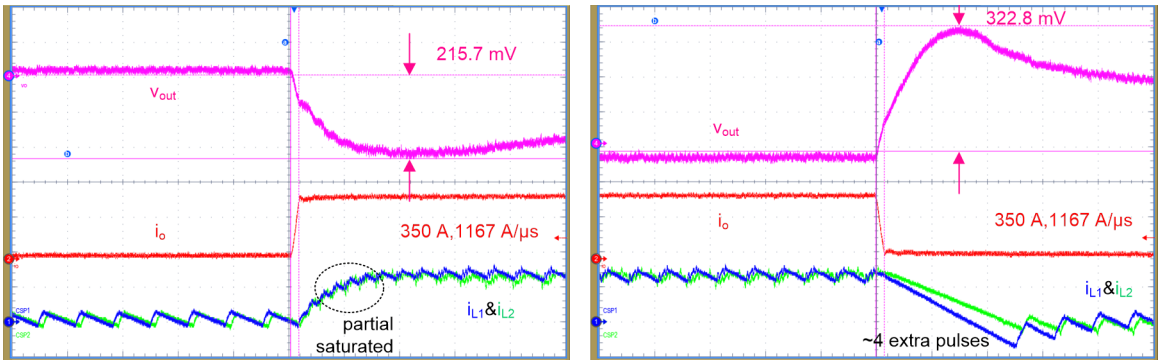

Figure 14. Load Transient Waveforms of Example 3

In this situation, load transient is "heavy" to both upward and downward load step, linear system response cannot be followed due to physical limitation, causing both undershoot and overshoot higher. Besides, pay attention to the upward load step in example 3, this is only partial saturated as k_{max} is relatively high. I_{sum} cannot follow linear system response at the very beginning, but can follow second half of load step. However if you look at downward, it can never follow the linear response caused by falling output current.

By using all of the equations listed in Section 3.2, we can easily get the calculated undershoot and overshoot voltage. Review Table 6 for all results below of calculations and bench test, analytical and experimental results are able to match without much difference.

Table 6. Calculations and Bench Test

Example Number	Calculated Undershoot(mV)	Bench Undershoot(mV)	Calculated Overshoot(mV)	Bench Overshoot(mV)
1	33.3	33.6	33.3	33.6
2	62.4	77.1	80.3	84.7
3	198.1	215.7	311.1	322.8

5 Conclusions

In Part 1, we conclude that loop saturation is so crucial when calculating load transient response. For a fixed design, it is the nature output response of linear system $G_{ii\_CL}(s)$, but not load step itself, will determine loop saturation. In D-CAP+ multiphase solution, maximum slew rate of I_{sum} is limited by voltage, inductance, phase number, switching frequency and blanking time(upwards).

If I_{sum} maximum slew rate can follow the linear system $G_{ii\_CL}(s)$ output nature response, loop saturation never comes. Loop bandwidth becomes the most critical factor coming into picture; If not, loop saturation occurs with more undershoot and overshoot expected. Then everything physical comes into picture except load transient slew rate, others like phase number, blanking time and switching frequency(t_{on} related) will make impacts.

Part 2 will describe capacitors selection (including types and value) to meet the requirements of output impendence and high rate repetitive load transient.

6 References

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