Application Report
SLUA996–December 2019

BQ21061 Two-Layer Small Form Factor Reference Design For Cost-Optimized PCBs

Anthony Pham

ABSTRACT

Wafer Chip Scale Package (WCSP) integrated circuits are a great option for saving printed-circuit board (PCB) area a circuit takes, but integrated circuits (ICs) with smaller pitch and multiple rows of pads push the PCB to make use of via-in-pad technology, thereby increasing board cost. While this might be normal for wearable and hearing aid type applications, there are other applications, such as charging cases for total wireless stereo technology and industrial scanners, that can get by without via-in-pad layout and leverage from a small form factor design. In this application report, the *BQ21061 I2C Controlled 1-Cell 500-mA Linear Battery Charger With 10-nA Ship Mode, Power Path With Regulated System (PMID) Voltage, and LDO* is routed without using any via-in-pad. This saves not only on board cost for the PCB but also demonstrates very small form factor for a feature-rich device.

Contents

List of Figures

List of Tables

Trademarks

1 Introduction

When every little detail matters and cost must be reduced without sacrificing functionality, in-pad vias become the easiest design feature on a PCB to remove. When it comes to WCSP packages, such as the BQ21061, a lack of vias can make accessing pins and routing to pins difficult and non-ideal. To combat these problems, two designs were implemented that are small form factor and two-layer solutions that combine functionality and saves on board area.

The first solution utilizes a diagonal trace to connect $\overline{LP}$ to an NC pin. Though limited by PCB manufacturing capabilities, it provides the simplest access to the low-power mode of the device. Low-power mode provides a low quiescent current and extends the run time of the device. The second design takes a user input pin to the gate of a MOSFET that connects the $\overline{MR}$ pin to ground or leaves it floating. Typically, communication to the device is not available in battery mode as it is prevented when the $\overline{LP}$ pin is pulled down to put the device into low-power mode. Communication with the BQ21061 device can be activated once $\overline{MR}$ is pulled down when the device is in low-power mode

Both designs take advantage of pin optimizations to create situations where the device is still functional, routable, and accessible. The following layout guide enables a user to use the BQ21061 chip scale package and discusses the steps taken in the design of two configurations as well as their features.

2 Design A: Routing $\overline{LP}$ pin With 4.5-mil Copper Spacing

One pin in particular is able to bypass the issue of routing and become accessible through the NC2 pin. As the NC2 is a floating no connect pin, the $\overline{LP}$ can be shorted with it and retain its functionality, creating an easy access point to route the $\overline{LP}$ pin. Figure 1 shows a diagonal short in the top layer on these two pins and Figure 2 shows the spacing between the trace and an adjacent pin.

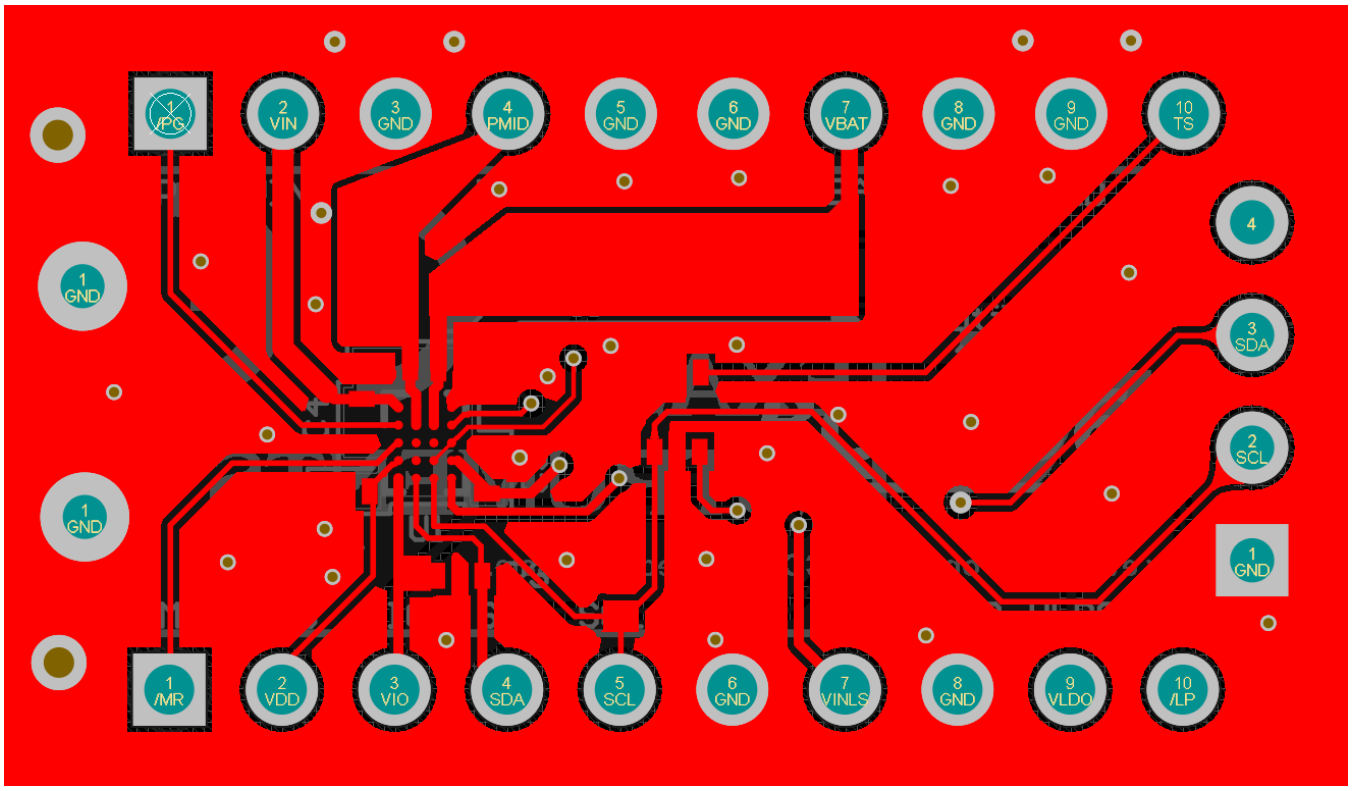

Figure 1. Design A: Top Layer

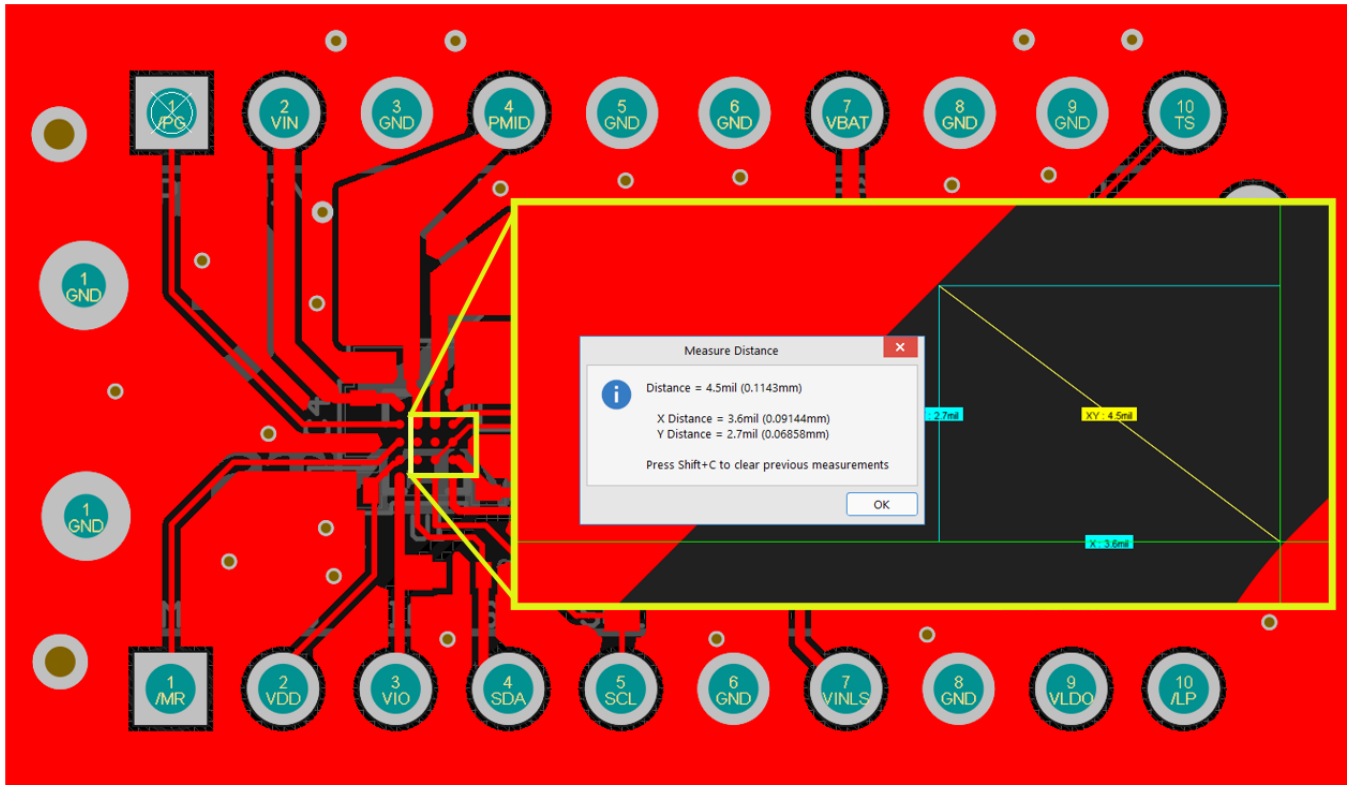

Figure 2. Design A: Showing the Spacing Between the $\overline{LP}$ Trace With Adjacent pin

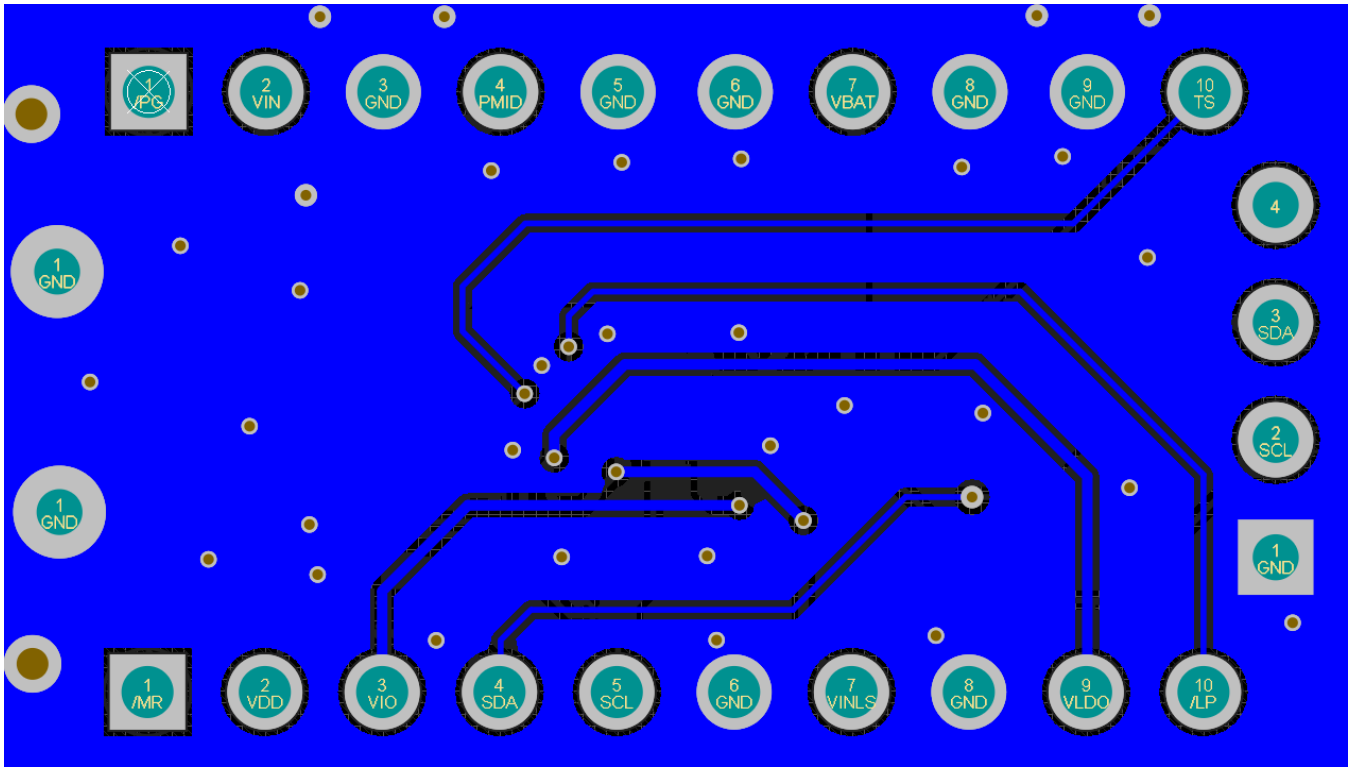

Figure 3. Design A: Bottom Layer

Advantage of the $\overline{LP}$ pin and routing

To create an accessible $\overline{LP}$ pin for routing, the design takes advantage of two factors: the NC2 pin and a 4.5-mil trace clearance. The NC2 pin is a no connect pin on the WCSP package that is more accessible than the $\overline{LP}$ pin. To be effective, the NC2 pin can be connected with the $\overline{LP}$ pin, effectively giving the $\overline{LP}$ pin more accessibility when it comes to routing this pin. The second factor is the 4.5-mil spacing between trace and an adjacent pin. With such little room to maneuver between pins on a WCSP package, finding ways to connect the two pins without in-pad vias and only two-layers while satisfying a 4.5-mil width clearance. Figure 4 shows the implementations of these two factors.

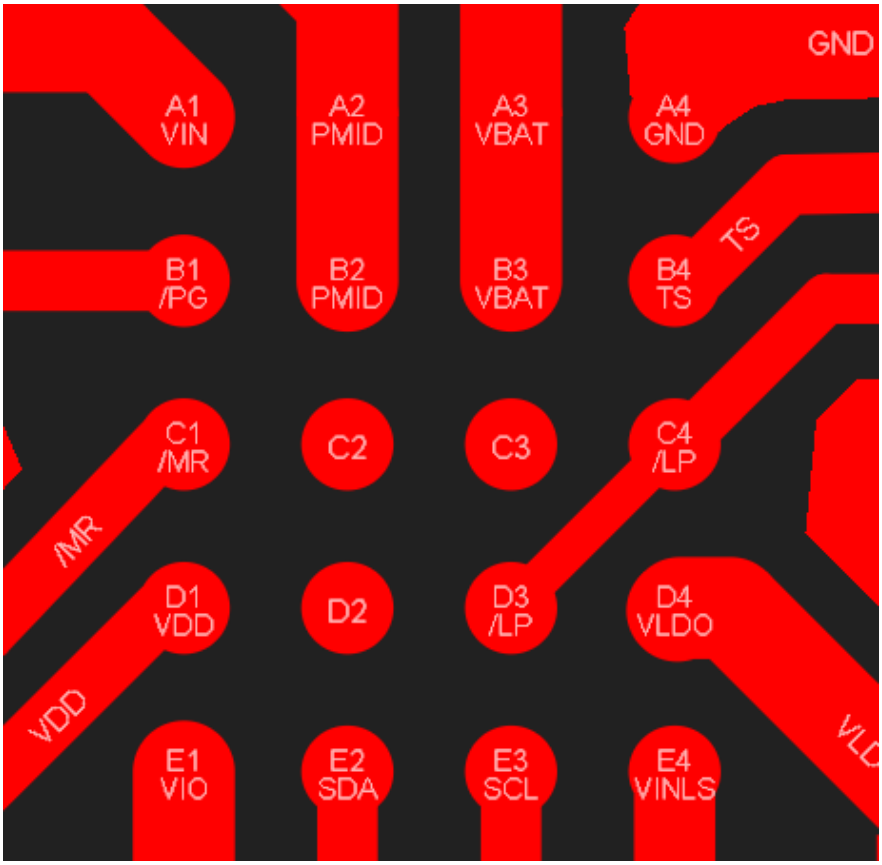

Figure 4. Design A: Routing Between the $\overline{LP}$ pin and the NC2 That Satisfies 4.5-mil Copper Clearance

The limiting factor for this design is the copper clearance requirement. This is because it is highly dependent on the capabilities of the PCB manufacturer. The use of this design is only available when the PCB manufacturer can agree to building a PCB with this clearance. Otherwise, no access to the $\overline{LP}$ pin is available, leaving low-power mode inaccessible.

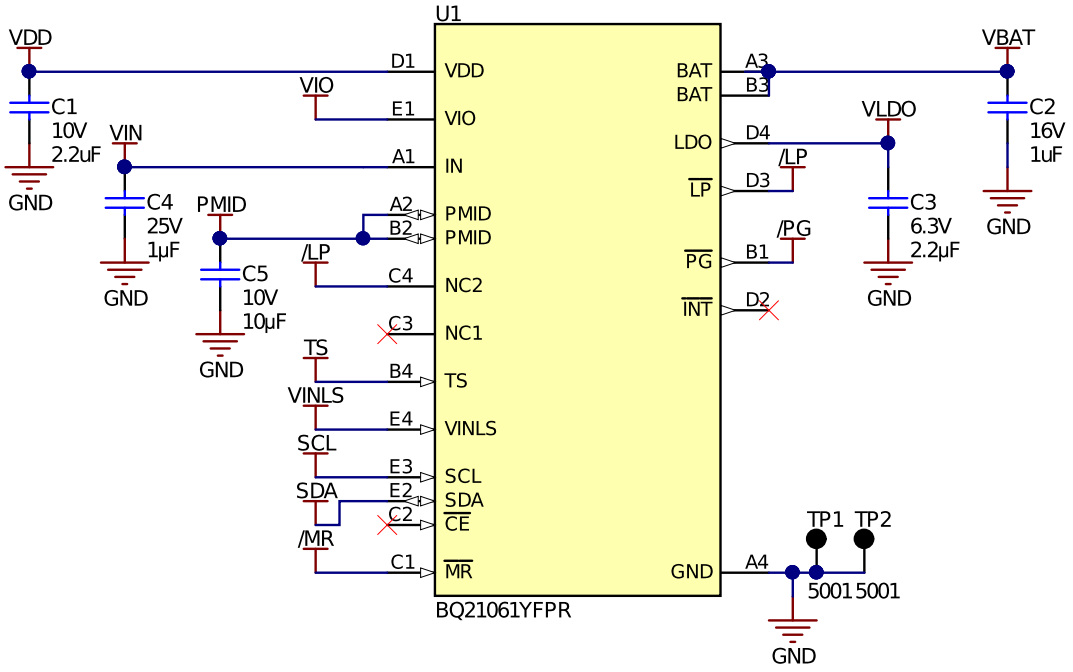

Figure 5. Design A: $\overline{LP}$ Optimized Routing Schematic

Schematic and Pin Optimization

- $\overline{LP}$ pin is shorted with NC2 pin for easier routing
- $\overline{CE}$ pin is left floating. It is internally pulled low with a 900-kΩ resistor and enables charging when low.
- $\overline{INT}$ pin is left floating. Normally used to output signal fault interrupts, the $\overline{INT}$ pin can be bypassed by reading any of the three fault flag registers with I2C

3 Design B: Toggling $\overline{MR}$ Through NMOS to Exit Low-Power Mode to Perform I2C Transactions

Many products have no push-button interface and only use an n-MOSFET (nMOS) connected to a microcontroller to control wake up and other actions. One of the features of the BQ21061 device is that you can access I2C controls when $\overline{MR}$ pin is low.

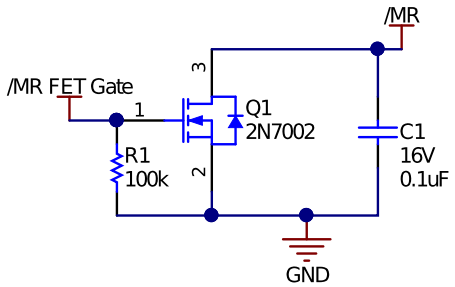

Figure 6. nMOS Schematic for Toggling the $\overline{MR}$ pin

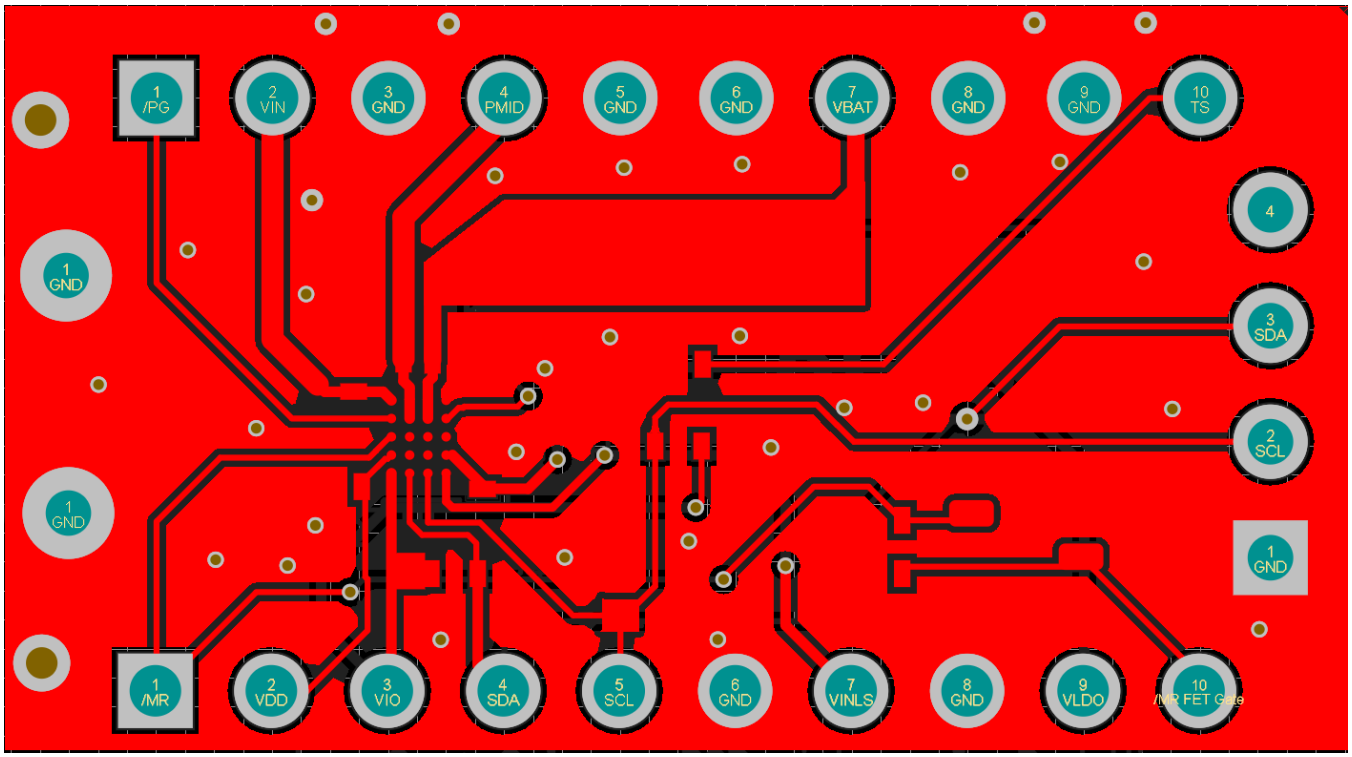

Figure 7. Design B: Top Layer

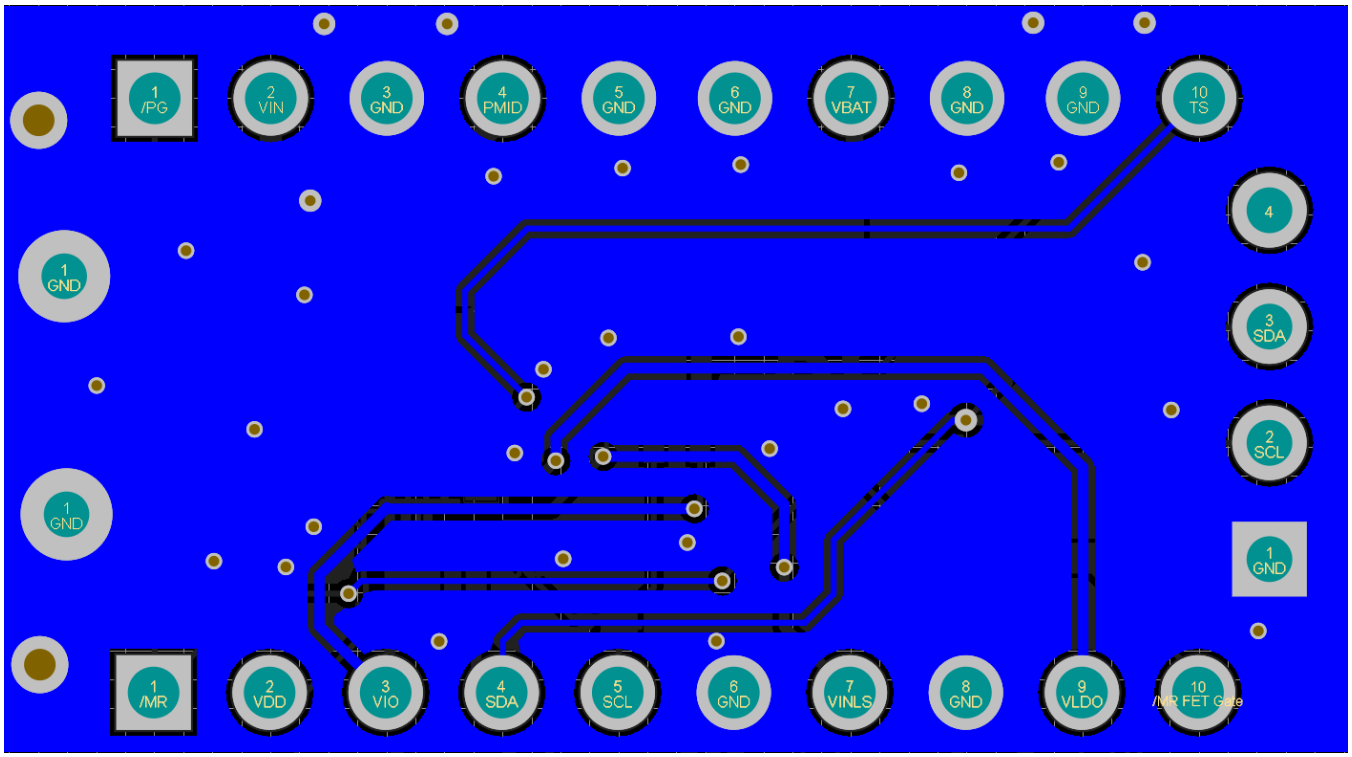

Figure 8. Design B: Bottom Layer

The $\overline{MR}$ pin is described as a pin that allows the user to reset or wake up the BQ21061 device from ship mode. In this design, the main functionality is providing active battery mode to the device. Active battery mode allows the device to communicate over I2C while only being powered by a battery. It should be noted that wake timers and hardware reset registers may have to be adjusted in this design.

To provide a way for the user to interact with the $\overline{MR}$ pin, a MOSFET is used. Figure 6 shows a 2N7002 MOSFET used with a capacitor and resistor to control the $\overline{MR}$ pin.

The MOSFET now allows for the user to use a signal to pull the $\overline{MR}$ pin to ground to reset, wake up, or interact with the device through I2C. When the gate of the MOSFET is high, the $\overline{MR}$ pin is pulled low and allows for communication. Otherwise, the $\overline{MR}$ pin is internally pulled up to BAT through a 900-kΩ resistor. Figure 9 shows the inability to communicate with the device when the $\overline{MR}$ pin is high and communication being valid when the $\overline{MR}$ pin is pulled low.

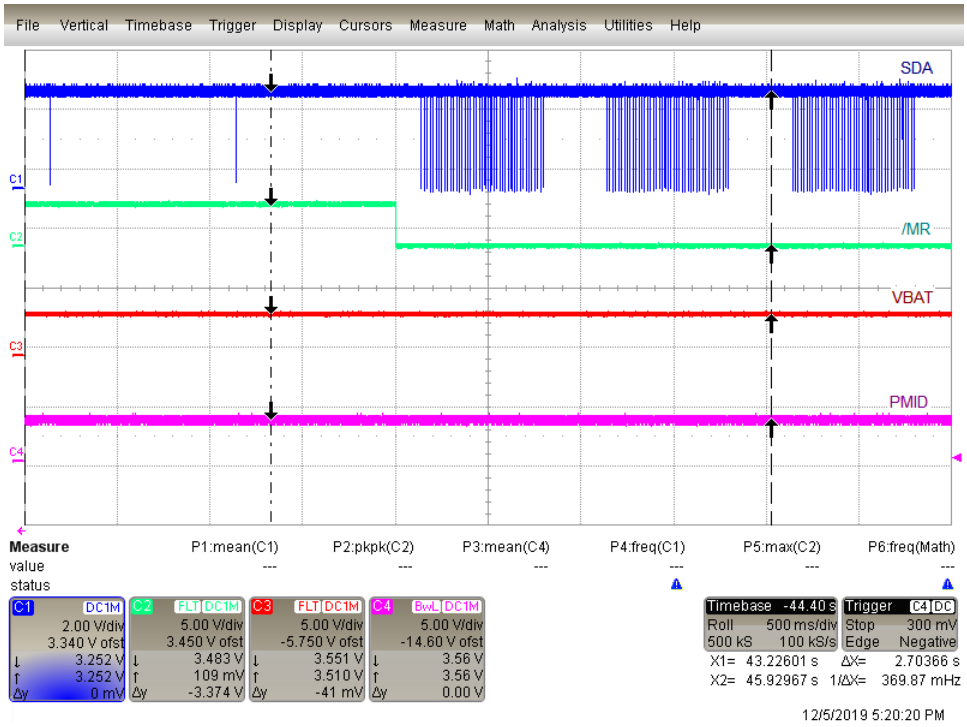

Figure 9. I²C Communication When $\overline{MR}$ is low

Notably here is the $\overline{MR}$ signal waveform. The gate of an nMOS is pulled high through a GPIO which allows the $\overline{MR}$ pin to be pulled low. As shown, I2C communication is attempted before and after the $\overline{MR}$ is pulled low and only occurs once the $\overline{MR}$ pin is low. When battery voltage is the only voltage source present, I2C is normally not possible if the device is not in active battery mode.

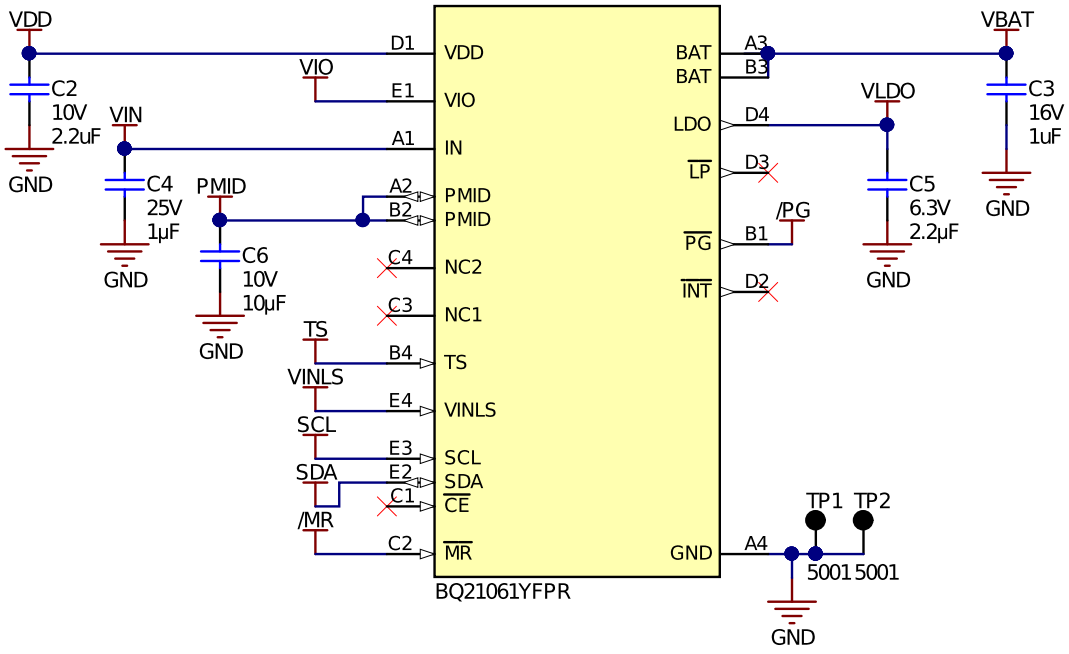

Figure 10. Design B: nMOS to Toggle $\overline{MR}$ Schematic

Schematic and Pin Optimization

- $\overline{CE}$ pin is left floating. It is internally pulled low with a 900-kΩ resistor and enables charging when low.
- $\overline{INT}$ pin is left floating. Normally used to output signal fault interrupts, the $\overline{INT}$ pin can be bypassed by reading any of the three fault flag registers with I2C
- $\overline{LP}$ pin is disconnected. The pin is internally pulled low and puts the device in low-power mode

4 Summary

Two designs have been created for the BQ21061 device that optimize pin connection and functionality to reduce solution size and reduce cost. The first design is dependent on a 4.5-mil trace width that connects the $\overline{LP}$ pin and the NC2 pin, allowing for the low-power pin to be accessed on the PCB. In the event where PCB manufacturing constraints do not allow for this solution to be possible, the second design allows for I2C communication while $\overline{LP}$ is pulled low through the use of a MOSFET that can pull $\overline{MR}$ low. Both designs optimize the pin connections, allowing for full functionality in situations where small form factors and efficiency are a priority.

5 References

1. Texas Instruments, *BQ21061 Product Page*
2. Texas Instruments, *BQ21061 I2C Controlled 1-Cell 500-mA Linear Battery Charger With 10-nA Ship Mode, Power Path With Regulated System (PMID) Voltage, and LDO Data Sheet*
3. Texas Instruments, *BQ21061 Setup Guide Tool*
4. Texas Instruments, *E2E™ Support Forums*

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265