Application Report
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Achieve Cooler Thermals and Less Power Loss of Your GaN Half-Bridge Design with the LMG1210

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ABSTRACT

When increasing the switching frequency of your GaN half-bridge design, the system will experience an increase in power loss. Like other power FETs, GaN FETs are limited by their thermal performance and need good thermal design to remain cost effective. The key to cooling down the system and reaching higher power density is having lower power loss. To reach 99 % efficiency in a 1-kW power stage system, less than 10 W of power loss can be dissipated. The driver's power consumption can be minimized to less than 1 W or 1 % of the total power by employing the proper techniques. Driver losses include quiescent, dynamic and gate charge losses and can limit the system's maximum potential efficiency. Having lower driver losses can enable higher efficiencies and can help prevent thermal dissipation problems. A cool system needs a fast, low power gate driver to positively impact the efficiency. LMG1210 can help minimize driver thermal dissipation to cool the system down while help achieve better layout technique, thermal management with two separate thermal pads and low LDO losses using a low LDO input voltage.

1 Overtemperature Protection Feature

A good practice when designing the most efficient gate drive circuit is taking good layout technique and thermal management into consideration. The system needs to be protected from thermal faults, so LMG1210 has three overtemperature protection (OTP) circuits. LMG1210 has a separate OTP circuit for the high-side, low-side and LDO to prevent the device from drawing too much current. The maximum operating junction temperature is specified in the datasheet as 125°C and the first OTP fault is at 150°C minimum. This 25°C minimum difference allows headroom for thermal transients before an OTP fault is reached. The low-side OTP fault will shut off both high-side and low-side outputs while the LDO remains on. If the low-side rises 10°C to 160°C minimum the LDO OTP fault occurs and shuts off the LDO. If the high-side reaches 160°C minimum only the high-side will shut off. Designing the OTP should be done for fault conditions in the system and should not be caused as part of system operation.

2 Simultaneous OTP trigger point

LMG1210 has two separate high-side and low-side thermal pads with their own OTP circuits. To ensure the OTPs are triggered at the same time, the two thermal pads need to be sized according to the power dissipation. The low-side OTP has a lower trigger point than the high-side OTP which means it will trigger first with equal power dissipation. Using the LDO creates additional power dissipation on the low-side which also makes the low-side OTP trip first. With equal power dissipation, the low-side OTP will trip first so either design the high-side thermal plane to be slightly larger or the low-side thermal plane to be slightly smaller. This will trigger the trip points simultaneously to compensate for the 10°C minimum trigger point difference between the high-side and low-side. With unequal power dissipation as when using the low-side LDO, the thermal pad area should be sized with the same ratio of power dissipated. For example assuming the same FETs, with a 10V LDO input voltage, 2/3's of the power is dissipated on the low-side and 1/3 is dissipated on the high-side. Simultaneous OTP trip points can be achieved by allocating the high-side thermal pad with 1/3 of the total area and allocating the low-side thermal pad with 2/3's of the total area. A small amount of extra area can be subtracted from the high-side for margin due to a higher shut off point.

3 Deadtime Protection Feature

While switching a power hungry half-bridge at multiple megahertz, it's nice to have a few tricks up your sleeve. One of those tricks is very precise dead-time circuitry that can be changed on the fly for different load conditions. Although dead-time loss has nothing to do with associated driver loss, this high-frequency feature is not to be overlooked when discussing thermal dissipation. The dead-time needs to become shorter and is more important as the switching frequency becomes higher. Minimizing dead-time while driving GaN is important because third quadrant conduction losses are higher than MOSFETs. The additional third quadrant conduction loss with GaN is due to not having a parasitic body diode to clamp the source to drain voltage. Dead-time is limited by the commutation time of the bootstrap diode and charging the parasitic well capacitance C_{ISO} found in the datasheet. C_{ISO} has been minimized down to 0.25 pF in order to reduce power loss. Losses associated with the bootstrap can be found in more detail in Design Considerations for LMG1205 Advanced GaN FET Driver During High-Frequency Operation. When minimizing dead-time it is important to utilize LMG1210's precision dead-time circuit to prevent dead-time variation and associated dead-time loss. The possible dead-time values span from 0.5 ns to 20 ns using 1.8 MΩ to 20 kΩ respectively. Further details on LMG1210's dead-time circuit can be found in *Dead Time Optimization LMG1210 GaN Driver*.

4 LDO Protection Feature

To protect the GaN gate, LMG1210 has a 5 V precision LDO which allows the system to utilize an existing rail higher than 5 V. The LDO not only keeps the GaN gate safely at 5V but also allows input voltages up to 18 V. When using the LDO it's important to minimize the VIN supply voltage since too high of a supply voltage can cause LMG1210 to consume enough current to reach OTP. Since the LDO output is fixed at 5V, having as low a LDO input voltage as necessary will prevent excessive power dissipation on the low-side LDO. The optimal VIN voltage of the LDO is set by the max dropout at 100 mA max LDO current, which is 6V. Using a low LDO input voltage will prevent unwanted gate drive losses in the LDO and help cool the system down.

5 Current Consumption Driver Sources

After getting to know LMG1210's high-frequency features, it's time to walk through an example to calculate LMG1210's worst case power consumption using the switching parameters in Table 1. LMG1210's current consumption can be divided between the high-side and low-side and has three sources of power dissipation:

- Driver Quiescent Current
- Gate Charge Current
- Driver Dynamic Current

In addition, if used, the low-side has additional losses in the LDO.

Table 1. Power Dissipation Example Parameters

PARAMETER	VALUE	UNIT
Switching Frequency	10	MHz
VIN voltage	8	V
Dead Time	1.5	ns
Dead Time Resistor	575	kΩ
Gate Charge	3	nC

6 Gate Charge Current

Gate charge-related current consumption can be calculated using Equation 1.

$$I_{chg} = Q_g \times f_{sw} \quad (1)$$

Assuming the same FET is used for both the high and low-side in our example, each consumes 30 mA of current.

7 Driver Dynamic Losses

When switching with no load, LMG1210 consumes additional current from no load driver switching loss. This is because both the high-side and the low-side have intrinsic dynamic current consumption beyond the quiescent current, which can be calculated in Equation 2 where I_{xS_DYN} is the dynamic current consumption in the high-side or low-side found in the LMG1210 datasheet.

$$I_{DYN} = f_{sw} * I_{xS\_DYN} \quad (2)$$

In our example where f_{sw} is 10 MHz, the dynamic current consumption is 12.5 mA for the low-side and 6.1 mA for the high-side.

8 Driver Quiescent Losses

The high-side quiescent current, found on the datasheet, must be added to the power dissipation calculation. In this case, it is 0.85 mA max. If operating in IIM, the low-side quiescent current can be found in the datasheet as 0.475 mA max, but in PWM mode, the dead-time resistors add additional quiescent current. This additional quiescent current can be calculated using Equation 3.

$$I_{qdxx} = 1.8 / (25\ k\Omega + R_{ext}) \quad (3)$$

Since R_{ext} is 575 kΩ in our example, the additional dead-time quiescent current is 3 µA for each resistor, or 6 µA total. So the total low-side quiescent current is 0.481 mA max. Table 2 shows a summary of the terms we calculated in Equation 3:

9 Driver Current Consumption Summary

Table 2. Current Consumption Summary

PARAMETER	I_Q (mA)	I_{DYN} (mA)	GATE CURRENT (mA)	TOTAL (mA)
High-side Current	0.85	6.1	30	36.95
Low-side Current	0.481	12.5	30	43

10 High-Side Power Consumption

At this point we can calculate the power dissipation of the high-side. Since we did not use a gate resistor we can make the assumption that all the gate charge loss occurs inside the gate driver. If using a gate resistor, refer to section 2 from Design Considerations for LMG1205 Advanced GaN FET Driver During High-Frequency Operation. The high-side power consumption is equal to the total high-side current times the bootstrap voltage. Let's assume that the bootstrap voltage is 4.5V, so the power dissipated in the high-side die is 166 mW shown in Table 3.

11 Low-Side Power Consumption

Turning our attention back to the low-side, we can take the calculated low-side current consumption and produce a low-side power consumption of 43 mA * 5 V = 215 mW. However this calculation does not account for the low-side LDO losses, which is discussed in the next section.

12 LDO Power Consumption

In our example, the VIN voltage is larger than necessary at 8 V so the LDO has a 3 V drop across it. The LDO current is supplying the low-side and the high-side current, therefore the total current through the LDO is 80 mA which falls within the 100 mA maximum LDO current. The power dissipation in the LDO is equal to the voltage drop across the LDO, 3 V, multiplied by the current through the LDO, 80 mA, to equal 240 mW in this case. The total power dissipation in the low-side is the sum of the 240 mW from the LDO and the 215 mW from the gate driver and associated circuitry, or 455 mW total found in Table 3.

Table 3. Power Dissipation Example Summary

PARAMETER	TOTAL POWER (mW)
High-side die power dissipation	166
Low-side die power dissipation	455

13 Power Dissipation Example Summary

From our example, the total power dissipated by LMG1210 while switching 3 nC at 10 MHz in a half-bridge configuration is less than 1 W. In comparison, the high-side power consumption is much less than the low-side due to the LDO losses and additional dynamic current of the low-side. This result indicates that when cooling the LMG1210, 3 times the thermal plane area should be devoted to the low-side since it dissipates almost 3 times as much power as the high-side. Good layout practice is recommended to improve thermal management, for more detail refer to the LMG1210 layout design guide in section 2 from TI Designs: TIDA-01634 Multi-MHz GaN Power Stage Reference Design for High- Speed DC/DC Converters. Designing as low a LDO input voltage as necessary is recommended to minimize driver power dissipation.

14 Overall Summary

To unlock the fastest yet coolest and most efficient GaN or MOSFET half-bridge design, a fast and versatile driver with stable control over the gate is required. LMG1210's internal LDO can be used to protect the GaN gate, however when using the LDO some design recommendations should be implemented to minimize driver power loss to cool the system down. While incorporating good layout technique and thermal management, the area of the high-side and low-side thermal planes should be split with the same ratio as the ratio of the power dissipation. Separating LMG1210's thermal pad power dissipation and including a low LDO input voltage can improve thermal performance and cool your system down.

Table 4. Additional Information

DESCRIPTION	TITLE
LMG1210 Datasheet	*LMG1210 200-V Half-Bridge MOSFET and GaN FET Driver*
LMG1210 User's Guide	*Using the LMG1210EVM-012 user's guide*
Designing With LMG1205	*Design Considerations for LMG1205 GaN FET Driver for High-Frequency Operation*
Optimizing Dead Time with LMG1210	*Dead Time Optimization LMG1210 GaN Driver*

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