Application Report
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Solar Inverter Layout Considerations for UCC21220

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ABSTRACT

Solar inverter designs are becoming more compact, with higher system voltages and higher operating temperature requirements. The high power output and complex control system requires a gate driver to support the system controller. Traditional level-shifter based designs have limited working voltage capabilities, and the high-side circuitry is not flexible enough to drive more complex multi-level topologies. The UCC21220 basic-isolated dual-channel gate driver eliminates many of the limitations of level-shifter based gate drivers, enabling designers to work with higher operating voltages and more complex topologies while maintaining spectacular timing parameters, high operating temperature, and minimal additional board area. This application report describes the layout guidelines that should be observed to minimize time spent on PCB development and revision when using UCC21220 in solar inverter projects, based on real-world use cases and debugging experiences.

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1 Primary Side Layout Considerations

In solar inverters with fast common-mode transients, high currents will inevitably couple between the primary and secondary ground circuits. When one of these ground circuits has a high resistance or inductance, the coupled transient currents will create large voltage differences between two points on the same electrical node, which manifests as ground bouncing or high-frequency ringing. Both of these voltage effects become significant when the input circuit path must travel more than a few centimeters between UCC21220 and the PWM controller, adding risk for gate drive input corruption or damage to the controller outputs. Figure 1 shows the common-mode current paths as the high side node begins charging the output inductor.

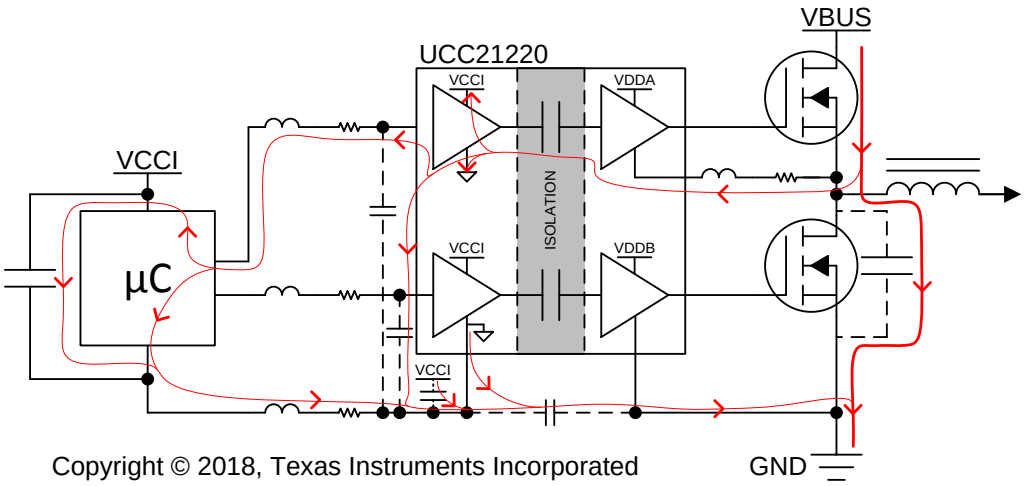

Figure 1. Common-Mode Transient Current Path

To demonstrate this common-mode current path, Figure 2 shows a double-pulse test performed with UCC21220 in two cases: on the left, with input bypassing removed and INA/INB/DIS pins driven by a TTL output several inches from the gate driver; on the right, following the layout guidelines given in this application report. When proper layout techniques and critical input components are ignored, the input noise from the test circuit at 400V is large enough to significantly disrupt the output. Even worse, the output disruption can trigger another noise event, causing the output to oscillate chaotically. However, with the addition of the input filter, DIS pin capacitor, and VCCI bypassing close to the gate drive input pins, the input signal remains clean despite several inches between the driver and the signal source.

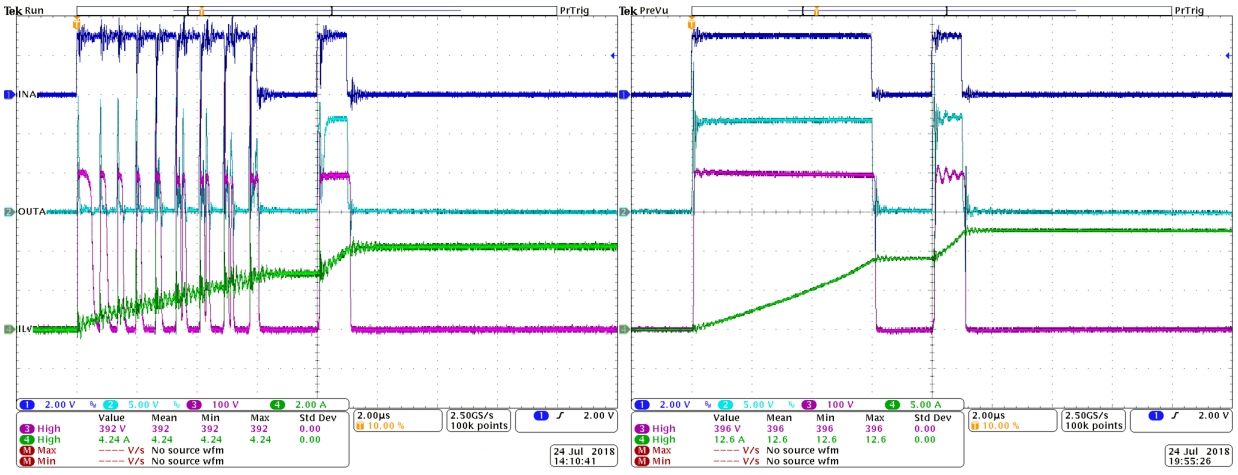

Figure 2. Effect of Input Components on Common-Mode Transient-Induced Input Noise

There are multiple critical input components and layout guidelines that should be observed for a successful design. The following list summarizes the key suggestions, and provides some details about the application impact.

1.1 Critical Input Components

- **Use capacitive input filters to suppress high-frequency noise.** Use when the PWM controller and the gate driver are separated by more than a few centimeters, or when fast common-mode transients are expected. A small capacitive filter with up to 100 pF and up to 100 Ω suppresses high frequency noise on the input terminals of the driver. The exact values should be selected to have a corner frequency and phase shift that begins at least one decade above the switching frequency to maintain a square-shaped pulse on the input.
- **The filter resistor helps protect the controller.** The series resistance limits the current to or from the controller during ground bouncing, damps any parasitic inductance in the gate drive line which may contribute to ringing, and helps to suppress any EMI absorbed by long input traces.
- **The filter capacitor rejects common-mode noise.** The input shunt capacitance diverts high-frequency common-mode noise currents on the inputs directly to the ground point.
- **Use input pull-down resistors for deterministic start-up and shut-down.** A pull-down resistor near the input pin ensures that the filter capacitor is completely discharged if the controller output initializes in an unknown state, or if the controller output is damaged. This pull-down resistor should have a value at least ten times the input filter resistor value to minimize the voltage divider impact.
- **The input components add negligible power dissipation.** With 100-pF capacitors on each input, 1-MHz PWM frequency, and 3.3-V input drive, less than 3 mW of power dissipation is added. Two 5-kΩ pull-down resistors driven with typical microcontroller voltages will add less than 5 mW of additional power dissipation, mostly concentrated in the resistor.
- **Disable pin: Tie to ground, or use a 1-nF capacitor.** If the DIS pin is unused, it should be tied directly to the GND pin. When using a controller to drive the DIS pin over a few inches or more, the UCC21220 requires a 1-nF capacitor with low ESR/ESL, placed close to the pins. In cases where fast disable response time is required, place the controller closer to the driver, use high drive strength outputs, and minimize the loop inductance.

1.2 Layout Guidelines

- **Pour an uninterrupted ground plane directly beneath the IC.** An uninterrupted input ground plane minimizes both resistance and inductance, keeping the common-mode impedance low. Every effort should be made to keep all input components and pins directly above this plane.
- **Bypass VCCI to the ground plane, close to the IC pins.** Bypass on the same layer using at least one low ESR/ESL ceramic capacitor. A second low-value ceramic capacitor is suggested to help shunt the common-mode transient current directly to the ground plane. The value of this capacitor can be determined during prototyping, by selecting the lowest impedance at the induced ringing frequency.
- **Prioritize bypassing VCCI on pins 3-4, not pins 8-4.** Pin 3 (VCCI) and pin 4 (GND) are internally bonded close together, the bond wires from these pins to the die are short, and the loop inductance between these pins has been optimized for low impedance power delivery across frequency. Pin 8 (VCCI) is internally bonded to pin 3 through approximately 0.2Ω at DC, but the distance of the bond is longer and the loop inductance is larger, so the AC impedance will also be larger.
- **Minimize VCCI capacitance to the secondary side.** Ideally, a low-impedance VCCI plane should be used to deliver the supply to each VCCI pin, and the supply and ground planes should be back-to-back in the layer stackup to improve the supply capacitance. Practically, many designs cannot afford more than two layers. In these cases, to minimize the surface area presented by the VCCI trace for common-mode transient exposure, avoid running VCCI along the back side of the driver or under other pins. Keep VCCI surrounded by low-impedance ground plane as much as possible.
- **Tie no-connect pins to a low-impedance node (VCCI or ground).** Avoid floating pins whenever possible. Tying primary-side no-connect pins to VCCI also permits drop-in functional replacement with UCC21222 and other SOIC-16 isolated dual channel gate drivers with a dead-time pin.

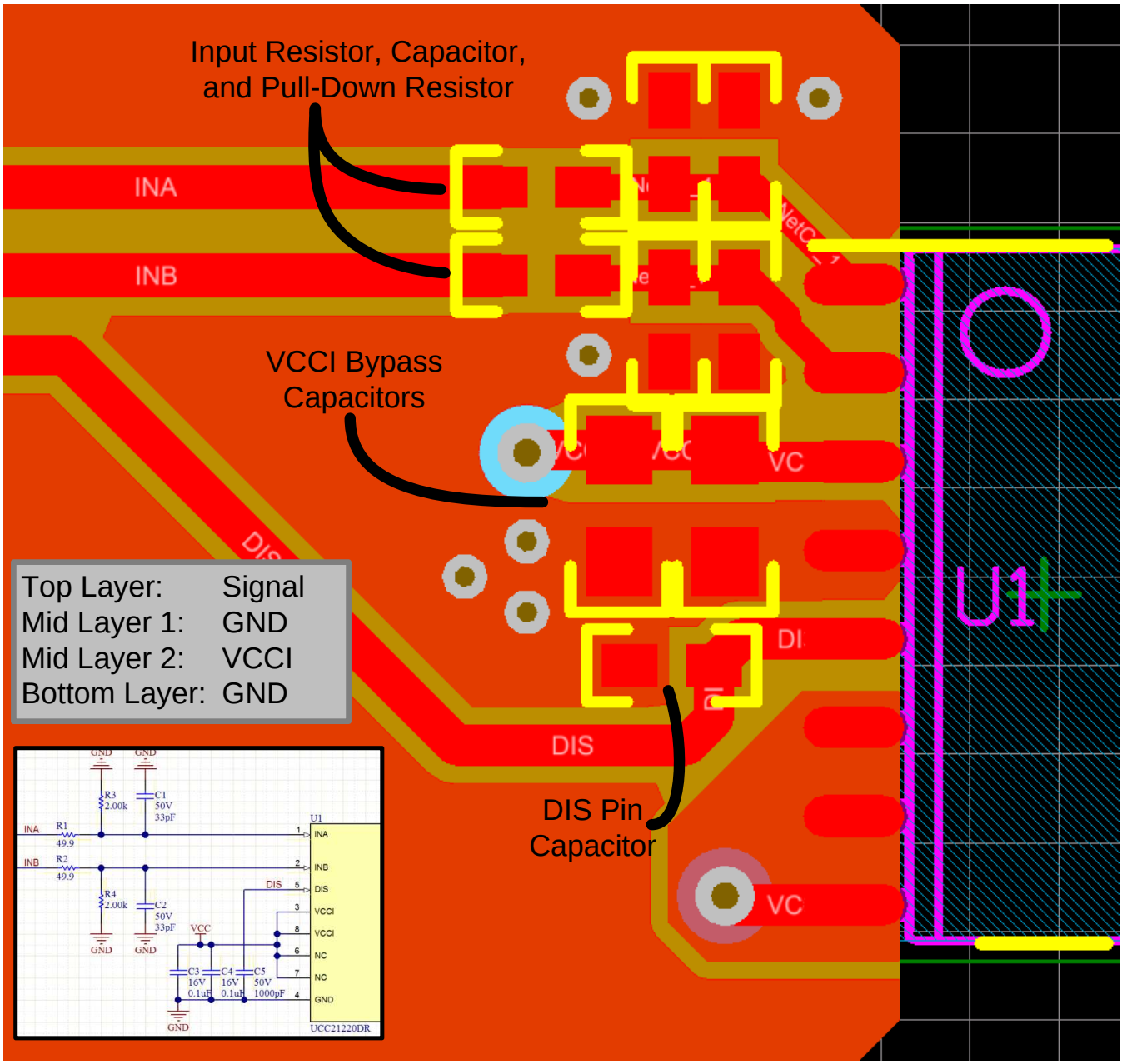

Figure 3. Primary Side Layout Summary

Figure 3 summarizes the layout guidelines with a PCB layout image.

2 Secondary Side Supply Considerations

2.1 Supply Bypassing

Gate drivers control the transfer of charge from a local bypass capacitor to the gate of a transistor. In all use cases, regardless of supply voltages or expected output currents, an absolute minimum 0.1-µF bypass capacitor is suggested, to be placed directly at the VDD and VSS pins of a driver output channel. This external capacitance is necessary to maintain the stability of internal regulators controlling the output logic and isolation decoding. For loads with drive currents that require external current buffers, it may be tempting to omit this capacitor in favor of a larger capacitor at the buffer as in Figure 4; in reality, the cost "saved" by omitting this capacitor will be a fraction of the added cost in debugging time and board respins.

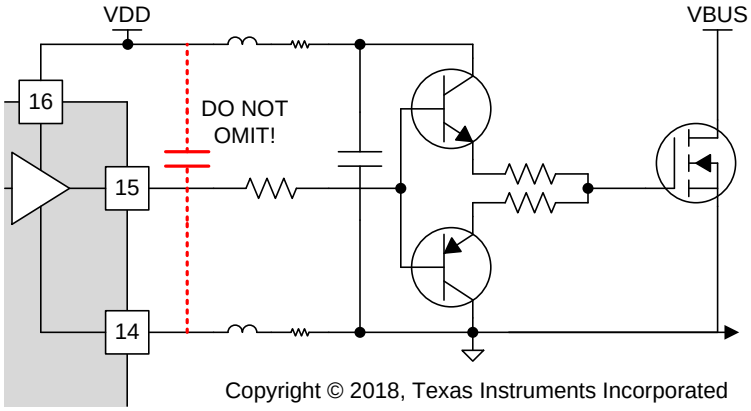

Figure 4. UCC21220 Output Bypassing is Required

The recommended maximum supply voltage for UCC21220 is 18 V, which is more than enough for most high voltage power MOSFETs. Consequently, use of a split supply is not common. Still, some cases may call for split supplies for added noise immunity. When using split supplies, it is helpful to understand the current paths during the switching cycle: the current for turn-on is supplied entirely by the upper capacitor (VDD→Source) and the current for turn-off passes entirely through the lower capacitor (Source→VSS) as in Figure 5.

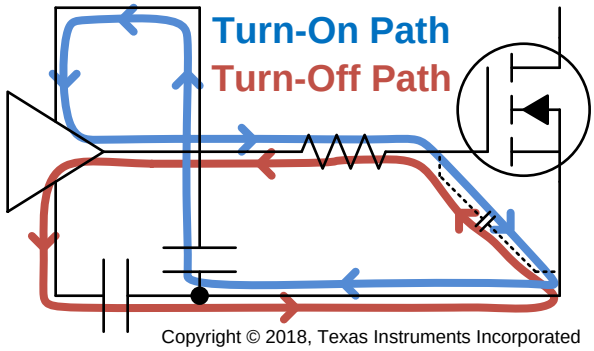

Figure 5. Current Paths for Split Capacitor Bypassing

With the turn-on and turn-off path in mind, placing an additional single capacitor between VDD and VSS can provide some benefit as a local bulk capacitor, since the split capacitors in series are reduced to their harmonic sum. It can be difficult to place three capacitor appropriately, since including them on the same layer as the gate driver typically increases the gate drive loop inductance by pushing the split capacitors farther away from the IC pins. On the other hand, placing the capacitor below the device through vias can add several nanohenries of inductance between the capacitor and the IC pins. Usually the space required for vias beneath the IC can be better utilized with an additional capacitor on the same layer as the UCC21220.

Different capacitor values are not recommended for upper and lower capacitors. Since the same current passes through both capacitors each cycle, using different capacitor values causes asymmetric voltage ripple on the supply pins. Smaller value capacitors increase the current ripple from the supply, which may interact undesirably with the supply line parasitic inductance to produce ringing. Smaller value capacitors, more insidiously, can generate sudden spikes in the total supply voltage during turn-off, pushing the VDD→VSS voltage closer to the absolute maximum (a problem compounded by the greater VDD→VSS voltage required for split supplies). The placement of split supply capacitors is suggested in Figure 6.

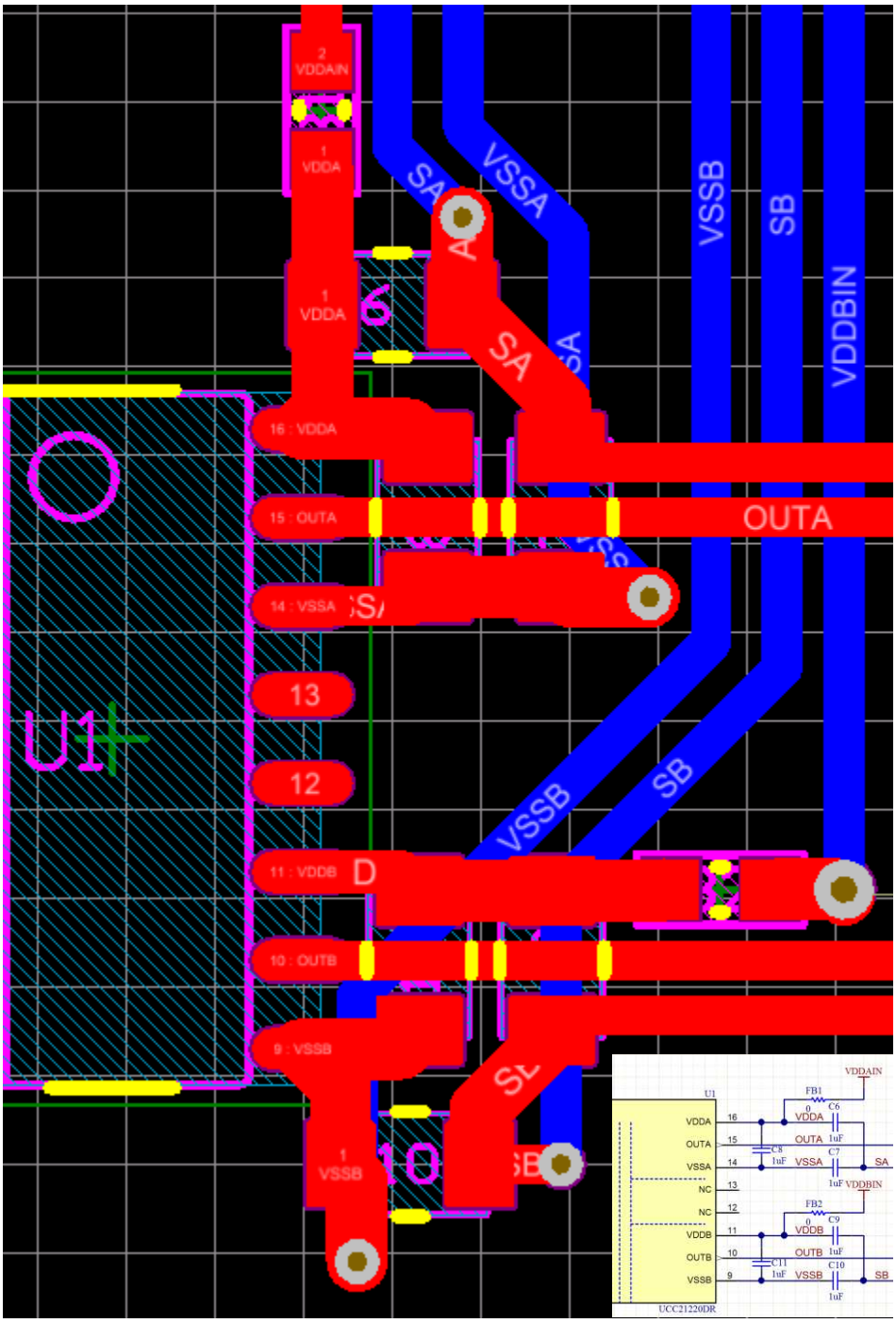

Figure 6. Recommended Placement for Split Capacitor Bypassing with UCC21220

Particularly stubborn noise spikes from the output supply source may persist despite using adequate bypassing capacitors or careful layout strategies. In some cases, the simplest solution may be inserting a ferrite bead into the supply lines. Ferrite beads present a much higher resistance at the blocking frequency than a low-valued resistor, with substantially improved filter performance as a result. In many cases, a series component is already designed into the supply line as a filter, and this component (usually a resistor) can simply be substituted with a ferrite bead. For initial system builds, it is a good idea to connect the supply through a 0-Ω resistor for precisely this kind of substitution: it is easy to remove in production if unneeded, but hard to insert on an unprepared test build.

2.2 Using Isolated Supplies with UCC21220

The topologies and duty cycles used in solar inverters frequently require isolated supplies to independently power the output channels of UCC21220. These isolated supplies are without question one of the most common cause of driver failures. Despite the wide availability of pre-packaged commercial isolated switching supplies for use with gate driver outputs, most of these designs are not rated for use with fast common-mode transients. In pursuit of lower costs, many designers create their own simple flyback circuits. But creating a robust, well-regulated flyback design is deceptively complex undertaking. Limited line and load regulation, magnetics variations over temperature, common-mode current injection into the feedback loop (if there even *is* a feedback loop), unbalanced winding inductances, and other confounding headaches strain the patience of every isolated supply designer. Instability and poor output regulation on the UCC21220 output supply will quickly lead to unexpected jumps in the supply voltage, which can cause significant damage to the gate driver and the rest of the switching circuit.

Simple post-regulator circuits as in Figure 7 can be used to minimize the common-mode transient impact on supply regulation. The input voltage range can be made much wider than the 20V absolute maximum of UCC21220, filtering any overvoltage transients from the isolated supply. Keep in mind that the post-regulator may have stability concerns as well, such as noise susceptibility, undervoltage transients, and phase margin issues. In one memorable case, during debugging of an inverter system, it was discovered that shifts in temperature could shift the value of the output capacitor, and the resulting phase shift would cause the input ripple of the isolated switching converter to become amplified instead of attenuated.

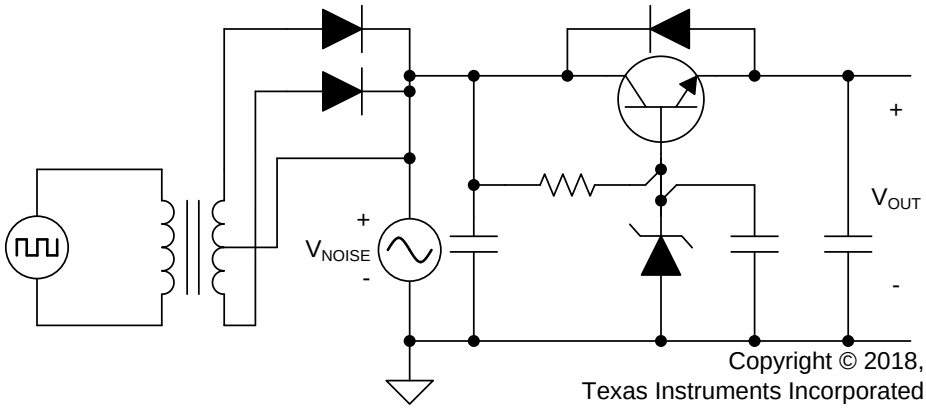

Figure 7. Simple BJT Linear Post-Regulator Circuit

3 Gate Drive Output Considerations

3.1 Driving Multiple Transistors

To minimize the on-state resistance and the power dissipation in the switching transistors, many solar inverter designs use multiple transistors in parallel, driven from a single gate driver output. UCC21220 is capable of driving multiple transistors, as long as appropriate layout considerations are made. The output connections of UCC21220 should be kept as short and wide as possible. The connections to the load transistor gate and source should be placed very close together to minimize loop inductance. Every nanohenry of extra inductance contributes to higher output ringing, which can affect the timing of the gate drive pulse between transistors, or damage the output of the UCC21220. When running the same output to multiple transistors, the outputs should share as much trace length as possible, and the length of the split segments should be equalized to minimize layout-related propagation delay mismatch. See Figure 8 for examples of this principle applied.

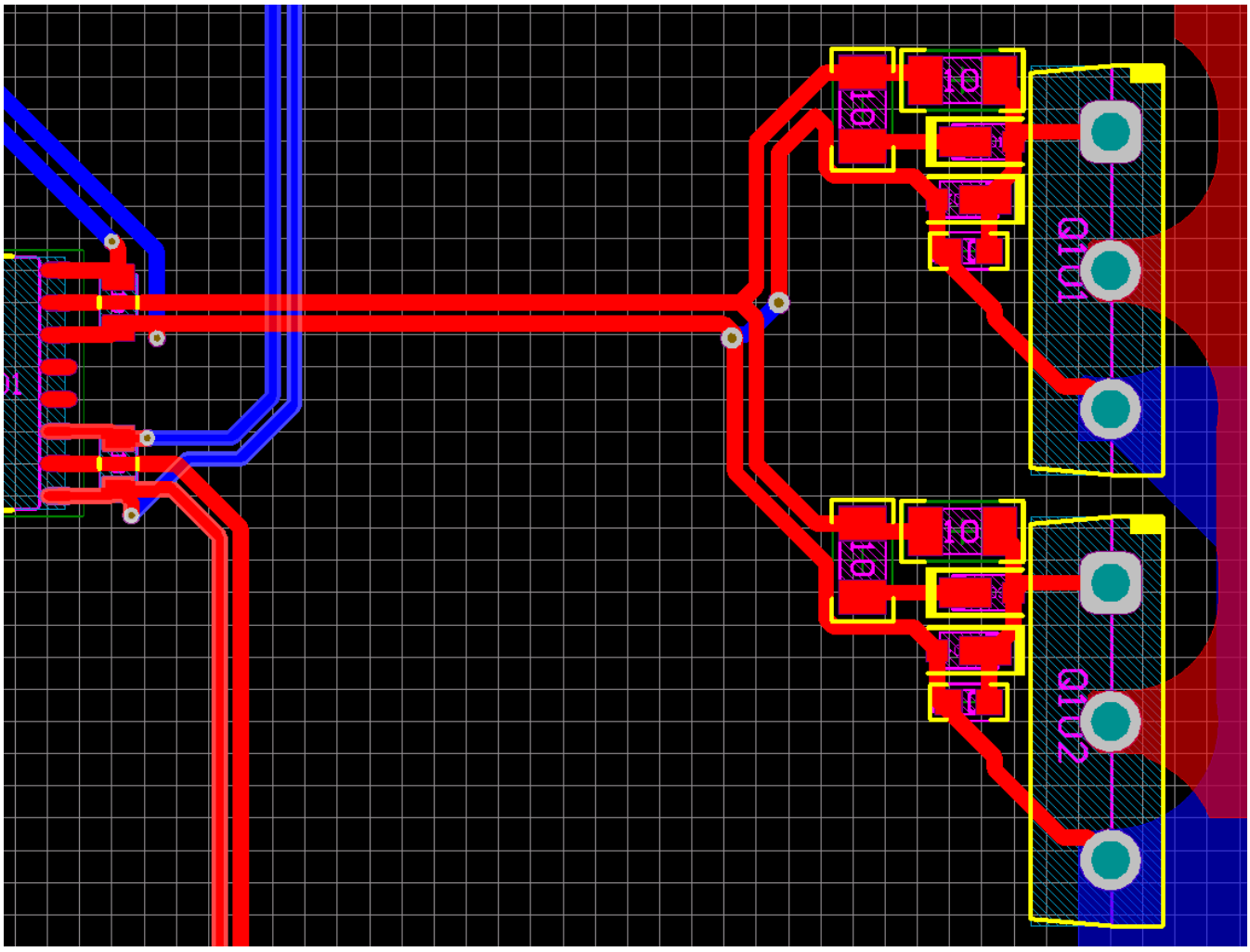

Figure 8. Length Equalization for UCC21220 Driving Two Load Transistors

3.2 Output Buffer Circuits

Buffering drive signals can help to deliver very high currents with minimal extra loop area, but proper layout techniques still must be used to realize the benefits of a buffer circuit. Buffering circuits require their own bypass capacitors close to the buffer pins, or else the effects of supply line inductance will severely hinder the output voltage and become the epicenter of excessive ringing throughout the supply lines. As previously mentioned, the buffer capacitors should never be used in place of a bypass capacitor for UCC21220. Capacitors at both the buffer and the driver IC must be present for optimal system performance. For BJT-style buffers, the buffer input resistor must be small enough to ensure the required gate drive current across operating conditions. However, there are several disadvantages to overdriving the buffer inputs, including longer delay times and larger ringing on the gate driver output. When output ringing is an important concern, placing the buffer drive resistor close to the gate driver generally improves ringing at the gate driver. The buffer circuit rarely requires the base drive resistor to be close to the buffer, since the BJT input diodes can clamp excessive overshoot and undershoot. Remember that BJT buffers can have current gain factors of more than a hundred, so the peak current requirements from the gate driver should rarely exceed a few hundred milliamps. Figure 9 summarizes the layout guidelines for BJT buffer circuits with an example, including split supply considerations. R6, R7 and R8 are placeholder resistors, and their values should be changed to suit the application.

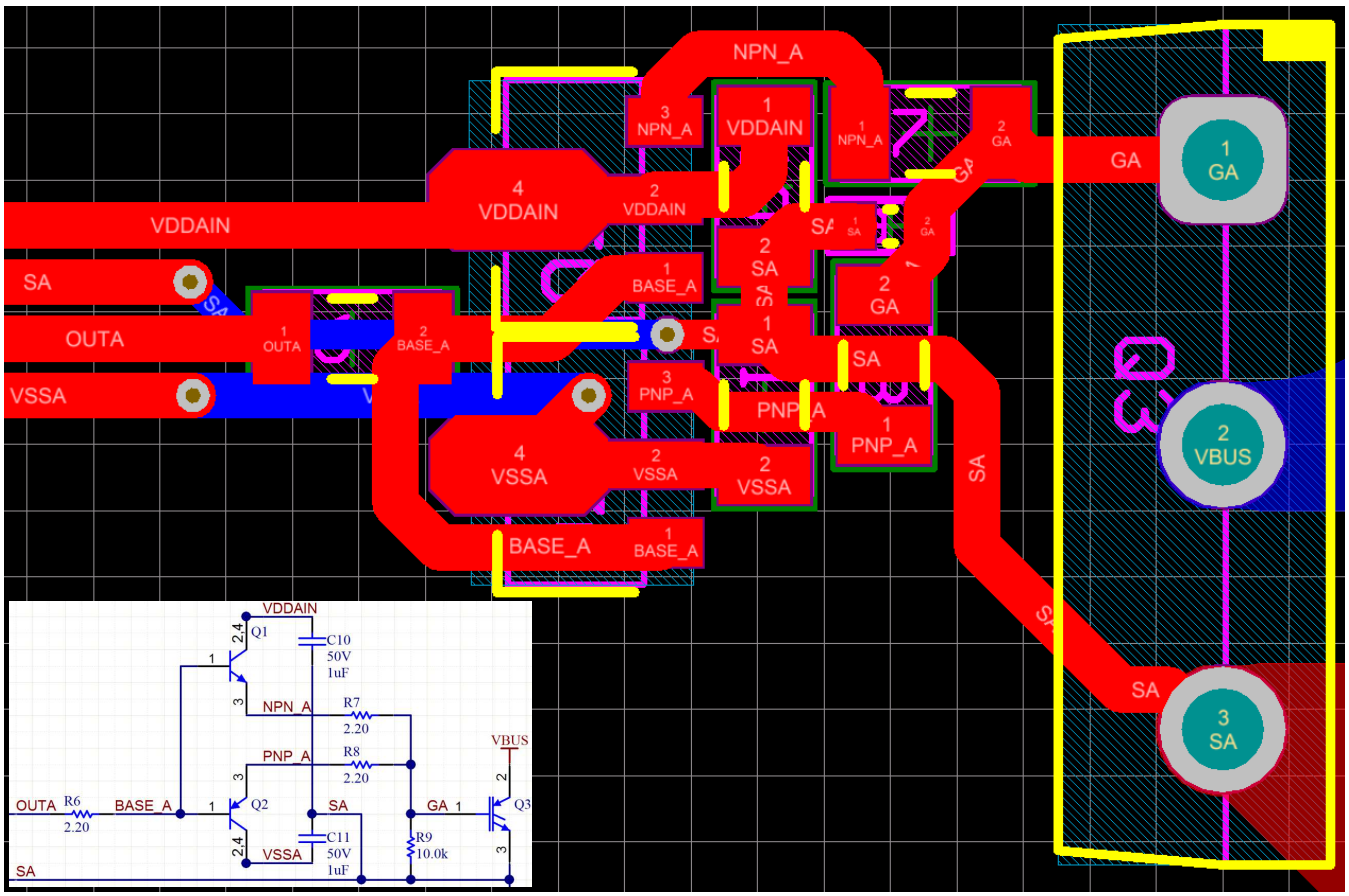

Figure 9. BJT Buffer Circuit Layout Strategy

3.3 Driver and Transistor on Separate Boards

A common trend in compact solar inverters and microinverters sees power transistors mounted on a separate board, for more convenient heatsinking and thermal management. Whenever a gate drive signal must pass through a board connector, it is absolutely essential that the transistor gate and source connections are closely coupled, with minimal interference from other connector pins or nearby inductors and magnetic fields. Consider the additional loop area created by the connector pin pitch, height, and diameter, as well as how it will affect the gate drive speed and the noise immunity. Whenever possible, use wide-pin connectors with fine pitch and low profile. While many connectors offer high current ratings, gate drive currents are almost exclusively high-frequency AC currents, and they will be impacted by connector parasitics and skin effect limitations. For high peak drive currents, consider using multiple connector pins to transmit the gate drive signal, since both resistance and inductance are reduced in parallel. Alternately, multiple pins can be more efficiently utilized by providing power to a buffer circuit located close to the switching transistor. Using a buffer can eliminate most of the gate drive loop inductance in the high current path while still providing high peak currents, and requires very little peak AC current from the gate driver.

4 Thermal Considerations

High ambient temperatures and compact layouts, characteristic of solar microinverters, require careful planning to accurately predict the power dissipation and thermal effects of the UCC21220. Some layout decisions can significantly improve thermal performance and minimize junction temperature increase. A large copper pour on the VSS pins can provide enough heatsinking to cut Θ_{JA}, the datasheet rated thermal resistance, in half. The UCC21220 datasheet gives detailed instructions in the application example for determining the power consumption due to loading, so these values can be predicted with high accuracy in advance. Many simulation tools also include a tool to calculate power dissipation, using the UCC21220 SPICE model provided on TI.com. And since the datasheet also provides Ψ_{JT} and Ψ_{JB}, the thermal characterization parameters, a simple thermocouple measurement at low ambient temperature can provide a verification of the junction temperature during hardware validation.

5 References

- UCC21220 Product Folder
- UCC21220 Datasheet
- UCC21220 Evaluation Module

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