Application Report
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bq76200 Reverse Voltage Considerations

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BMS: Monitoring and Protection

ABSTRACT

The bq76200 high-side, N-channel FET driver does not allow pins to go negative. While it may be common to have a flyback diode as shown in the EVM, some systems may want to allow the PACK+ to go negative. This document describes a circuit and test results that assist in the successful implementation of a reverse voltage circuit in a bq76200 battery application.

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Trademarks

1 Introduction

In a battery system, polarity is important to provide the proper voltage to the system and keep currents within design limits. The PACK+ terminal of a battery will typically be positive with respect to the PACK- terminal. In a lithium-ion battery with a switched protection circuit, once the protection has switched off the terminal is free to move. One situation where the PACK+ terminal may want to go negative is the inductive response of a load to switching off current during a battery protection event. Another is the reverse connection of a charger. A flyback or freewheel diode is one common solution to an inductive spike. An example is shown as D1 in Figure 1. The diode will provide a current path for the current to continue to flow in the inductance of the load while clamping PACK+ at the forward voltage drop of the diode below PACK-. The flyback diode will also short a charger connected with reverse polarity, up to the capability of the diode.

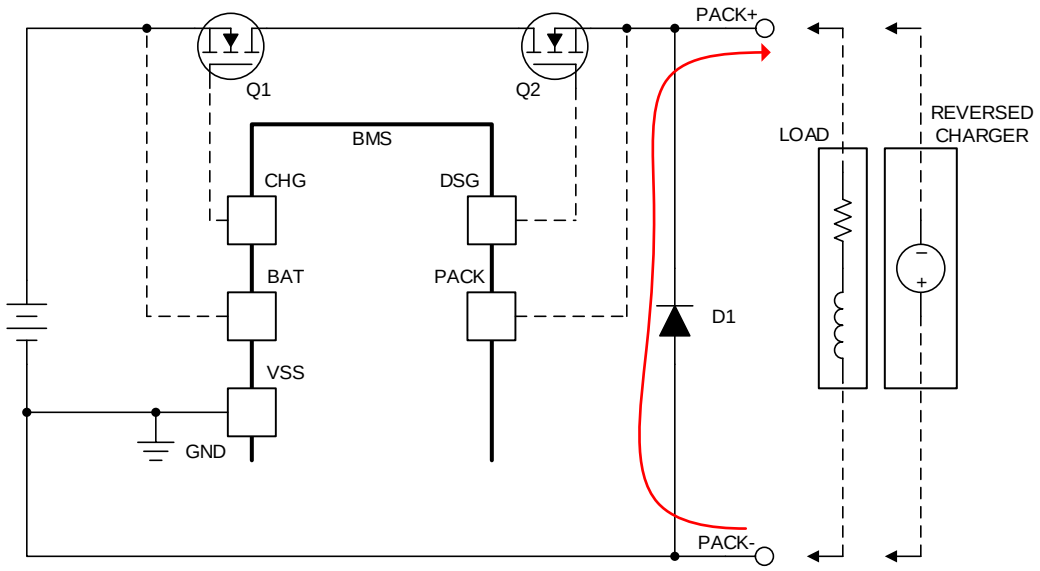

Figure 1. Flyback Diode in Battery

Some systems prevent reverse connection of charger through a unique connector interface. However, other systems may use a common connector type for the charger connection and have an opportunity for an incorrect charger to be attached and experience a reverse voltage condition. With a reversed charger, both the battery and charger want current to flow in the same direction. The result may be a short circuit or discharge to undervoltage with a protection event in the battery. If the charger has survived the event, the voltage goes negative. See Figure 2 as an example of current flow with a reversed charger. As the PACK+ terminal and discharge FET source are forced to a negative voltage by the reversed charger, the DSG pin remains at approximately 0 V. Since the R_{GS} is large with respect to R_{DSG}, the gate voltage is also near 0 V, so the Q2 discharge FET again conducts as a source follower and operates in the ohmic region which may cause heating of the FET and failure. The negative voltage developed will depend on the charger characteristic. The negative voltage produces a current in the PACK pin net limited by the Rp filter resistor. The current in the DSG pin net is small due to the large R_{GS} value. The sum of these two currents and the discharge FET current make up the reversed charger current.

In many integrated circuits including the bq76200 current drawn from the pins flows through a parasitic diode structure and results in a voltage violating the -0.3 V absolute maximum limit for the pins. The resulting condition could damage the integrated circuit. For the bq76200, current drawn from the DSG and PACK pins increases the BAT pin supply current and can damage the BAT pin filter resistor.

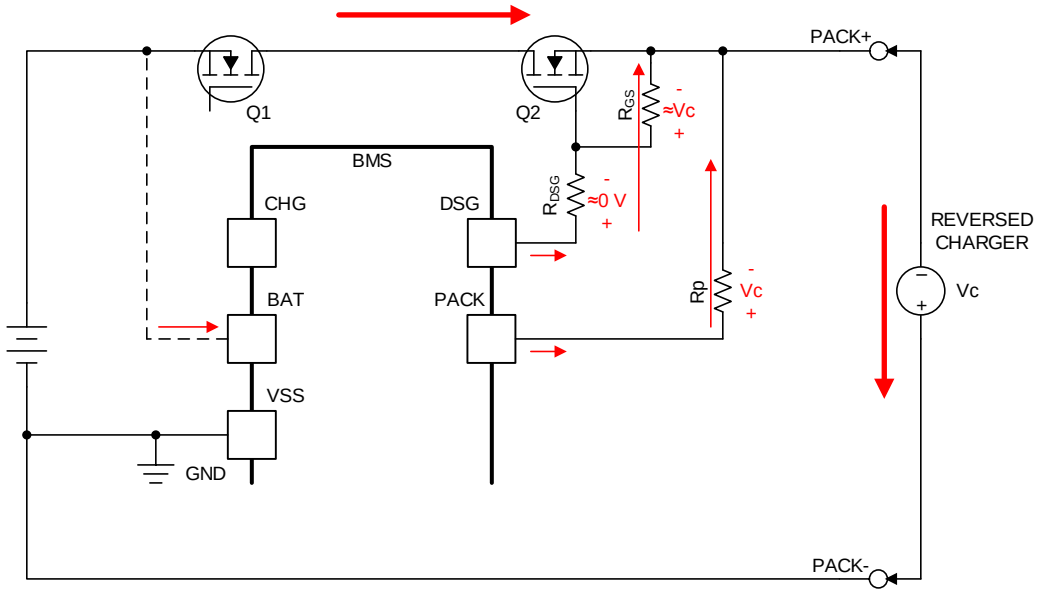

Figure 2. Currents With Reversed Charger Connection

A battery pre-charge circuit typically operates in parallel with the charge FET. Since voltage from the reverse charger is dropped across the discharge FET and the pre-charge circuit is not exposed to the reverse voltage, the pre-charge function is not included in this analysis.

2 Low Voltage Reverse Voltage Protection

A typical implementation of a reverse voltage protection circuit for a low voltage system up to approximately 18 V is shown in Figure 3. An N-channel enhancement MOSFET, Q3, is added across R_{GS} of the discharge FET with the gate connected to ground. Q3 is selected with a lower $V_{GS(th)}$ than Q2. When the PACK+ terminal goes negative the source of the clamp FET goes negative turning on the FET and clamps the discharge FET gate to the source preventing current flow. The negative voltage is dropped across the R_{DSG} resistor rather than the R_{GS} resistor. With the negative voltage on PACK+, the discharge FET sees the sum of the battery and charger voltages and must be specified with a suitable V_{DS} voltage. The reversed charger carries the sum of the current from the DSG and PACK pin nodes. When the IC is sensitive to the negative voltage on the PACK and DSG pins, the Schottky diodes D1 and D2 provide a current path from ground to avoid conduction from the IC pins. This circuit works while the battery and reverse voltages are within the absolute maximum V_{GS} limit of the clamp FET. If reverse voltages or transients exceed 20 V, the gate of Q3 needs protection components. Power dissipation in the Rf and R_{DSG} resistors during the reversed charger connection also imposes a practical limit on the voltage range of the circuit. At 16.8 V, the power in the typical 100-Ω Rp resistor for the bq76200 is 2.8 W.

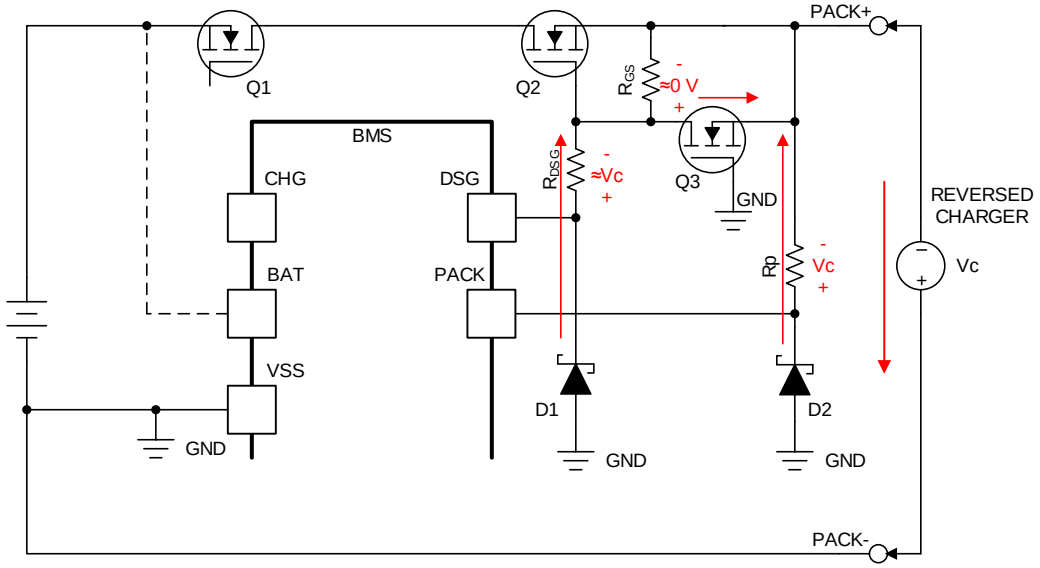

Figure 3. Low Voltage Reverse Voltage Clamp Circuit

3 High Voltage Reverse Voltage Techniques

When higher battery voltages are needed, some method to reduce the currents is needed to keep the power in the external components in a suitable range. Switching off the pin path or limiting the current drawn are methods to reduce the current and power in the resistors during reverse voltage. Figure 4 shows a circuit implementation for the bq76200 using a P-channel switch in the DSG pin path and a current limiter in the PACK pin path.

The voltage between the DSG and PACK pins controls the P-channel signal FET, Q4, to switch the DSG signal to the FET gate. When DSG is high, the Q4 FET is on and the DSG voltage is provided to the Q2 discharge power FET gate through R_{DSG}. When DSG turns off initially, the signal FET is on and the power FET gate is pulled down. Once the signal FET is off, it acts as a diode in parallel with R_{DSG2} to continue to pull down the gate. R_{DSG2} will limit the current from the DSG path during reverse charge while Q4 allows a lower gate resistance during normal operation.

In the PACK path, Q5 is an N-channel depletion mode MOSFET which is on when V_{GS} is 0 V. Rp is an added resistance to provide a gate-source voltage to Q2. When PACK+ is pulled below ground, the gate voltage of Q5 is driven low and Q5 begins to turn off, this provides a current limiting effect to reduce the power in the Rf and Rp resistors.

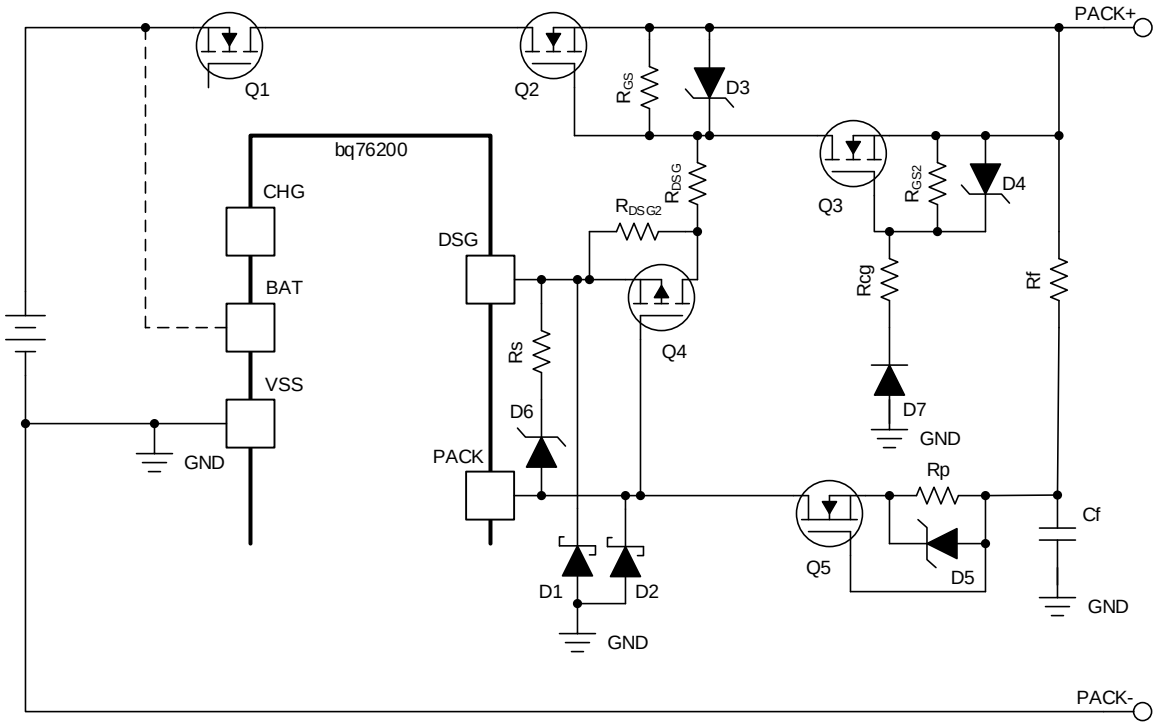

Figure 4. bq76200 Reverse Voltage Circuit

3.1 Component Selection

A circuit was constructed to test Figure 4. The battery protection MOSFETs in this test circuit are 100-V V_{DS} CSD19532Q5B. The typical 10-MΩ R_{GS} resistors from the bq76200 data sheet are used to minimize quiescent current and keep the load– on the charge pump low. The FET gates are protected with 16-V zener diodes.

A low voltage FET is used for a clamp FET since its voltage will not exceed the power FET gate voltage and is protected by the zener diode. A 2N7002 is selected for the Q3 FET, the gate is protected by a 16-V zener, a 10-MΩ resistor R_{GS1} keeps the FET off in normal conditions. When the PACK+ voltage is reversed, a 1-MΩ Rcg gate resistor with ground reference turns on the FET and has low power dissipation. A 1N4148 diode D7 prevents constant current in the gate resistor when the PACK+ is at normal voltage.

In the DSG path, R_{DSG} is 510 Ω to provide adequate turn on and turn off of the DSG FET. Larger R_{DSG} values slow turn off and allow the DSG pin voltage to increase during turn on. Smaller values allow more current to be pushed into the DSG pin by a transient or fast charger voltage rise on PACK+. An 18-V zener D6 and 100-Ω resistor Rs are used between the DSG and PACK pins to avoid internal conduction and losses during switching. It is desirable to have a P-channel FET with a $V_{GS(th)}$ lower than the 2.6 V typical $V_{GS(th)}$ of the power FET. An available BSP322P FET was used for Q4 since its $V_{GS(th)}$ voltage is 1.5 V, typical. R_{DSG2} is 10 kΩ to provide a pulldown across the FET when it is off. This value provides 0.1 mA/V with a reverse voltage applied and at –50 V the power in the resistor is 0.25 W. The value can be adjusted for derating, as needed.

In the PACK path, filtering should not be increased arbitrarily since it slows the response of the PACK pin to the actual PACK+ voltage and can slow switching of the discharge FET. Rf and Cf are kept at the typical recommended values of 100 Ω and 10 nF. The resistance in the PACK path should be relatively small due to an approximate 5-mA bias current when both PACKDIV and PRECHG are on. The BSS169 depletion mode FET was available and is used for the Q5 current limiter. The BSS169 has a $V_{GS(th)}$ voltage of –2.2 V typical, a 200-Ω Rp provides this voltage at 11 mA. Actual current depends on the FET characteristic. While these values were used for the test circuit, the power dissipation and safe operating area (SOA) of the BSS169 FET do not allow continuous operation at high voltage. A larger resistor value

reduces the current and power dissipation in Q5 but results in more voltage drop when PACKDIV and PRECHG are used, and could affect switching due to the filter effect of the resistance and PACK pin and net capacitance. A FET with either a smaller $V_{GS(th)}$ to reduce the current or a higher power dissipation would keep the part in its SOA at high voltage. A 16-V zener diode prevents transients from exceeding the Q5 FET maximum V_{GS} while allowing normal operation.

The Schottky diodes, D1 and D2, provide current from ground to the DSG and PACK nets for the reverse voltage source. The Schottky diodes are selected for a low forward voltage to keep the node voltage within the absolute maximum of the IC and to have an acceptable leakage at normal pack voltages. The leakage current of the diode on the DSG node provides a load on the charge pump during normal operation. The BAT46W diode has a maximum forward voltage of 0.45 V at 10 mA and a maximum reverse current of 2 µA at 75 V at room temperature. While the forward voltage does not meet the absolute maximum voltage of the bq76200 with the currents described previously, the components were available and used in this test circuit.

Table 1 summarizes the components used in the test circuit. These values do not represent a finished design, they are test values used to illustrate the circuit concept. Select values to provide operation within the component limits for the circuit requirements of the system and test to confirm operation.

Table 1. Test Circuit Component Values

Reference Designator	Part or Value
Cf	10 nF
D1, D2	BAT46W
D3, D4, D5	MMSZ5246B 16V
D6	MMSZ5248B 18V
D7	1N4148W
Q1, Q2	CSD19532Q5B
Q3	2N7002
Q4	BSP322P
Q5	BSS169
R_{GS}, R_{GS2}	10 MΩ
R_{DSG}	510 Ω
R_{DSG2}	10 kΩ
Rf, Rs	100 Ω
Rp	200 Ω
Rcg	1 MΩ

3.2 Test Results

When a negative voltage is applied to the pack terminals with the bq76200 disabled, currents into the circuit are shown in Figure 5. Battery current into the circuit remains low over the voltage test range. Current from the reverse voltage source to PACK+ increases with the reverse voltage. A measurement with the DSG pin disconnected shows that the R_{DSG2} resistor is a substantial source of the reverse supply current, and while the Q5 circuit limits current, it is not a constant current. The clamp FET gate bias current is included in the PACK+ currents, but the value of Rcg limits the current to less than 0.1 mA at 100 V.

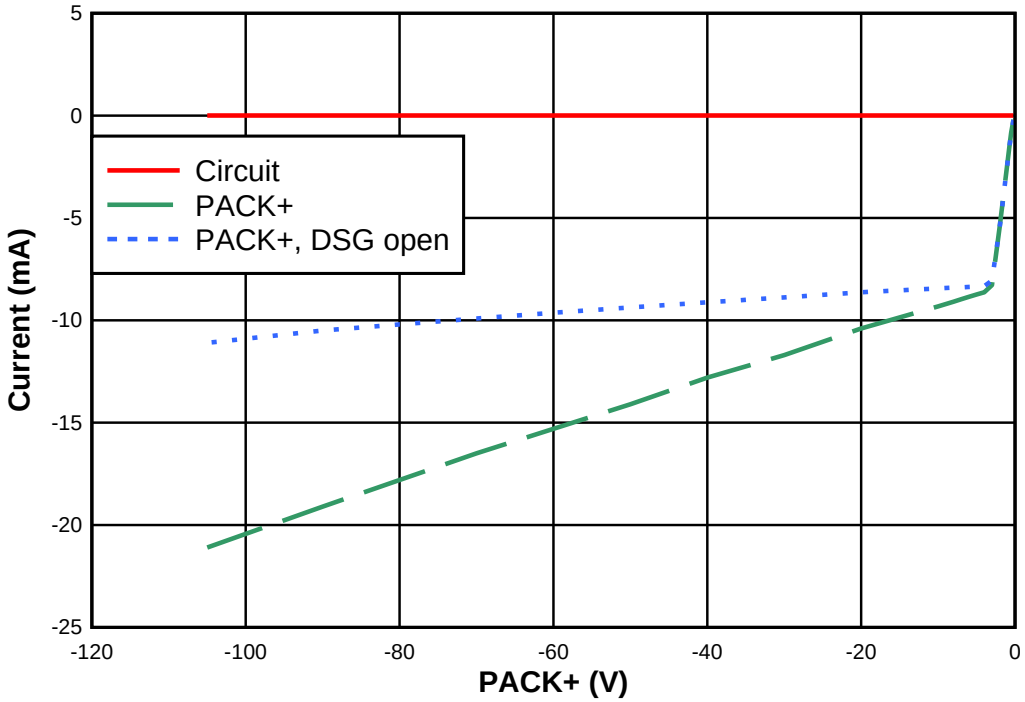

Figure 5. Test Circuit Currents With Reverse Voltage

One concern with adding components is a possible change in the switching behavior of the circuit. Discharge FET turn off of a similar circuit without the reverse voltage components is shown in Figure 6. Figure 7 shows the turn off of the discharge FET with the Figure 4 circuit. When DSG is turned off, the current ramps down but some current lingers as the PACK+ voltage falls. An effect from the capacitance of the switching components in the reverse voltage circuit is observed in the bump on the PACK signal, but turn off is similar. Figure 8 shows an example of short circuit turn off with a protector controlling the bq76200.

NOTE: Waveform captures in this document show charge current as positive.

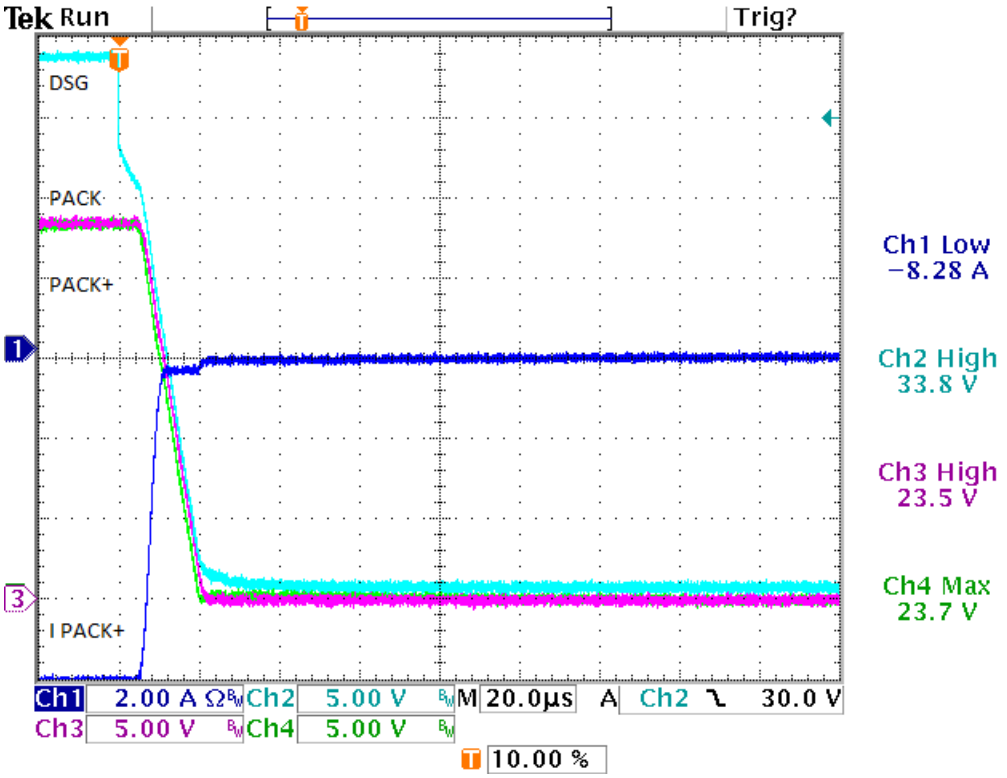

Figure 6. Turn Off With Normal Circuit

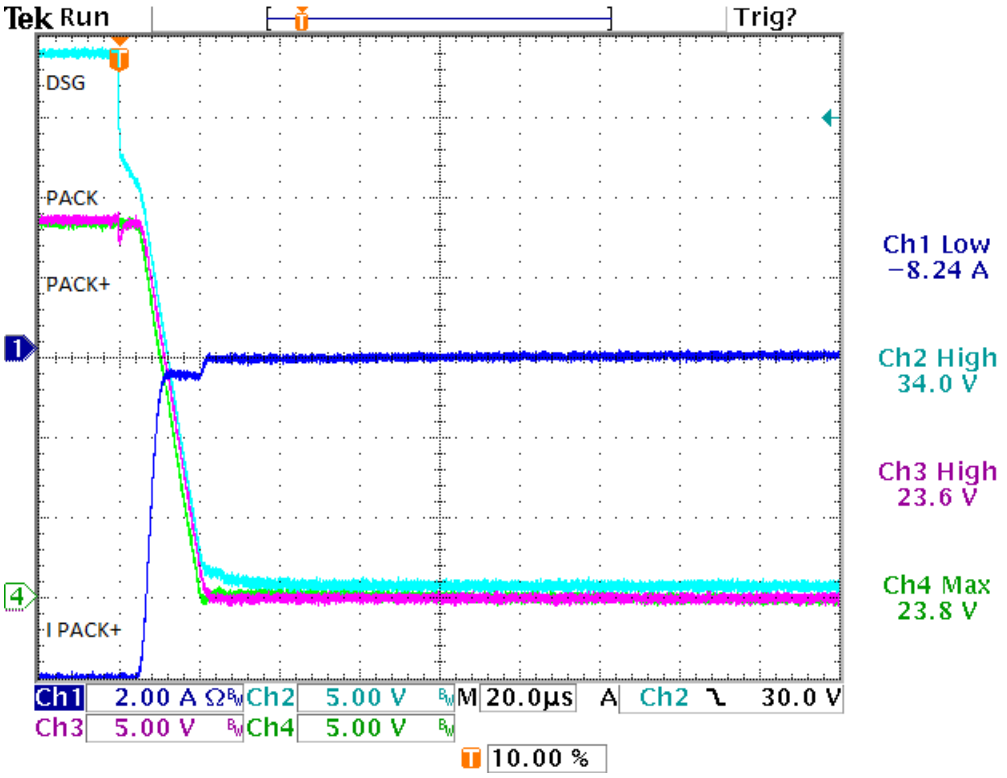

Figure 7. Turn Off With Reverse Voltage Circuit

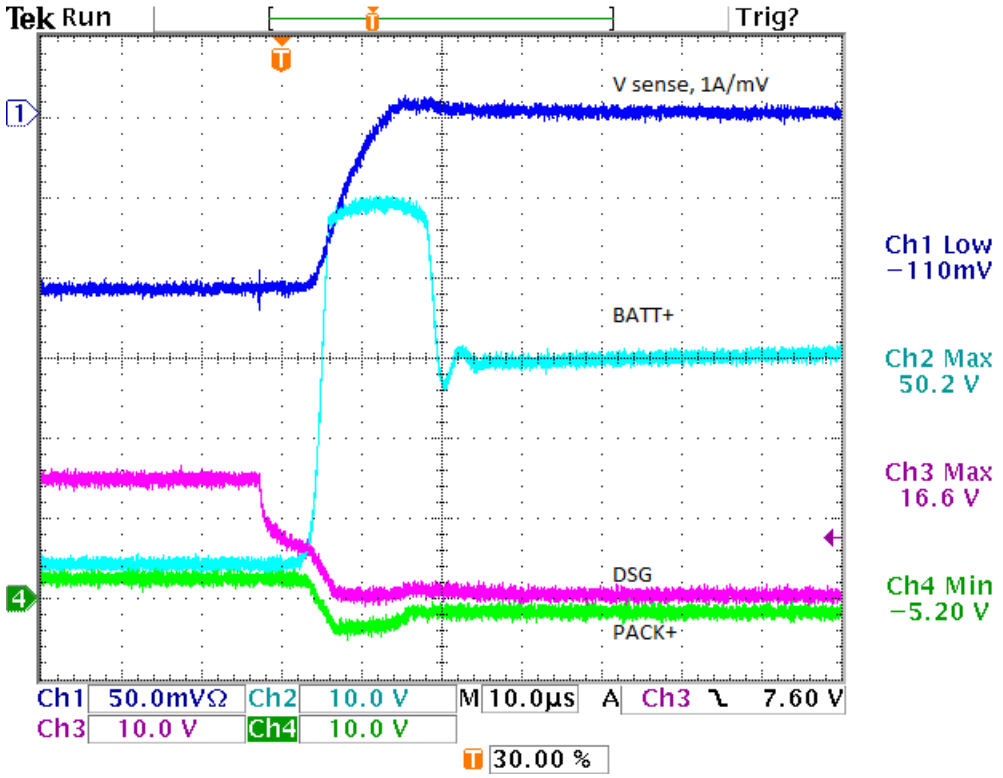

Figure 8. Short Circuit Turn Off With Reverse Voltage Circuit

When a reversed charger is connected to an enabled circuit, after the protection event the charger recovers and a negative voltage develops on PACK+. The voltage waveform will depend on the charger characteristic. Figure 9 shows an example of a reverse voltage applied after DSG switching.

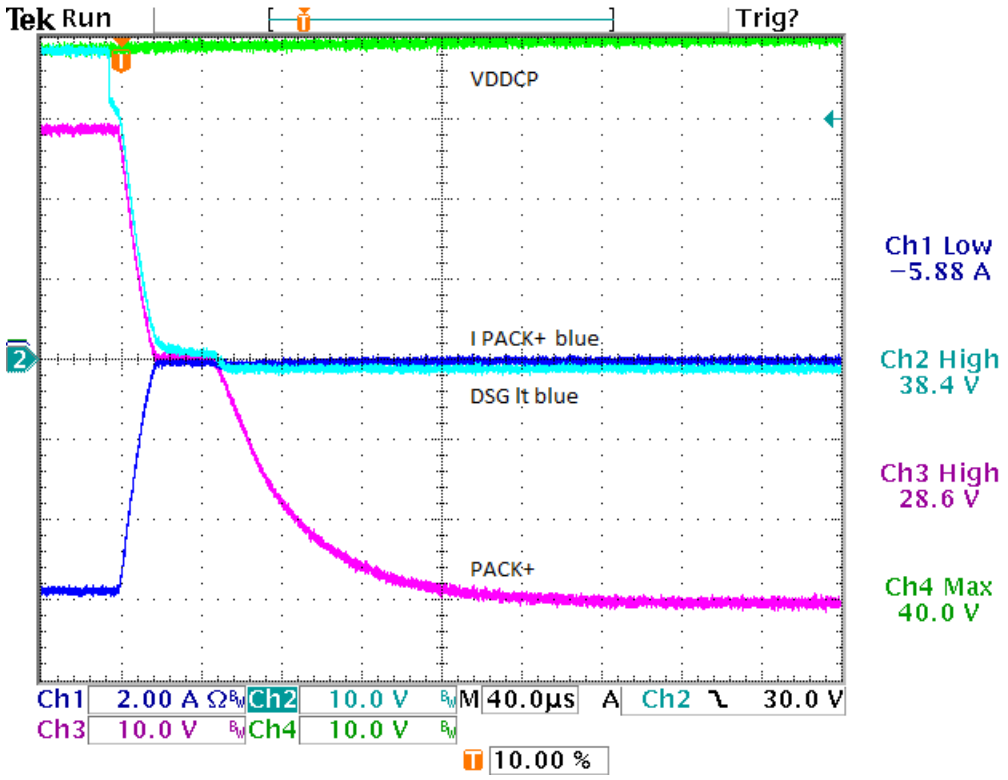

Figure 9. Discharge Disable With Reverse Voltage

4 Summary

With low voltage systems, a single FET may be used to clamp the discharge FET off during reverse voltage. With higher voltage, however, the power dissipation in the connecting components becomes large and additional circuitry is needed to keep dissipation to a reasonable level. The circuit techniques presented in this application report are useful to implement a reverse voltage circuit when components are sized appropriately for the system design.

5 References

For additional information, see the following documents available at www.ti.com.

- *bq76200: High Voltage Battery Pack Front-End Charge/Discharge High-Side NFET Driver* (SLUSC16)
- bq76200 EVM User's Guide (SLVU926)

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