Application Report
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bq76200 Beyond the Simple Application Schematic

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BMS: Monitoring and Protection

ABSTRACT

The bq76200 high-side N-channel FET driver is a highly-integrated solution to control FETs in a battery management circuit. The simple circuit in the data sheet can be effective in many applications, but the user may encounter situations where the device does not appear to switch as expected or unexpected damage occurs. This document describes the switching operation of the bq76200 and shows how external components may affect the operation of the circuit. This information can help the designer successfully implement battery switches beyond the bq76200 simple schematic.

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1 Introduction

The bq76200 high-side N-channel FET driver was designed for low component count to provide a simple implementation. The part utilizes a charge pump to provide the voltage above the battery to operate the CHG and DSG drivers for the high-side FETs. The drivers include internal resistance to limit the switching time of the FETs. Level shifters are provided from the logic level inputs. A driver is provided for a P-channel pre-charge FET referenced to the higher of BAT or PACK. The charge-pump reservoir capacitor is external and easily scaled for larger loads. Two resistors are used on the pack divider pin to drop the voltage to a level for an ADC in an MCU. So in a best case implementation, only 3 passive parts would be required in addition to the FET circuitry for basic operation. However, in a removable battery this implementation would leave the PACK pin exposed directly to the outside world and through the FETs the BAT pin would experience the same transients. Electronic designers are accustomed to placing decoupling capacitors at integrated circuit power pins to reduce transients into the component, and an addition of a series resistor will further reduce transients into the IC, so these components are shown in the data sheet simple schematic, Figure 1. See the data sheet (SLUSC16) for additional descriptions and specifications. The application section of the data sheet describes a number of options in use of the part and examples are shown in the application note *FET Configurations for the bq76200 High-Side N-Channel FET Driver* (SLVA729). The bq76200EVM-606 has an implementation with some transient suppression components, test points, FET options and includes series resistors to the FET gates R_{DSG} and R_{CHG}, but values are shown as zero. A better understanding of the IC may be desirable for the designer to determine components applicable to the specific circuit implementation.

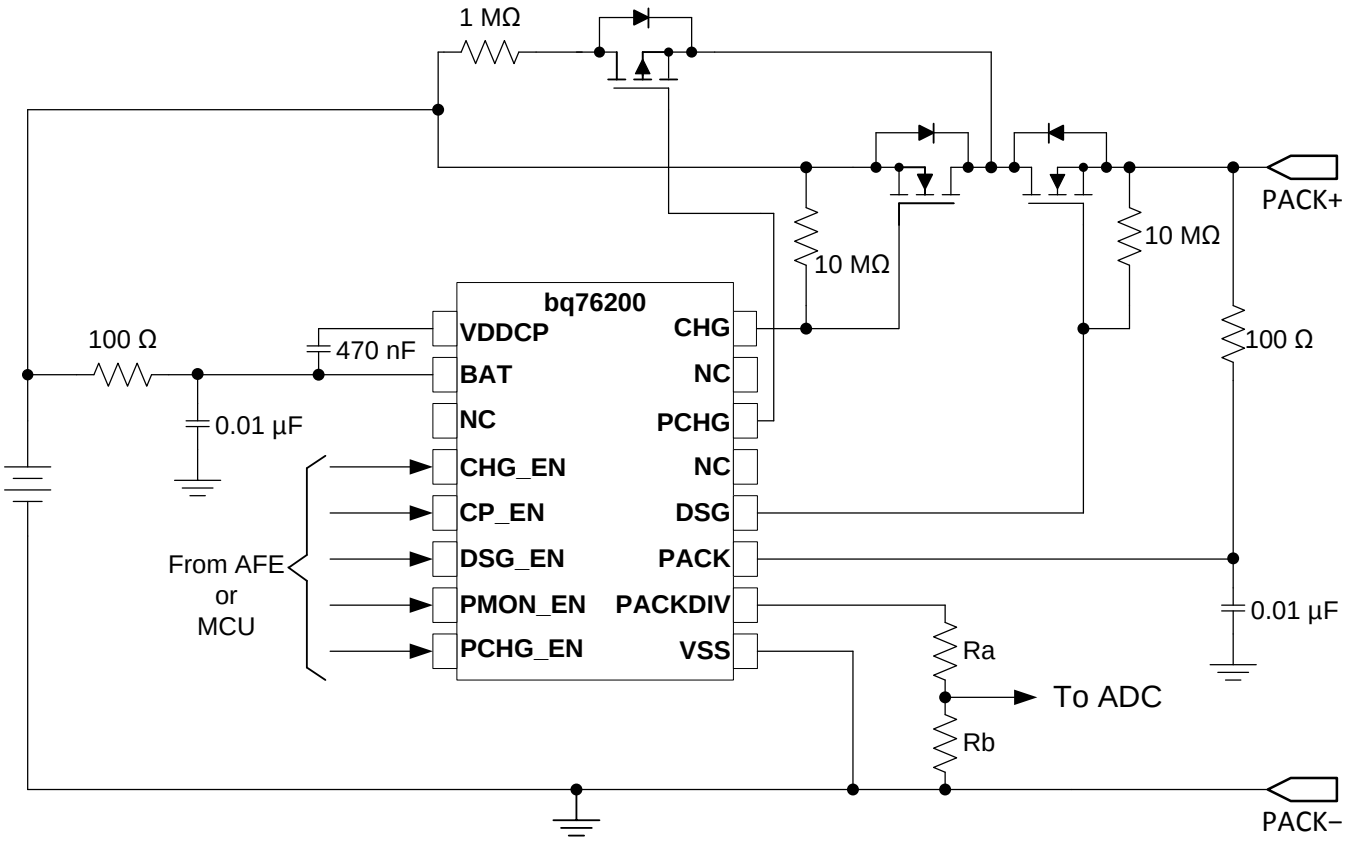

Figure 1. bq76200 Data Sheet Simple Schematic

2 Device Architecture

The bq76200 data sheet block diagram shows internal functions on a basic level. The diagram in Figure 2 shows functional behavior of the switches in the device. Switches are implemented with transistors, the switches shown represent the function. CHG switches to the VDDCP level when on and the BAT pin when off. The DSG pin is also switched to VDDCP when on but to the PACK pin level when off. PCHG is set to the common or higher of the BAT or PACK pin voltage when off and a voltage below when on. PACKDIV is set to the PACK pin voltage when on and allowed to fall when off. The resistors shown in the diagram do not represent specific parameters from the data sheet, but function with the circuitry to give the resistance shown in the data sheet parameters for the listed test condition. The paths are all resistive, so there will be a limit to the current available to turn on and off the FETs.

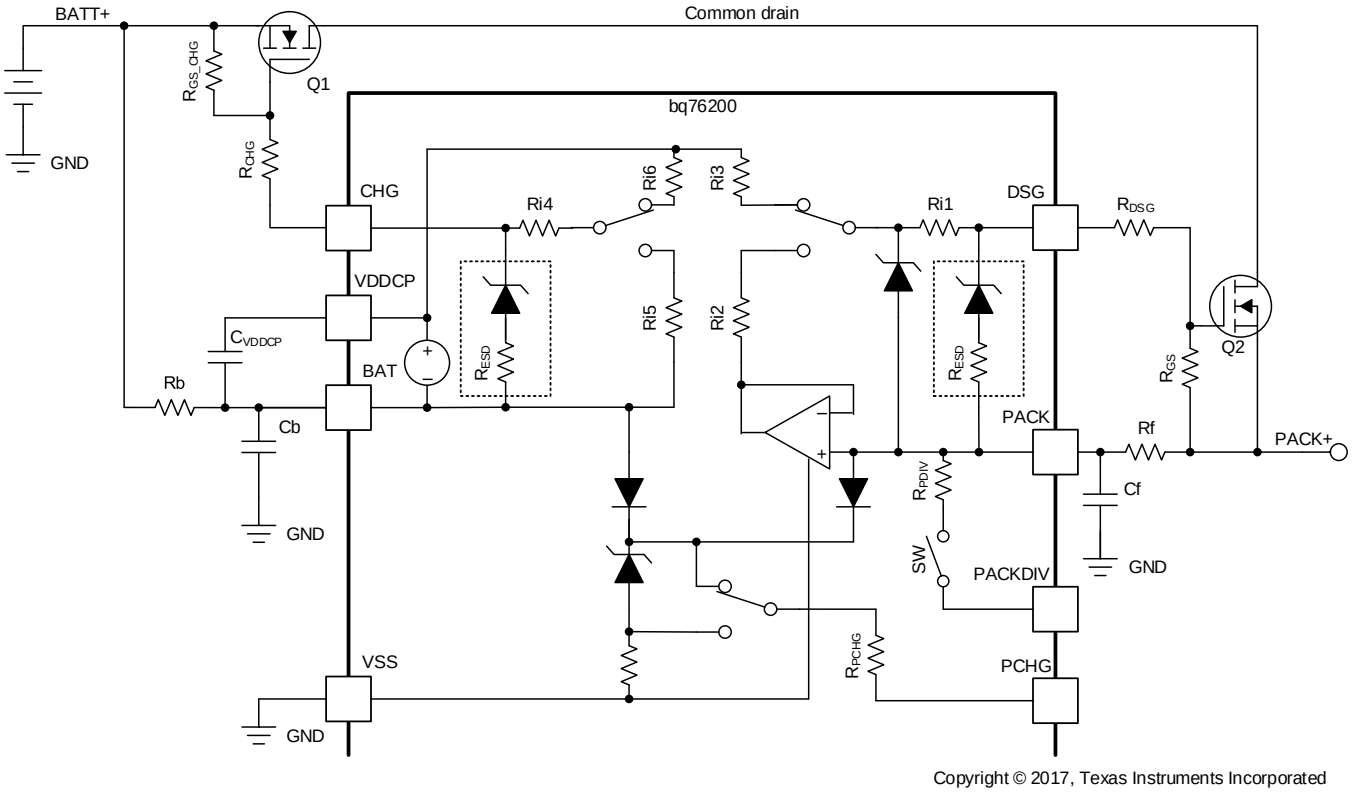

Figure 2. bq76200 Switching Architecture

2.1 Charge Pump

The bq7200 provides the gate voltage for the N-channel FETs above the battery voltage from a charge pump. The charge pump is a low-current design which will run, when required, to maintain the FET drive level. Current is drawn from the BAT pin to power the charge pump which stores charge in the C_{VDDCP} capacitor. When current is needed to switch the CHG or DSG output, that current comes primarily from C_{VDDCP}, while the charge pump runs to maintain the voltage. While the current capability of the charge pump is not listed in the data sheet, using the equation for a capacitor I = C dv / dt, it can be estimated from the parameters. At the 9-V minimum output voltage and a 100-ms startup time, the charge-pump current will be approximately 470 nF × 9 V / 100 ms, or 40 µA. Since the circuit is for use in a battery, the designer should minimize the load on the charge pump, and since the data sheet does not provide a minimum current, the designer should provide a suitable margin for the charge-pump load.

The charge pump operates with 4 thresholds and a delay. When enabled, the charge pump will run and increase the VDDCP voltage to a stop threshold, then turn off to reduce supply current. When the VDDCP voltage falls to a start threshold, the charge pump will start and again raise the VDDCP voltage. The charge pump runs at its fixed current, the rate of its rise and fall will depend on the individual part and operating conditions, but primarily on the size of the capacitor. When the drivers place a load on the charge pump, it will change the rate of the voltage rise and fall. If the load current is more than the charge

pump can provide, the voltage will fall through a UVLO threshold. After a delay, the device will turn off the drivers to avoid damage to the FETs. Once the charge-pump voltage rises above a recovery voltage threshold, the drivers will be re-enabled. If the overload is gone, the charge-pump voltage will continue to rise, if the overload is still present, the voltage will drop again. Figure 3 shows the concept of the 4 thresholds. Figure 4 shows an example of the charge pump with an overloaded CHG driver. When operating normally, current is drawn for the charge pump only to increase the voltage, but when overloaded, current is drawn continuously.

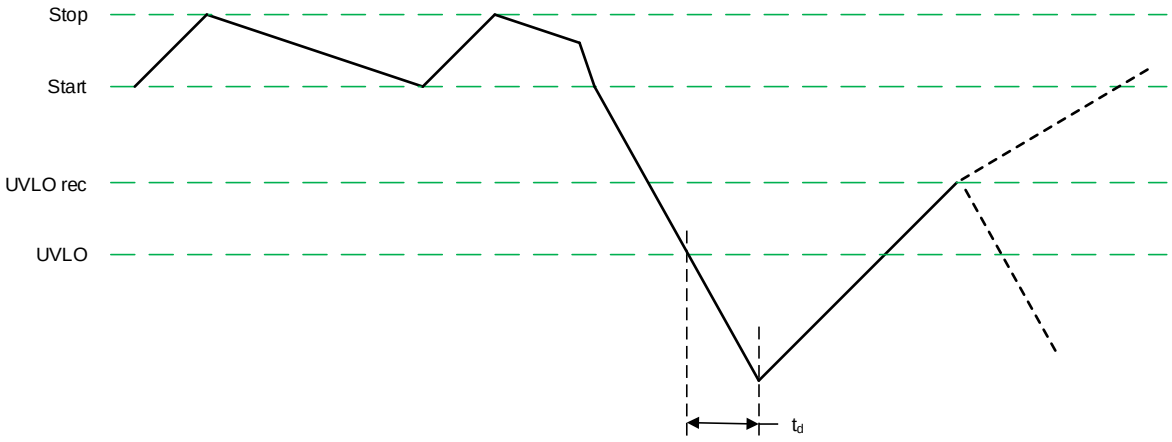

Figure 3. Charge-Pump Thresholds

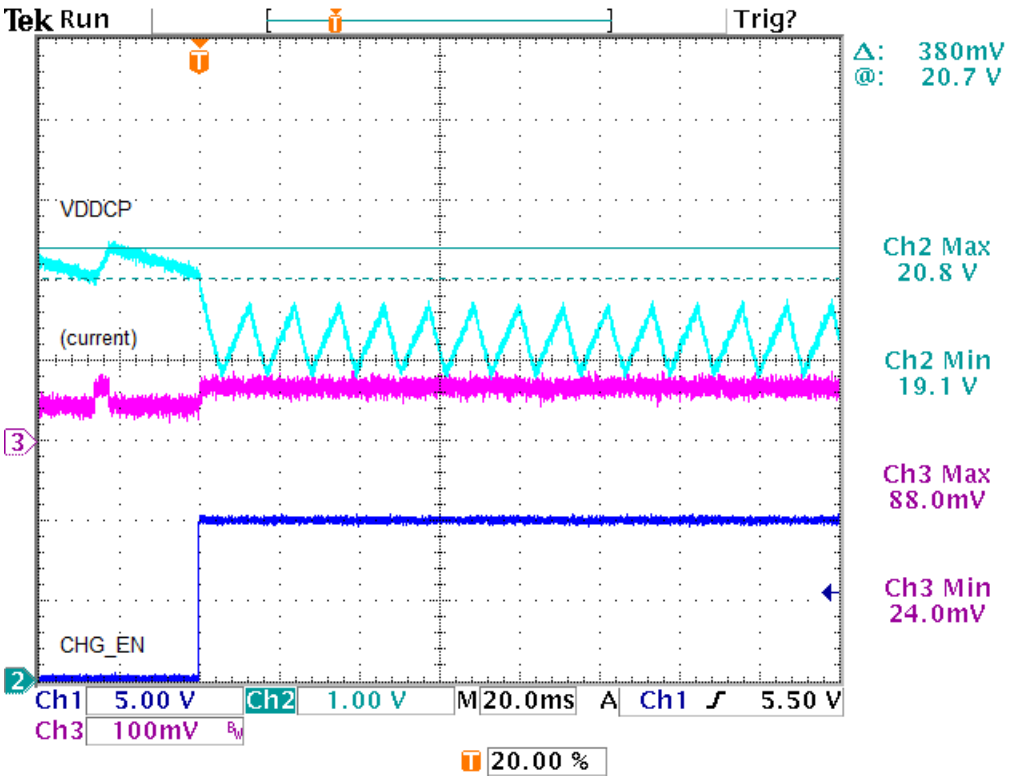

Figure 4. Overloaded Charge-Pump Example

The time for the driver to be on and when it will re-try depends on the amount of overload. Figure 5 shows an example of the DSG driver overloaded. When first enabled, the driver is on longer since VDDCP starts from an operating level between the start and stop thresholds. On the subsequent pulses the driver is on a shorter time since the starting voltage is the lower UVLO recovery threshold. When the overload is significant, such as turning on DSG when PACK cannot rise, the pulse may be very narrow.

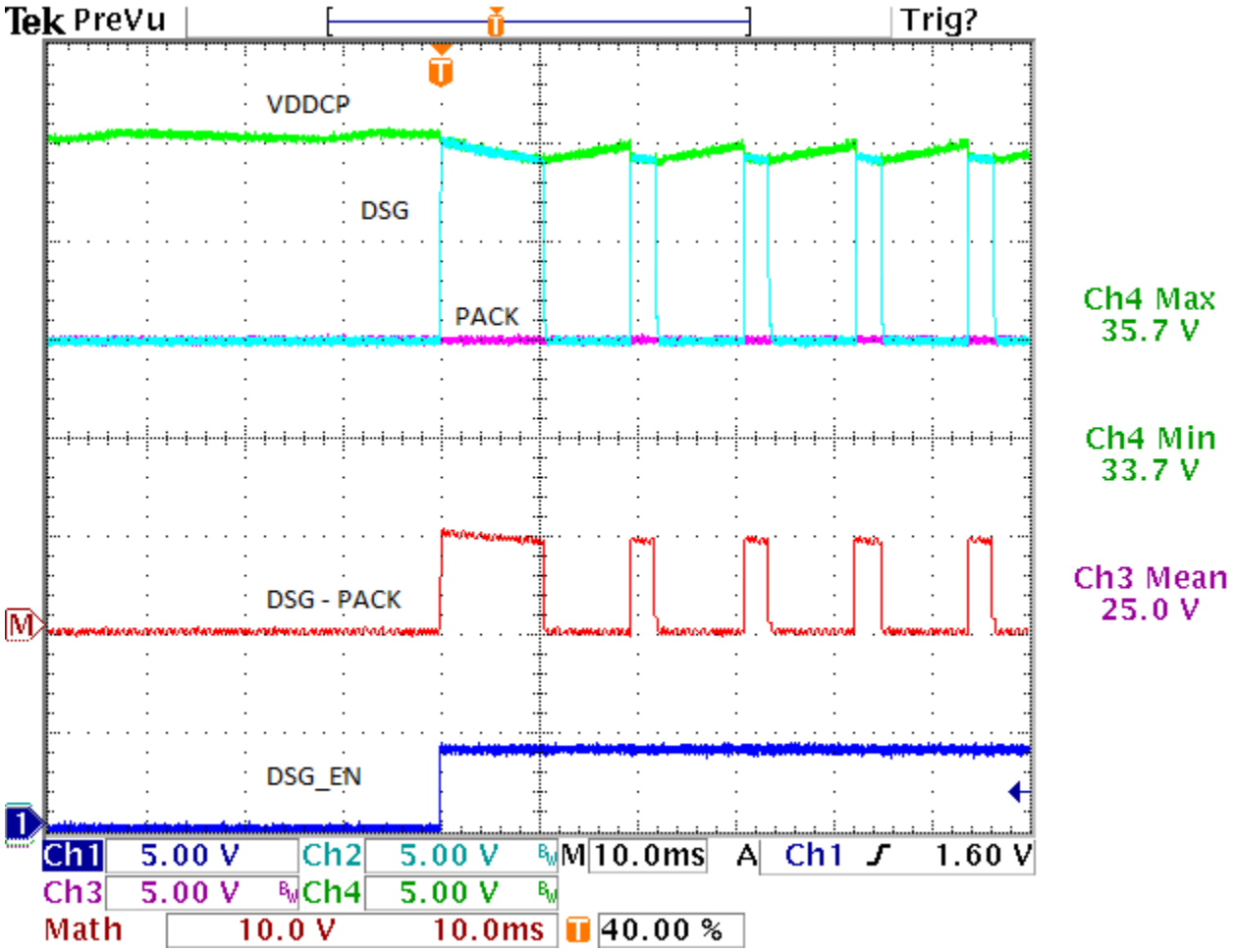

Figure 5. DSG Cycling Example

2.2 N-Channel FET Driver

The bq76200 CHG and DSG outputs are designed for continuous operation of FETs which have a limited gate voltage range. The drivers are resistive as represented in Figure 2 and with the parameters shown in the data sheet. The power is from the VDDCP pin which has a limited supply voltage. In the case of the CHG driver, the high voltage is limited since VDDCP has a limited voltage above the BAT pin, but in the case of the DSG driver, the VDDCP supply could be much larger than the PACK pin. A zener is included in the DSG path with the intent to limit the voltage between the DSG and PACK pins.

Each driver has an ESD cell on the driver output pin which will trigger when the voltage is sufficient to protect the circuitry between the pins. While this circuit is designed to take high current for a very short time, Figure 6 shows an example measurement of the DSG driver when it is on and forced with a DC source to see its characteristic. Below the normal output voltage, the DSG will source some current but cannot be pulled down significantly or it will reach UVLO and turn off. As the voltage rises above normal, the pin begins to push current into the charge pump, then into the internal zener. At approximately 30 V, the ESD cell will trigger and the voltage drops to approximately 14 V. The ESD cell is designed to protect the part from short transients typically in handling and assembly, not for continuous operation in circuit. Although there is no limit in the data sheet for current into the pin, the ESD cell will have a practical current limit above which, it will fail. In this example the pin shorted, but could fail open or with another altered characteristic. A resistance between the FETs and the pins will reduce the current. The maximum current for the part is not characterized or shown in the data sheet, but the designer should limit currents to some reasonable level to avoid damage to the part. One amp peak and continuous currents less than 80 mA may be reasonable, although avoiding ESD trigger from system voltages and significant continuous current in a battery are preferred.

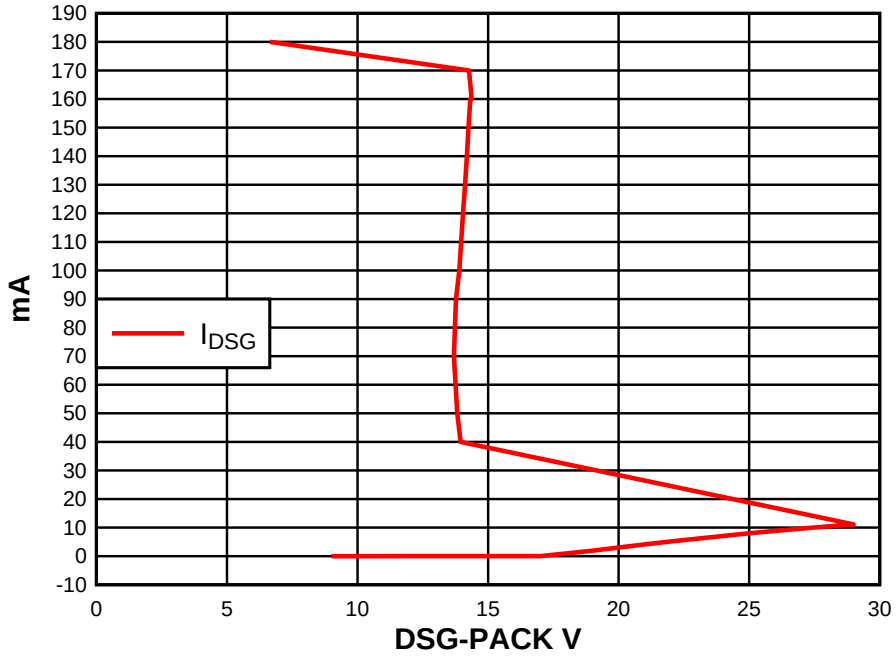

Figure 6. DSG V-I Characteristic

2.3 PCHG and PACK Monitor

While the CHG and DSG outputs are intended for continuous operation, the PCHG and PACKDIV outputs are intended for intermittent operation. PCHG is to drive a P-channel FET with respect to the higher of the BAT or PACK pin. PACKDIV is to allow measurement of the PACK+ voltage through the PACK pin.

Supply currents for the PCHG and PACKDIV function operation are not shown in the data sheet. PCHG may be used to pre-charge a battery at a low rate through a current-limiting resistor. While the driver may be on a long time in this use, the current is from the charger which is viewed as a high-capacity source. When PCHG is used for a pre-discharge function to apply a test current to PACK+ for load detection, it is expected to be on a relatively short time. PACKDIV is expected to be on only long enough to measure the PACK voltage and at a low duty cycle. PCHG drive current will come from either BAT or PACK, the current is approximately 1.5 mA, when regulated. An example of PACK pin current from PCHG is shown in Figure 7. PACK current when PACKDIV is enabled with PMONEN is approximately 3 mA when regulated, Figure 8 shows an example. While the PMONEN supply current to operate the switch is about 3 mA, the current through the switch is recommended to be 500 uA, or less. With both enables active and the maximum recommended load, the current in Rf will be approximately 5 mA resulting in 0.5 V across the 100 Ω recommended Rf. Since the current is relatively constant across the PACK voltage, this creates an offset in the PACK voltage different from the gain of the PDIV resistor divider. So while the contribution to overall pack load from these supply currents may be low due to the source and duty cycle, the pack designer should be aware of these currents when designing the pack and setting the duty cycles. Rf should not be large or a shift in the PACK voltage will occur which can affect the PCHG and PDIV voltages.

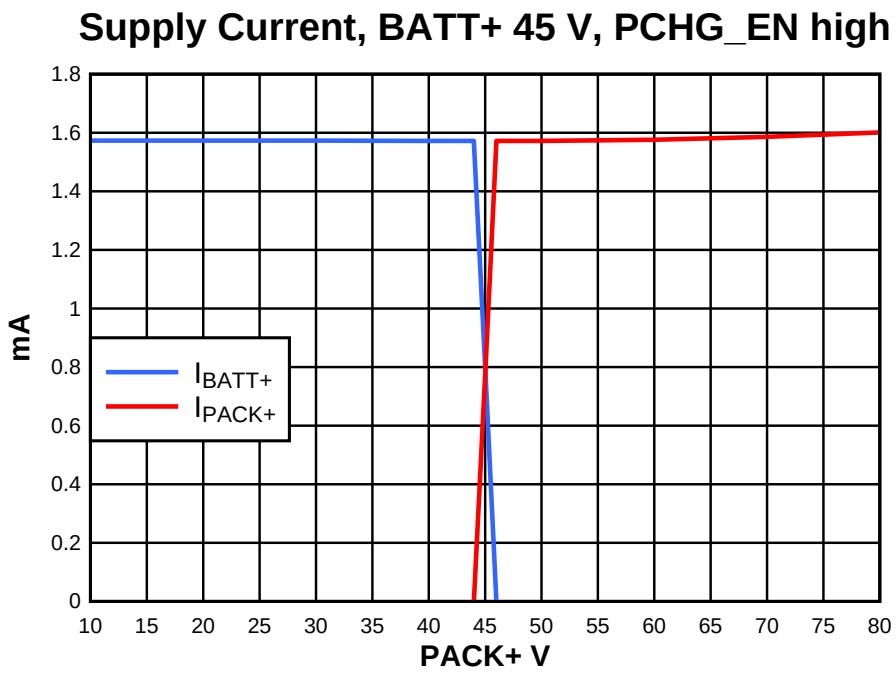

Figure 7. PACK Current From PCHGEN Example

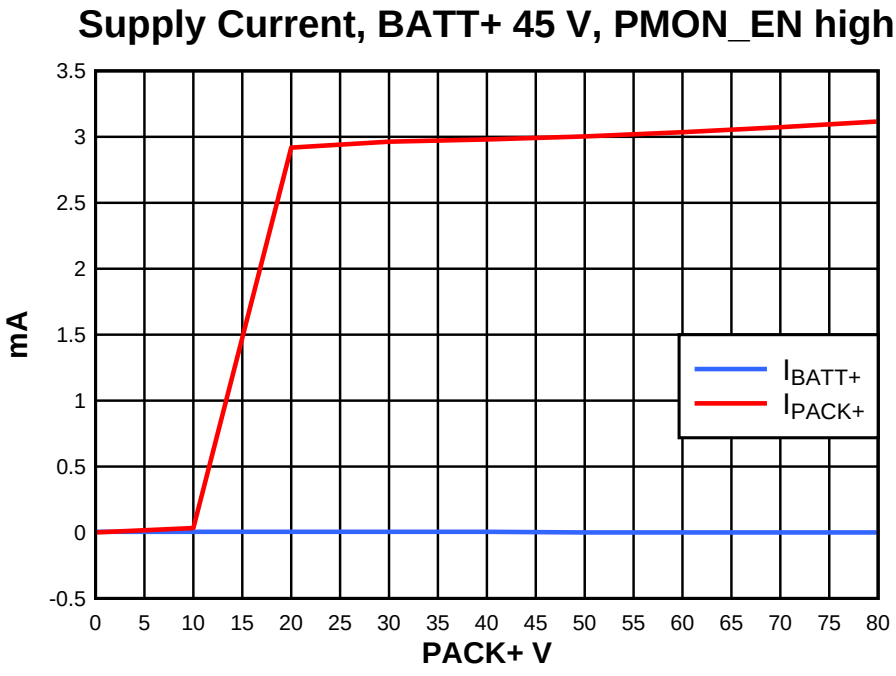

Figure 8. PACK Current From PMONEN Example

3 PACK and BAT Filters

As mentioned in the introduction, the filters on PACK and BAT keep transients out of the IC. The filters should not be arbitrarily large; however, since the PACK and BAT pins are the way the part knows the voltage of the sources of the FETs. The high level of the drivers is set by the BAT pin voltage. When the filter is large, the FET V_{GS} will vary with transients on the PACK. Figure 9 shows an example of the charge FET V_{GS} with a large (1 µF) filter, actual results will vary with the specific design. The PACK pin filter will have effects related to the DSG driver discussed in Section 4.

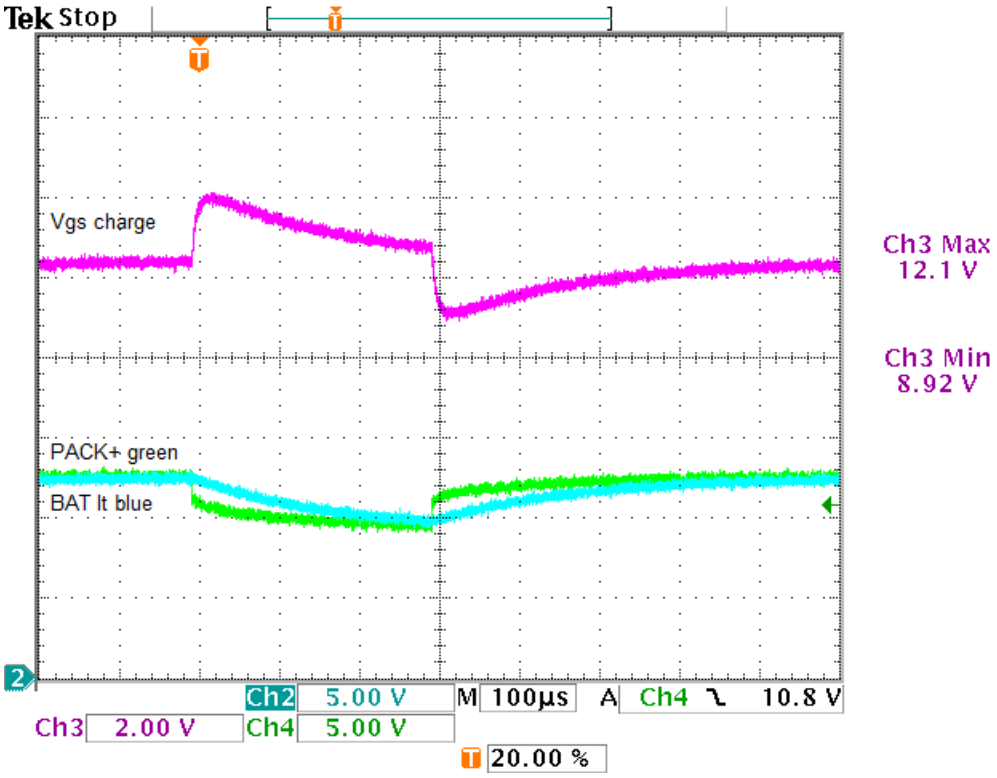

Figure 9. Large BAT Filter Effect

4 DSG Circuit

4.1 DSG Turn On

When turning on the DSG output, it will rise from 0 V to VDDCP. The discharge FET comes on as a source follower or common drain amplifier. Figure 10 shows the circuit relevant to DSG turn on. The currents during turn on will depend on the battery voltage and the external component values. With sufficient voltage, various paths inside the IC may conduct and draw current from the charge-pump capacitor C_{VDDCP}. If the VDDCP is discharged to the UVLO level during switching, the drivers will turn off and the switching will be unsuccessful. Table 1 describes current flow in the circuit during turn on.

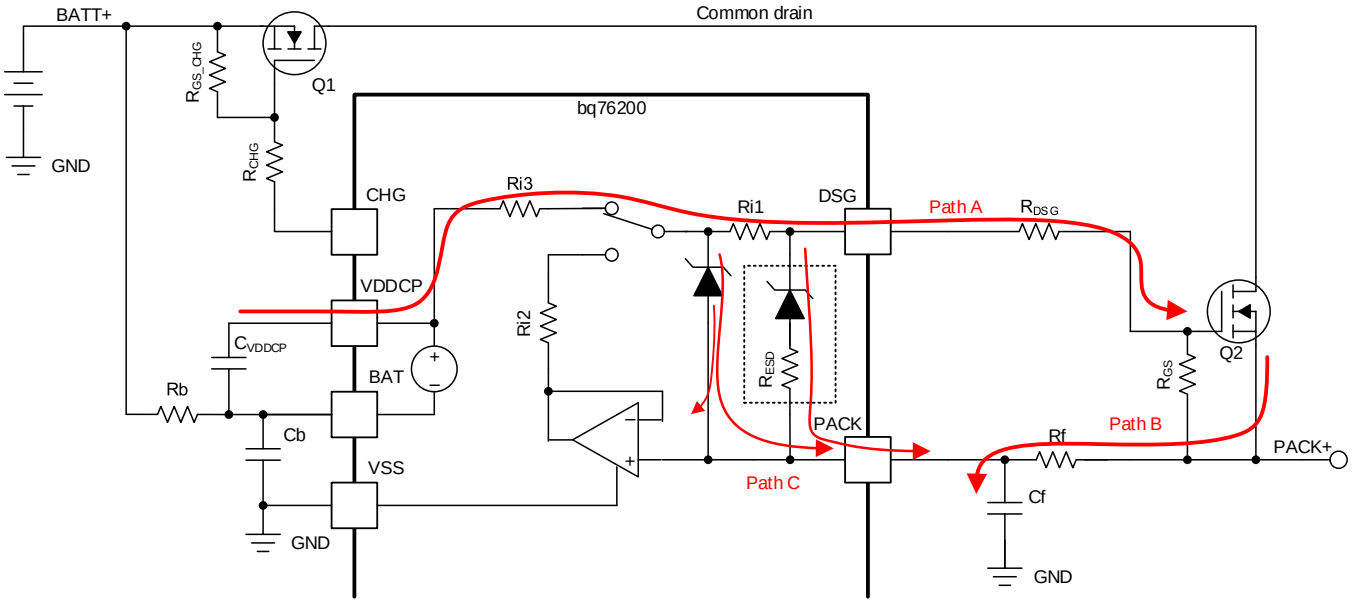

Figure 10. DSG Turn On Current Flow

Table 1. DSG Turn On Current Flow

R_{DSG}	Path A	Path B	Path C	Description
0 or small	Current charges gate and PACK+ rises quickly	Large drop across Rf	Current flows	FET turns on quickly with large drop across Rf and internal switching losses. Cf charges both from PACK+ and internal paths. ESD may trigger. Switching is less successful at higher voltages
100's Ω to few kΩ	Gate charges and PACK+ rises moderately	Small drop across Rf until fast rise of PACK+	Little conduction, but ESD may trigger at high voltages	FET turns on moderately. Cf charges primarily from PACK+. Switching is successful.
Large	Current is small and DSG rises quickly, gate charges slowly	Little current, FET does not turn on	Current flows through internal paths to raise PACK pin voltage	DSG rises quickly with voltage drop across the R_{DSG}. FET is delayed turning on and internal paths conduct discharging C_{VDDCP} into Cf and dropping VDDCP below the UVLO voltage. Switching is not successful, may turn on after several attempts if PACK can pump up.

Figure 11 shows an example of switching DSG with a moderate resistance where the DSG pin voltage initially rises to approximately 13 V. When the FET starts to turn on, the voltage between DSG and PACK starts to rise quickly and the ESD cell triggers. There is a high current out of the FET gate back into the DSG pin and out the PACK pin while the ESD path conducts.

NOTE: Waveform captures in this document show current into pins as positive.

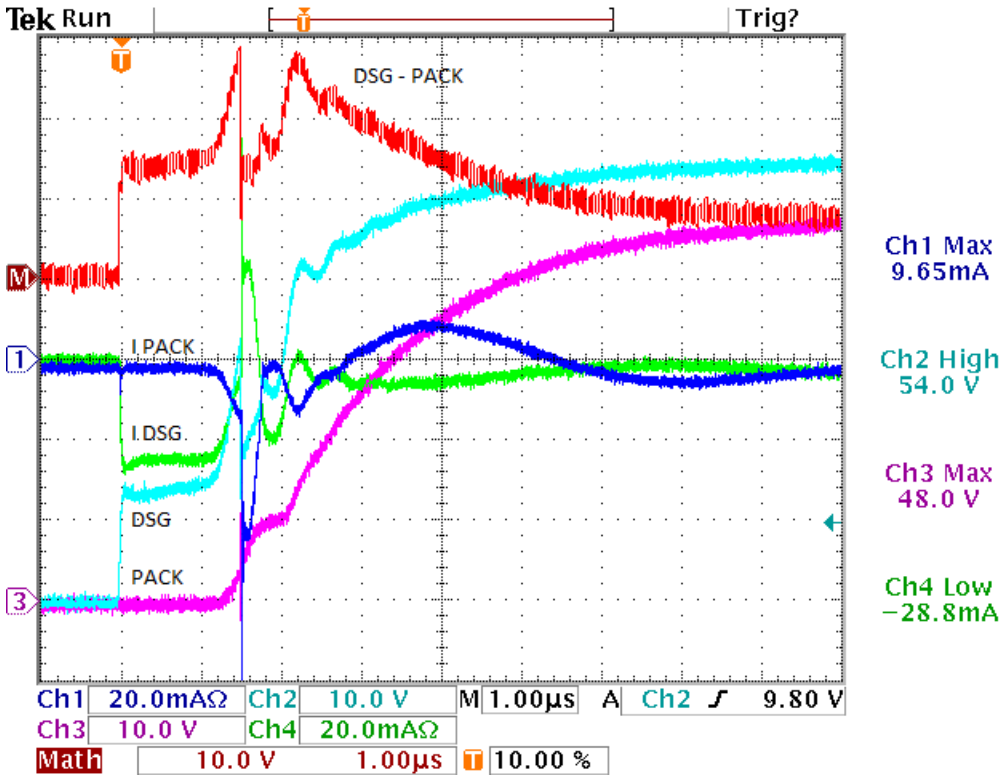

Figure 11. DSG Turn On With ESD Trigger

The amount of charge lost from C_{VDDCP} to internal switching or transferred to the Cf capacitor rather than the FET gate will increase with voltage. At higher voltages the designer may want to increase the size of C_{VDDCP}, but avoiding losses is also desirable. Addition of a zener diode with series resistor between the DSG and PACK pin as shown in Figure 12 will prevent excess voltage between the pins during DSG turn on and avoid internal switching losses. The Rs resistor avoids direct coupling between the pins during zener conduction which could result in oscillation. The resistor and zener should be selected to allow normal operating voltage while reducing the DSG to PACK voltage to approximately 20 V during switching and less than 25 V to avoid the ESD trigger. Figure 13 shows an example turn on with a 100 Ω Rs, an 18 V D1 and 510 Ω R_{DSG}. A smaller Cf will also reduce the potential for charge-pump current into the filter capacitor.

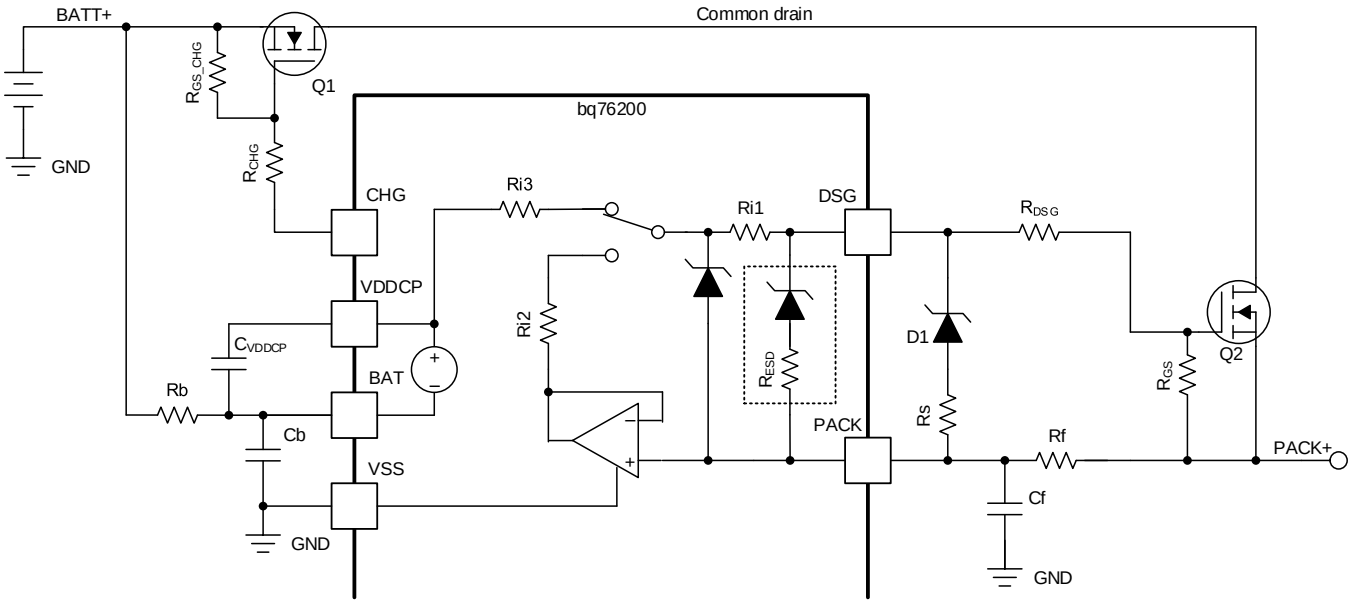

Figure 12. Resistor and Zener to Reduce DSG Switching Loss

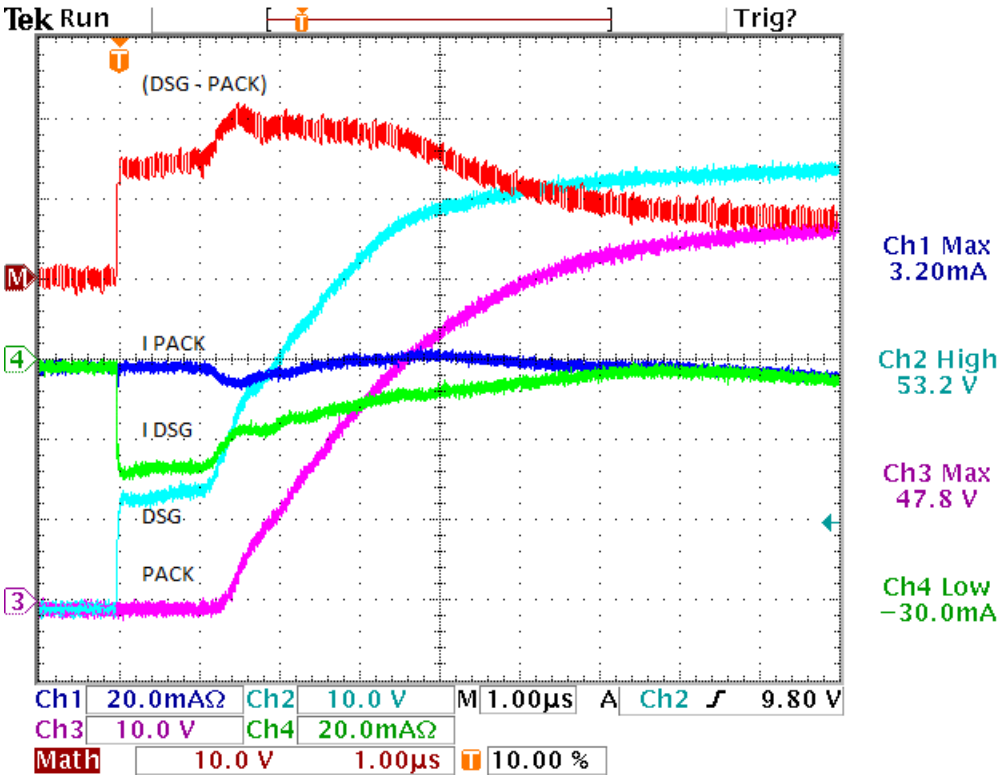

Figure 13. DSG Turn On With Resistor and Zener

4.2 Protecting the FET Gate and DSG Pin

While the discharge MOSFET is operating as a source follower during turn on, the gate may rise very quickly with respect to the source, particularly if the source is held down by a heavy load. When a charge voltage is applied to the PACK+ with the DSG off, the voltage will distribute across R_{GS} and R_{DSG} to the DSG pin which can cause a large negative V_{GS} on the discharge FET. The designer may expect large transients in their design, have observed a transient during test, or have been cautioned by their FET supplier about the turn on speed of the MOSFET. A zener diode may be desired between the gate and source to protect the FET V_{GS} from excessive voltage as shown in Figure 14. The zener voltage is normally selected between the normal operating voltage and the maximum level of the FET, 16 V may be a common value. Remember that a zener diode is rated at a test current and will conduct at a lower voltage. Although the zener diode will limit the positive voltage to the FET gate, it will also provide a path for current into the DSG pin node. If R_{DSG} is zero, current could be almost unlimited. As described in Section 2.2, while the data sheet does not have an absolute maximum current for the DSG pin, the part will have a limit and can be damaged by excessive current. Selecting an R_{DSG} value to limit the current to a safe limit is recommended. A back-to-back zener will allow more voltage swing on the FET source before pushing current into the driver circuit, but may be uncommon due to the added component.

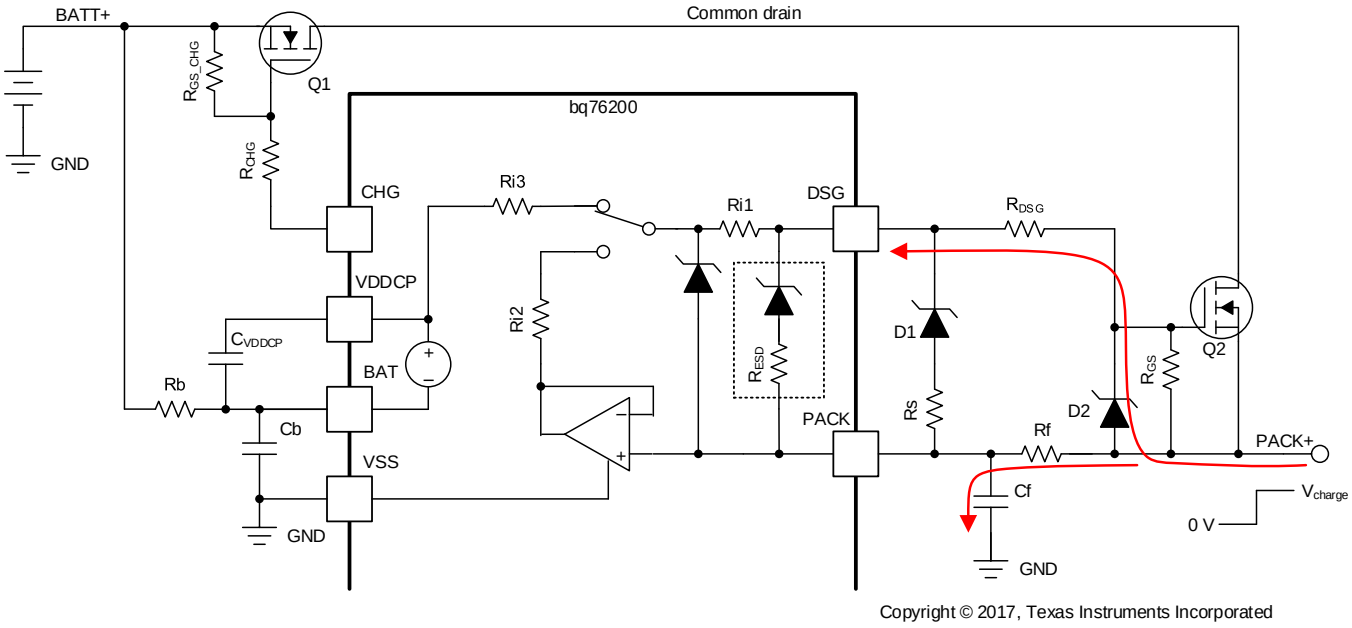

Figure 14. Zener Protection for DSG FET Gate

4.3 DSG Turn Off

Turning off the discharge FET has 2 phases, first is the turn off of the FET, second is the drop of the PACK+ voltage to PACK–. The relevant paths for turn off of the discharge FET are shown in Figure 15. Table 2 summarizes the current flow in the 2 phases.

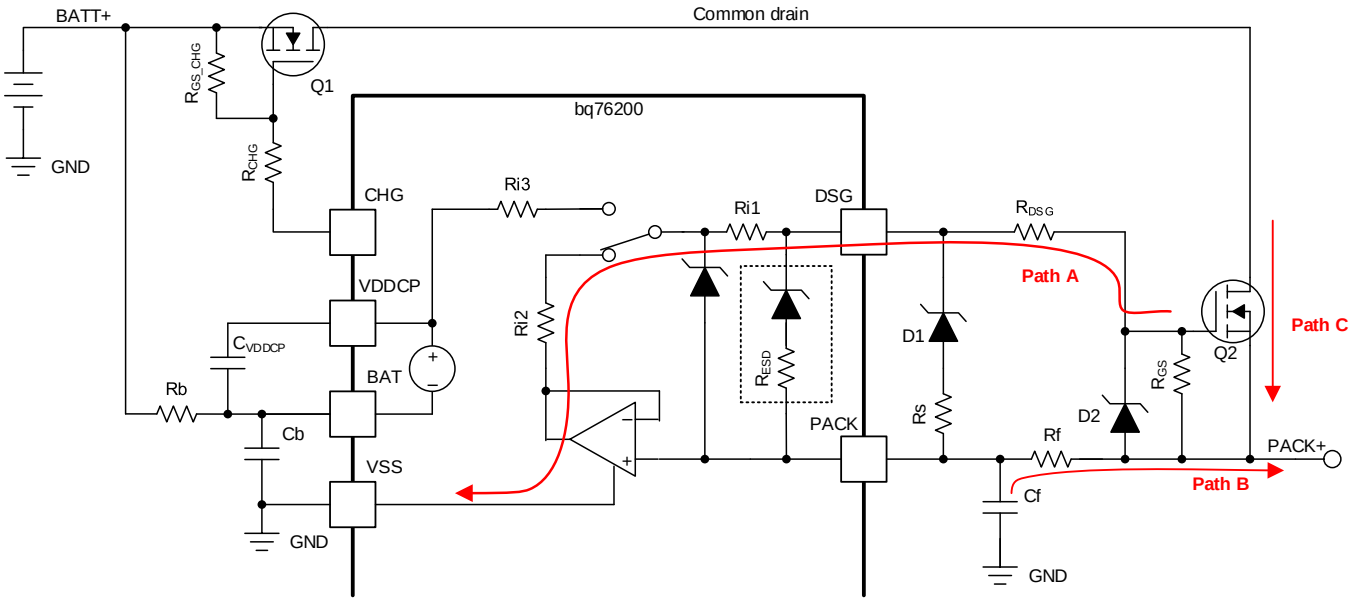

Figure 15. DSG Turn Off Current Paths

Table 2. DSG Turn Off Phases

Phase	Path A (Gate)	Path B (PACK Filter)	Path C (FET D-S)	Description
Discharge FET turn off	DSG sinks current to GND referenced to the PACK voltage	No current	Discharge current stops	FET turns off as gate voltage is pulled below V_{GSth}
PACK+ voltage fall	DSG is held near PACK pin voltage	Cf discharges through Rf as a constant current source	Discharge current is stopped but may resume if PACK pin capacitance does not discharge	Load current discharges PACK+ capacitance and PACK filter

Figure 16 shows an example turn off of the 2 phases. At first the DSG pin voltage pulls down the gate voltage. The FET current drops. When the FET is off, the PACK+ voltage begins to fall as the load discharges any load or PACK+ capacitance and the PACK filter. During the PACK+ fall the FET limits the voltage between gate and source which limits the voltage across Rf and the discharge rate of the Cf capacitor. The DSG pin continues to sink gate current to ground, the voltage is adjusted down to approximate the PACK pin. The circuit acts as a constant current source and if prolonged by a large filter time constant the discharge current can build again as the discharge FET operates as a source follower. Figure 17 shows an example of a larger-than-recommended Cf. The PACK pin and net will have some capacitance, so Cf can not be reduced to 0 or Rf made arbitrarily large. Using small Cf and Rf and a discharge FET with a high $V_{GS(th)}$ improves DSG turn off.

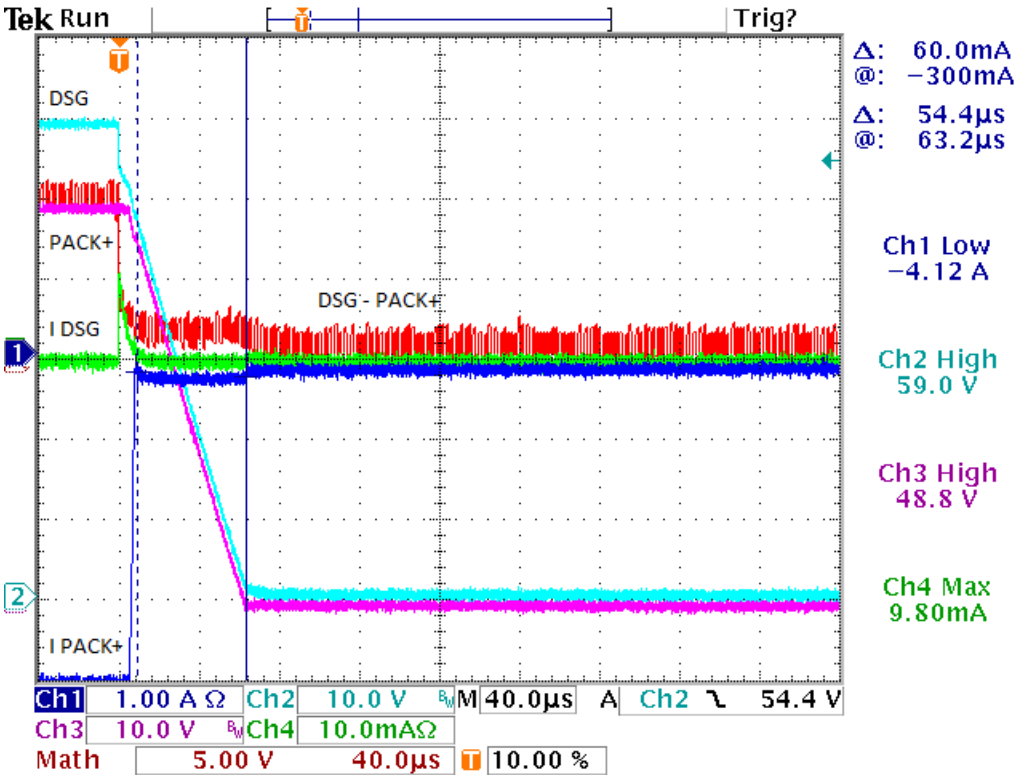

Figure 16. Discharge FET Turn Off Example

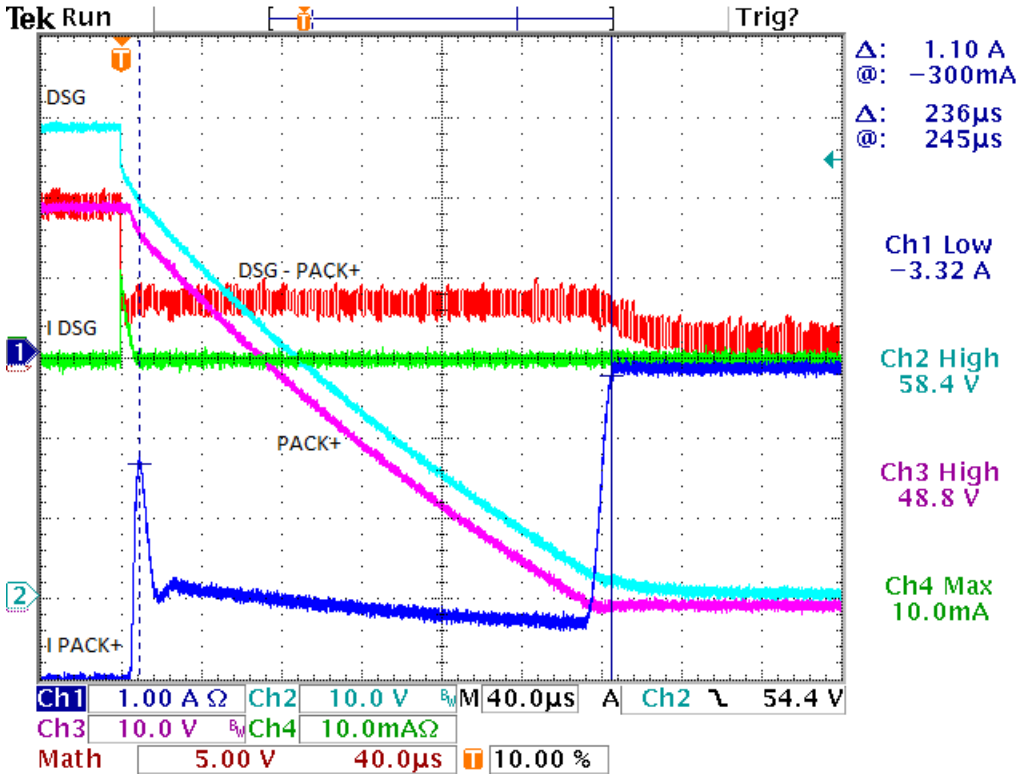

Figure 17. Discharge FET Turn Off With Large Cf

5 CHG Circuit

CHG turn on and off are straightforward with CHG switched between VDDCP and BAT levels. Current for turn on comes from the charge-pump capacitor C_{VDDCP}. At turn off, current is pulled from the CHG pin to the BAT pin. The internal circuit for the CHG pin does contain an ESD structure between the CHG and BAT pins with characteristics similar to the DSG pin, see Figure 18. When connecting the battery during pack assembly, a large step on the BATT+ node will cause the voltage to distribute across the R_{GS_CHG}, R_{CHG}, CHG, and BAT pins. Initially the BAT pin is at zero volts and if the ESD structure triggers, the CHG voltage will be clamped 15 V above the BAT pin and the remaining voltage will distribute across the R_{CHG} and gate resistors. Since the R_{CHG} is small compared to the gate resistor, most of this voltage appears across the gate and could stress the FET gate.

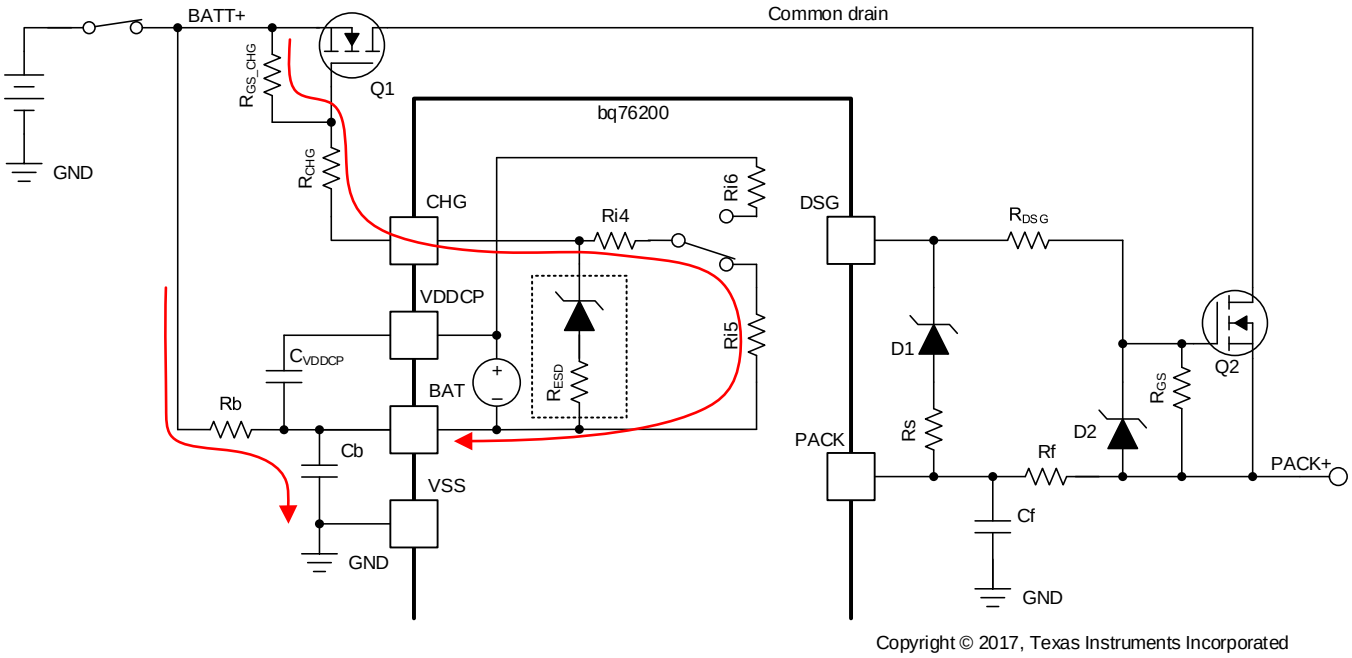

Figure 18. Battery Connection With Basic CHG Circuit

Adding the D3 zener between the gate and source of the charge FET as shown in Figure 19 will prevent the large V_{GS} voltage, but will increase current into the CHG pin. Like the DSG pin, the data sheet does not show a maximum current into the CHG pin, but it can be damaged by too large of a current and a non-zero resistor should be used for R_{CHG}. A resistor and zener between CHG and BAT pins will provide a current path to limit the voltage between the CHG and BAT pins to reduce the internal current and avoid trigger of the ESD cell, but will not prevent ESD trigger unless the series resistance is very small. Since the zener circuit would only be used during assembly, avoiding the components by using a suitable R_{CHG} resistance is preferred. Figure 20 shows an example of battery voltage step with D3, a 510 Ω R_{CHG}, and the standard 100 Ω and 10 nF Rb and Cb pin filter.

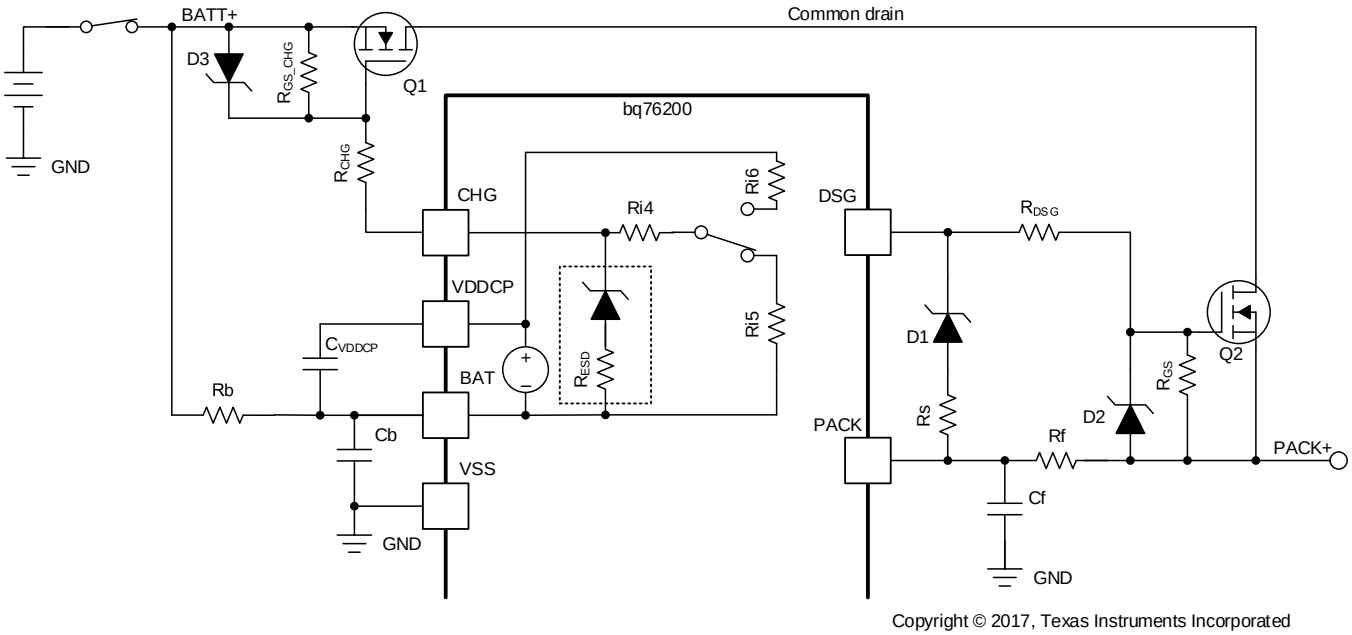

Figure 19. Common External Components With CHG Circuit Gate Protection

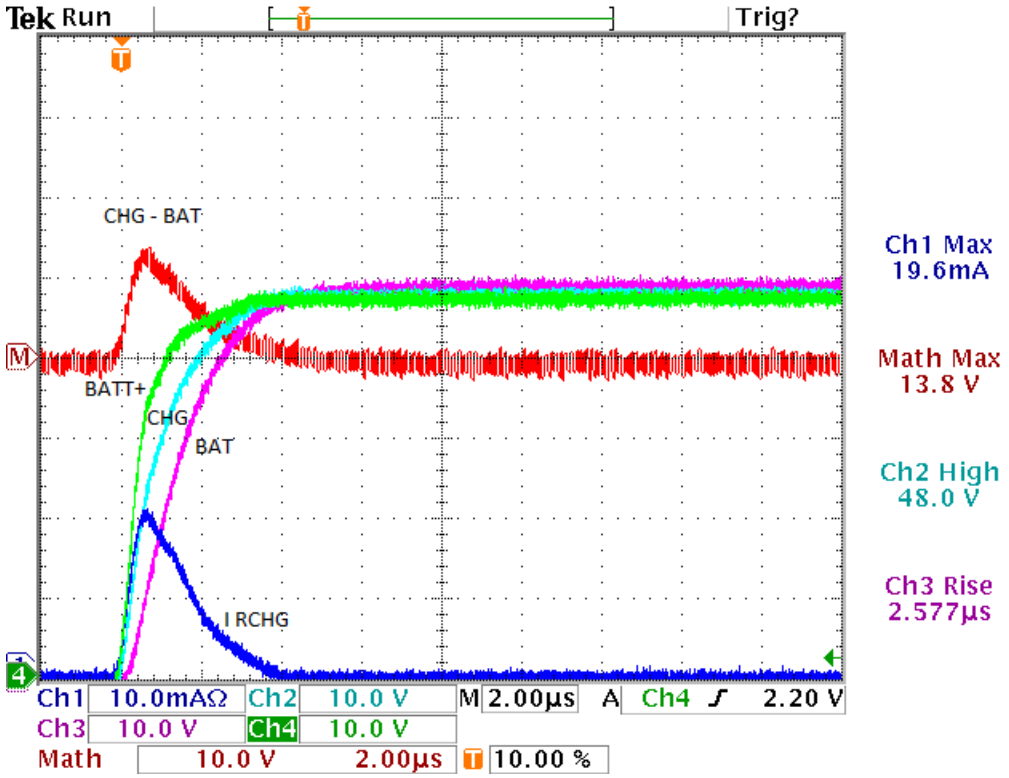

Figure 20. Battery Connection Example With D3, 510 Ω R_{CHG}

6 Summary

Depending on the application, additional components from the bq76200 simple data sheet schematic may be desired. This application report has discussed several operational considerations for using external components. Table 3 summarizes the use of external components included in Figure 19. A designer should select components appropriate for their design and test to confirm proper operation in their environment.

Table 3. External Component Description

Reference Designator	Common Values	Description
C_{VDDCP}	470 nF, or larger	Charge-pump capacitor, scale for the load, see the data sheet and FET configurations application report (SLVA729).
R_{GS} and R_{GS_CHG}	10 MΩ	Gate-source resistor to keep the power FETs off when not powered. Use a large value to reduce charge-pump load.
Cf	10 nF	PACK pin filter capacitor. A smaller value makes DSG turn off easier, a larger value can decrease success of DSG turn on and extend current at DSG turn off.
Rf	100 Ω	PACK pin filter resistor. Provides a 1-µs time constant with the standard 10 nF Cf. Should not be larger when using PDIV or PCHG to avoid voltage drop. Large values can also slow DSG turn off.
D1 and Rs	18 V and 100 Ω	Current-limiting clamp to avoid internal switching losses including ESD trigger during DSG turn on at higher voltages. Does not prevent ESD trigger from external transients.
D2	16 V	Zener diode to prevent transients from exceeding V_{GS} limits of the discharge FET during turn on or charger connection. Creates a path for pushing current into the DSG pin.
R_{DSG}	100 Ω to few kΩ	Resistance influences turn on and turn off of the discharge FET. An optimum value avoids conduction of the zener paths during turn on. Also limits current into the DSG pin from a positive transient on the PACK+ net.

Table 3. External Component Description (continued)

Reference Designator	Common Values	Description
Cb	10 nF	BAT pin bypass and filter capacitor
Rb	100 Ω	BAT pin filter resistor. Provides a 1-µs time constant with the standard 10 nF Cb.
D3	16 V	Zener diode to prevent transients from exceeding V_{GS} limits of the charge FET during pack assembly (cell connection) or large battery transients. Creates a path for pushing current into the CHG pin.
R_{CHG}	100 Ω to few kΩ	Resistance influences turn on and turn off of the charge FET. Switching is typically less critical than discharge FET due to the lower charge current. Select a value to keep the CHG pin current low during assembly and transients.

7 References

For additional information, refer to the following documents available at www.ti.com:

- *bq76200 High Voltage Battery Pack Front-End Charge/Discharge High-Side NFET Driver* data sheet (SLUSC16)
- *bq76200EVM User's Guide* (SLVU926)
- *FET Configurations for the bq76200 High-Side N-Channel FET Driver* (SLVA729)

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