Gate Drive Outputs on the UCC28950 and UCC28951-Q1 During Burst Mode Operation

Application Report

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ABSTRACT

The UCC28950/UCC28951-Q1 phase-shifted full-bridge controllers offer several features to improve power conversion efficiency at light loads. In particular, as the load current drops below the DCM threshold the duty cycle applied to the transformer reduces and eventually the device enters a burst mode. This application note describes how a user can design their gate driver circuits to operate correctly in burst mode.

1 Introduction

Narrow pulse widths (less than 50% duty cycle) may be observed in the first OUTD pulse of a burst and at start-up.

NOTE: The greyed out area in Figure 1 is not ensured.

Typical examples of this behavior are shown in Figure 2 through Figure 5. The initial OUTD pulse (blue) is sometimes full width but sometimes very narrow. The T_{ON} pulse (the OUTA/OUTD overlap time) is unaffected. This means that if the design uses a gate drive transformer, then the correct gate drive is always applied to the switches in the H bridge.

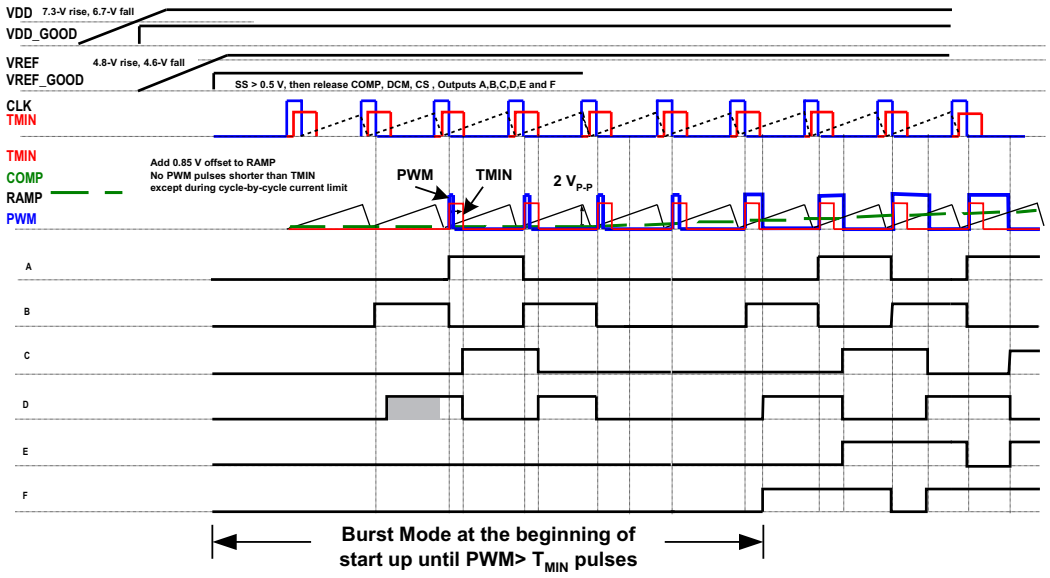

Figure 1. UCC28950/UCC28951-Q1 Startup and Burst Mode Timing Diagram (The Area in Grey is Not Ensured)

2 Gate-Drive Testing

If the designer wishes to use a gate drive device, such as the UCC27714, then some additional testing must be done to make sure that the bootstrap capacitor (C_{BOOT} in Figure 6) is fully charged by the short OUTD pulse. If this is not done, then the next OUTC pulse may not be delivered to the gate of QC. If this happens, QC will not be turned on and current will flow through its body diode instead of its channel. At the start of the next T_{ON} interval QD is turned on again. The resulting reverse recovery current in the body diode of QC can appear as a shoot through current and QC and QD may fail short.

2.1 Typical Waveforms of a Gate-Drive Device

Yellow = OUTA, red = transformer primary, blue = OUTD

Figure 2.

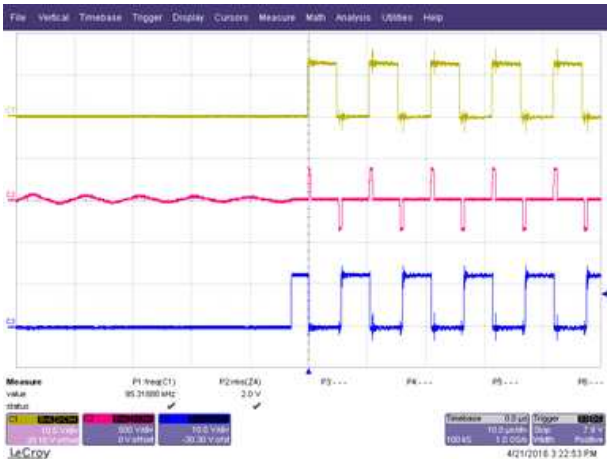

Figure 3.

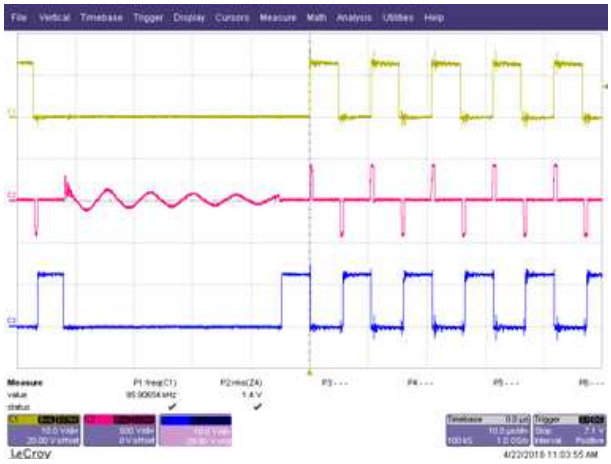

Figure 4.

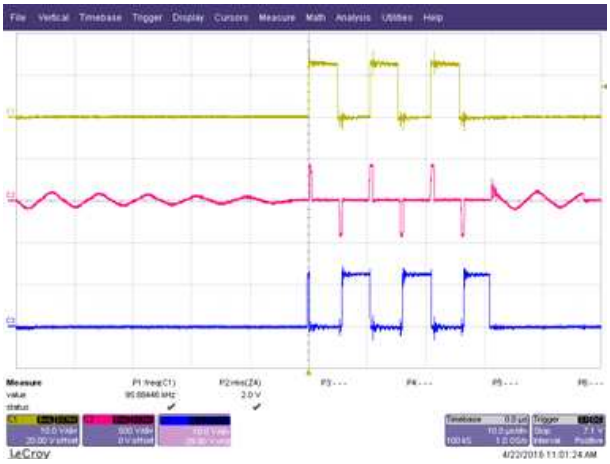

Figure 5.

3 Design Recommendations

A successful gate-driver design requires that the designer follow a few rules.

- Keep R_{CHG} small.
- D_{CHG} must have a high-peak current capacity.
- • Use $CV_{CC} \geq 10 \times C_{BOOT}$. Cboot should be chosen so that $Q_{BOOT} \geq 10 \times Qg$.
- Optimize the layout to minimize parasitic impedances in the charging paths outlined in red in Figure 6.

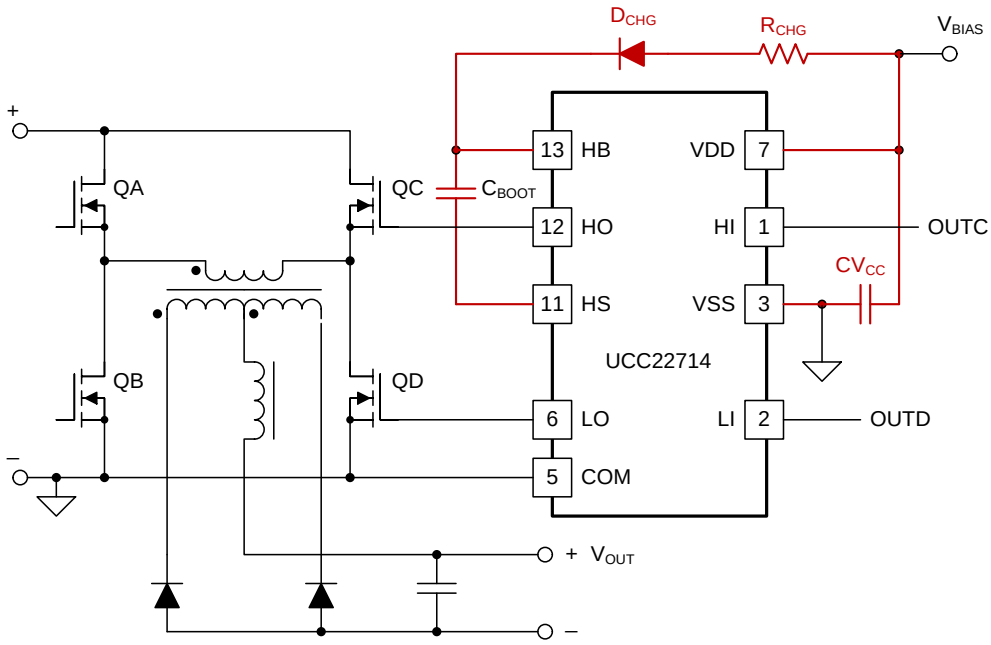

Figure 6. Simplified Gate Driver Schematic

4 Conclusion

The UCC28950 and UCC28951-Q1 offer a burst mode of operation which may be used to improve power conversion efficiency at light loads. To successfully use a device-based gate-driver circuit the designer must pay careful attention to the design of the bootstrap capacitor charging networks.

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