

# Evaluating UCD3138 in Interleave PFC or Bridgeless PFC Configurations using UCD3138PFCEVM-026

**Application Note** 



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#### 1 Introduction

The default configuration of UCD3138PFCEVM-026 is single phase PFC. It can re-configured to interleave 2-phase PFC or bridgeless PFC by hardware modification and re-configuration of the firmware in the UCD3138 controller.

Warning: the PFC EVM could be damaged if a wrong firmware is downloaded or if the hardware modifications are implemented incorrectly.

#### 2 UCD3138PFCEVM-026 Hardware Modification

Follow the instructions in the schematic below to implement the hardware modification for the desired PFC configuration.

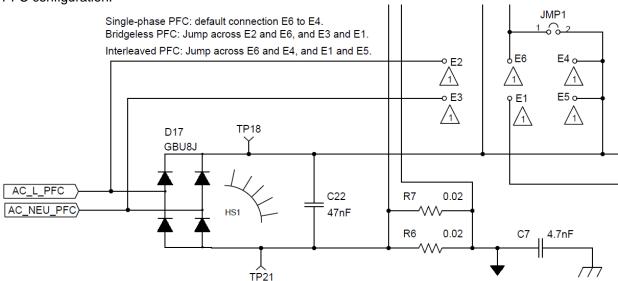


Figure 1: UCD3138PFCEVM-026 Schematic

#### 2.1 2-Phase Interleaved PFC

As shown in the schematic above, simply install a jumper across E6 and E4, and E1 and E5. This is the only hardware modification to implement 2-phase interleave PFC.

## 2.2 Bridgeless PFC

As shown in the schematic above, simply install a jump across E2 and E6, and E3 and E1. This is the only hardware modification to implement bridgeless PFC.

NOTE: Make sure to only have the jumpers installed for a single option at one time. The PFC EVM could be damaged if more jumpers are installed than are necessary for the required topology.



## 3 UCD3138 Firmware Re-configuration in UCD3138PFCEVM-026

Note: Please contact your local TI representative to obtain the firmware source code for reconfiguring UCD3138PFCEVM-026 into Interleaved PFC or Bridgeless PFC.

A compilation flag is used to compile the source code into the different PFC topologies.

#### 3.1 Interleaved PFC

To compile the source code as a 2-phase interleaved PFC:

- □ Open "system\_defines.h"
- □ Define the PFC\_TYPE as **0**, as shown below:

□ Compile the code in Code Composer Studio v3.3

#### 3.2 Bridgeless PFC

To compile the source code as a bridgeless PFC:

- Open "system\_defines.h"
- □ Define the PFC\_TYPE as **2**, as shown below:

//PFC type defines: choose the right type, DO NOT CHNAGE THE VALUES!
//#define PFC\_TYPE 0 //for interleave PFC with shunt sensing
//#define PFC\_TYPE 1 //for single phase PFC with shunt sensing
#define PFC\_TYPE 2 //for bridgeless PFC with CT sensing

□ Compile the code in Code Composer Studio v3.3

For detailed information regarding how to compile the project and download the executable file (.xo) into the UCD3138 device, please refer to the document "Using the UCD3138CC64EVM-030" (Texas Instruments Literature #: SLU886, User guide for the UCD3138CC64EVM-030 EVM). <a href="http://www.ti.com/tool/ucd3138cc64evm-030">http://www.ti.com/tool/ucd3138cc64evm-030</a>



# 4 Experimental Results

For the Figures below, CH1: V<sub>AC</sub>; CH2: I<sub>AC</sub>; CH3:I<sub>L1</sub>; CH4: I<sub>L2</sub>

#### 4.1 Interleave PFC

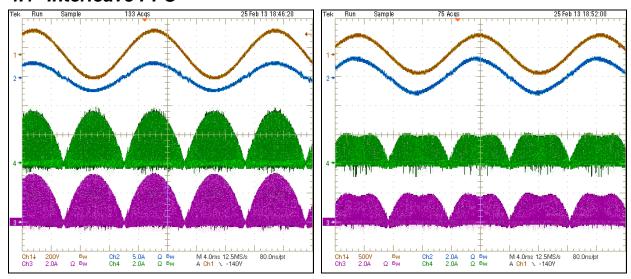


Figure 2: 115VAC, 190W Inductor Currents

Figure 3: 230VAC, 190W Inductor Currents

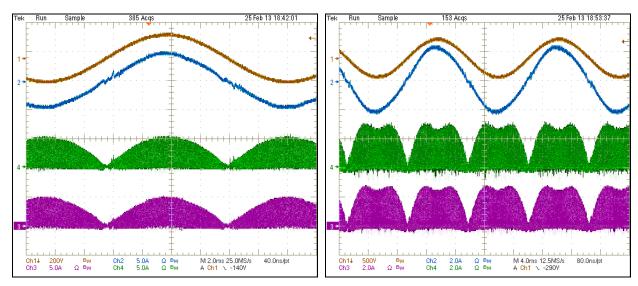
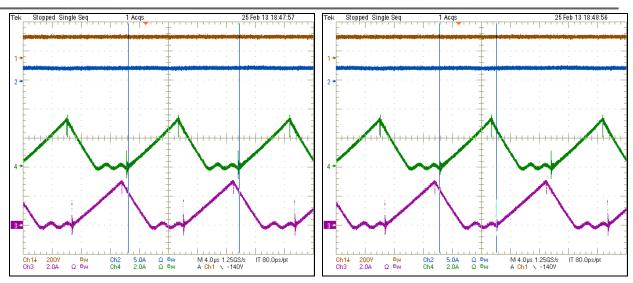


Figure 4: 115VAC, 360W Inductor Currents

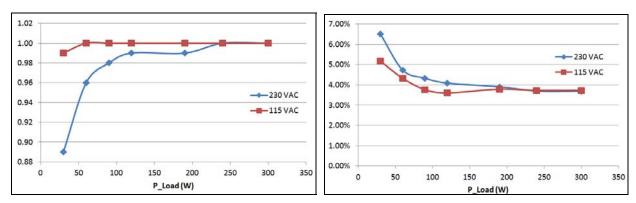
Figure 5: 230VAC, 360W Inductor Currents





**Figure 6: Inductor Currents Switching Frequency** 

Figure 7: Inductor Currents Phase Delay



**Figure 8: Interleaved Power Factor** 

Figure 9: Interleaved THD



# 4.2 Bridgeless PFC

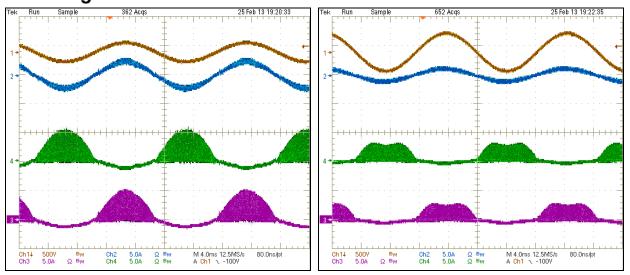


Figure 10: 115VAC, 190W Inductor Currents

Figure 11: 230VAC, 190W Inductor Currents

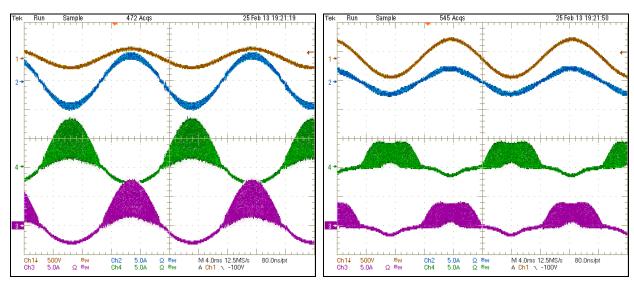


Figure 12: 115VAC, 360W Inductor Currents

6.00% -- 230 VAC 5.00% **■** 115 VAC 4.00% 3.00% 2.00% 1.00% 0.00% 0 50 100 150 200 250 300 350 P\_Load (W)

Figure 13: 230VAC, 360W Inductor Currents

1,02 1.00 0.98 0.96 → 230 VAC 0.94 -115 VAC 0.92 0.90 0.88 0 50 100 150 200 250 300 350 P\_Load (W)

Figure 14: Bridgeless Power Factor

Figure 15: Bridgeless THD



# 5 Theory of Operation

### 5.1 2-Phase Interleave PFC Implementation using UCD3138

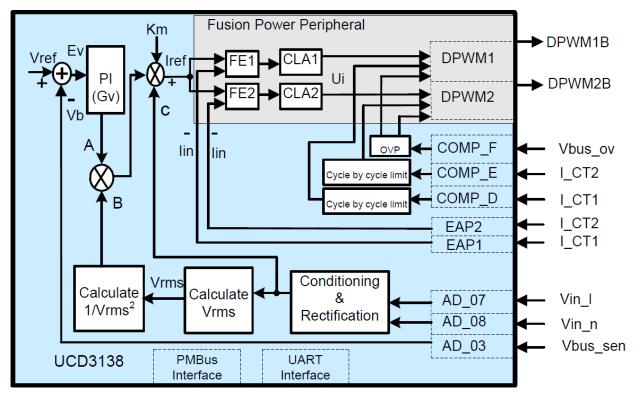


Figure 16: UCD3138 controlled interleaved PFC block diagram

Figure 16 illustrates the block diagram of UCD3138 configured to implement 2-phase interleaved PFC. The input voltage Vin Line and Neutral are sensed separately by two ADC channels AD\_07 and AD\_08. PFC output voltage Vbus\_sen is sensed by another ADC channel AD\_03. In addition, a separate Vout sensing circuit is connect to an on chip analog comparator COMP\_F for over voltage protection (OVP). Two current transformers are used to sense the MOSFETs' instantaneous current and their output I\_CT1 and I\_CT2 are connected to EAP1 and EAP2 respectively for individual current loop control. The two current control loops run independently, each generating a DPWM output to control the respective phase. In addition, I\_CT1 and I\_CT2 are also connected to two on chip analog comparators COMP\_E and COMP\_D for cycle-by-cycle current protection.

An average current mode control is used for input current regulation: current reference is calculated based on Vin, voltage loop output and voltage feed forward. This averaged current reference is then translated to instantaneous signal as if they were sensed at the middle of CT output. The translated reference is then compared to the middle point value of CT output, the error goes through a 2-pole 2-zero digital compensator, a PWM signal is generated based on the compensator output to control the PFC.

It needs to be mentioned here that the above configuration accommodates with TI's PFC evaluation board UCD3138PFCEVM-026. It is not necessary to follow this configuration. For example, I\_CT1/I\_CT2 can be connected to a different EAP channel, different CLAs can be used for current loop compensation, and PFC can be driven by different DPWM outputs also. However, it is recommended using the similar configuration as UCD3138PFCEVM-026, for ease of evaluation.



#### 5.2 Bridgeless PFC Implementation using UCD3138

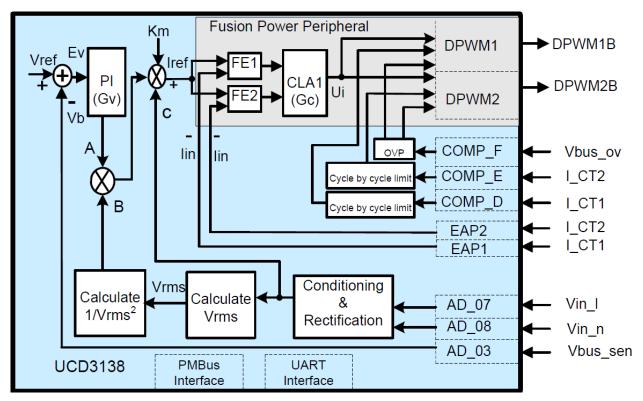


Figure 17: UCD3138 Controlled Bridgeless PFC block diagram

Figure 17 is an example of block diagram of a bridgeless PFC controlled by UCD3138. The input voltage Vin line and neutral are sensed separately by two ADC channels AD\_07 and AD\_08. PFC output voltage Vbus\_sen is sensed by another ADC channel AD\_03. In addition, a separate Vout sensing circuit is connect to an on chip analog comparator COMP\_F for over voltage protection (OVP). Two current transformers are used to sense the MOSFET instantaneous current and their output I\_CT1 and I\_CT2 are connected to EAP1 and EAP2 respectively for current loop control. In addition, I\_CT1 and I\_CT2 are also connected to two on chip analog comparators COMP\_E and COMP\_D for cycle-by-cycle current protection. The control loop generates two PWM outputs DPWM1B and DPWM2B to drive the MOSFETs through gate driver.

An average current mode control is used for input current regulation: current reference is calculated based on Vin, voltage loop output and voltage feed forward. This averaged current reference is then translated to instantaneous signal as if they were sensed at the middle of CT output. The translated reference is then compared to the middle point value of CT output, the error goes through a 2-pole 2-zero digital compensator CLA1, a PWM signal is generated based on the compensator output to control the PFC.

It needs to be mentioned here that the above configuration accommodates with TI's PFC evaluation board UCD3138PFCEVM-026. It is not necessary to follow this configuration. For example, I\_CT1/I\_CT2 can be connected to a different EPA channel, a different CLA can be used for compensation, and PFC can be driven by different DPWM output as well. However, it is recommended using the similar configuration as UCD3138PFCEVM-026, so that most of the UCD3138PFCEVM-026 source code can be reused and the design period can be much shorter.



## 6 References

- 1. UCD3138 Device Datasheet, Lit # SLUSAP2, <a href="http://www.ti.com/lit/gpn/ucd3138">http://www.ti.com/lit/gpn/ucd3138</a>
- 2. Using the UCD3138CC64EVM-030, Lit # SLUU886, http://www.ti.com/litv/pdf/sluu886
- 3. UCD3138 PFC Application, Contact Texas Instruments

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