5W USB Flyback Design Review/Application Report

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Introduction:

In USB and isolated low power converter designs-quasi resonant and discontinuous conduction mode flyback converter topologies are a popular choice, due to their low parts count and relatively low cost. To reduce the cost even further, TI has developed a quasi-resonant/discontinuous current mode flyback controller with primary-side control. This removes the need for optocoupler and TL431 feedback circuitry reducing the cost of these low power designs even more. To achieve relatively low no load input power and regulate the output voltage and output current this device uses a control methodology known as control law. This control methodology uses a combination of primary peak current amplitude modulation (AM) and frequency modulation (FM) to regulate the output current and voltage please refer to the data sheet [1] for details. This application report reviews the design of the 5W adapter, UCC28700EVM-068, evaluation module [2] using the UCC28700 power supply controller. The design calculations are based on typical values. In a production design the values need to be modified for worst case conditions. Also note there is a MathCAD design tool [3] that goes along with this application note to make the power supply design process easier using this device.

Design Specifications:

Description	Minimum	Typical	Maximum	Units
RMS Input Voltage	90 (V_{INMIN})	115/230	265 (V_{INMAX})	V
No Load Input Power			30 (P_{INL})	mW
Output Voltage	4.75	5 (V_{OUT})	5.25	V
Output Voltage Ripple			100 (V_{RIPPLE})	mVpp
Output Load Step (0.1 to 0.6A), (0.6 to 0.1A)	4.1 (V_{OTRM})		6.0	V
Output Current			1(I_{OUT})	A
Switching Frequency			105 (f_{MAX})	kHz
Full Load Efficiency (230/115V RMS input)	73(η)			%

Table 1, Design Specifications

Functional Schematic:

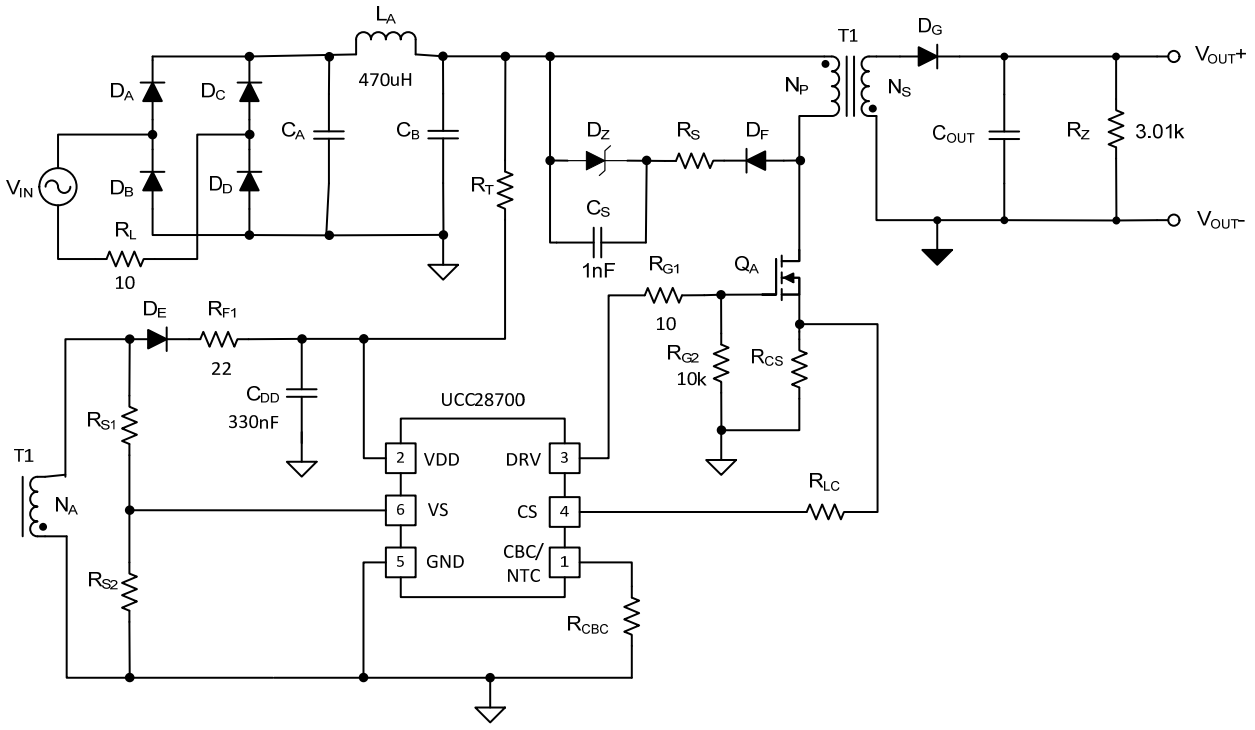

Figure 1, UCC28700 5W Offline Flyback Functional Schematic

Selecting RCB/NTC Resistor:
In this design cable compensation was not used and resistor R8 was not populated.
Please refer to the data sheet on how to setup cable compensation [1].

Initial Power Budget:
To meet the efficiency (η) goal an initial power loss budget (P_{BUDGET}) needs to be set.

$$P_{OUT} = V_{OUT} \times I_{OUT} = 5V \times 1A = 5W$$

$$P_{BUDGET} = \left(\frac{P_{OUT}}{0.74} \right) - P_{OUT} \approx 1.85W$$

Bridge Rectifier Selection (D_A ..D_D):
For this design a 600V, 0.8A, bridge rectifier from Diodes Incorporated was chosen for the bridge rectifier diode (D_A.. D_D), part number HD06.

$V_{FDA} = 1V$, forward voltage drop of bridge rectifier diode (V_{FDA})

$$I_{DA} = \left(\frac{\frac{P_{OUT}}{\eta}}{V_{INMIN} \frac{2}{\pi}\sqrt{2}} \right) = \frac{\frac{5W}{0.74}}{90V \frac{2}{\pi}\sqrt{2}} \approx 85mA$$, bridge rectifier average diode current (I_{DA})

$P_{DA} = V_{FDA} \times I_{DA} = 85mW$, estimate power dissipated in bridge rectifier diode (P_{DA})

Estimate remaining power budget based on bridge rectifier loss.

$P_{BUDGET} = P_{BUDGET} - 2 \times P_{DA} \approx 1.68W$

Transformer Calculations (T1):

Transformer demagnetizing duty cycle (D_{MAG}) is fixed to 42.5% based on the UCC28700 control law methodology [1].

$D_{MAG} = 0.425$

T_R is the estimated period of the LC resonant frequency at the switch node.

$T_R = 2us$

Calculate maximum duty cycle (D_{MAX}):

$$D_{MAX} = 1 - D_{MAG} - f_{MAX} \frac{T_R}{2} = 1 - 0.425 - 105kHz \frac{2\mu s}{2} = 0.47$$

Calculate transformer primary peak current (I_{PPK}) based on a minimum flyback input voltage. This calculation includes a factor of 0.6 to account for the reduction in flyback input voltage caused by the ripple voltage across the input capacitors (C_A and C_B).

$$I_{PPK} = \frac{2 \times P_{OUT}}{\eta \times V_{INMIN} \sqrt{2} \times 0.6 \times D_{MAX}} = \frac{2 \times 5W}{0.74 \times 90V \sqrt{2} \times 0.6 \times 0.47} \approx 382mA$$

Selected primary magnetizing inductance (L_{PM}) based on minimum flyback input voltage, transformer, primary peak current, efficiency and maximum switching frequency (f_{MAX}).

$$L_{PM} = \frac{\frac{2 \times P_{OUT}}{\eta}}{I_{PPK}^2 \times f_{MAX}} = \frac{\frac{2 \times 5W}{0.74}}{(376mA)^2 \times 105kHz} \approx 896uH$$

$V_{QAON} = 2V$, estimated voltage drop across FET during conduction

$V_{RCS} = 0.75V$, voltage drop across current sense resistor

$V_{DG} = 0.6V$, estimated forward voltage drop across output diode

Calculate transformer turns ratio primary to secondary (a_1) based on volt-second balance.
Note in the following equation L_{SM} is secondary magnetizing inductance.

$$a_1 = \frac{N_P}{N_S} = \sqrt{\frac{L_{PM}}{L_{SM}}} = \frac{D_{MAX} \times \left(V_{INMIN}\sqrt{2} \times 0.6 - V_{AON} - V_{RCS}\right)}{D_{MAG} \times \left(V_{OUT} + V_{DG}\right)} \approx 14.5$$

$V_{DDMIN} = 8V$, UCC28700 minimum VDD voltage before UVLO turnoff.

$V_{DE} = 0.3V$, estimated auxiliary diode forward voltage drop

$V_{OUT\_INIT} = 2V$, Minimum voltage on the output when adapter is connected to a device with a depleted battery.

Calculate transformer auxiliary to secondary turns ratio (a_2)

$$a_2 = \frac{N_A}{N_S} = \frac{V_{DDMIN} + V_{DE}}{V_{OUT\_INIT} + V_{DG}} \approx 3.2$$

Transformer primary RMS current (I_{PRMS})

$$I_{PRMS} = I_{PPK}\sqrt{\frac{D_{MAX}}{3}} = 151mA$$

Transformer secondary peak current RMS current (I_{SPK})

$$I_{SPK} = \frac{P_{OUT} \times 2}{V_{OUT} \times D_{MAG}} \approx 4.7A$$

Transformer secondary RMS current (I_{SRMS})

$I_{SRMS} = I_{SPK}\sqrt{\frac{D_{MAG}}{3}} \approx 1.8A$, transformer secondary RMS current

For this design we estimated the power dissipated by the UCC28700 (P_{IC}) would be 50mW maximum. Note this will vary in the design based on the FET that is being driven and the maximum frequency it is being driven at.

$P_{IC} = 50mW$

Calculate auxiliary winding peak current (I_{APK})

$$I_{APK} = \frac{P_{IC} \times 2}{(V_{OUT} + V_{DE}) \times a_2 \times D_{MAG}} = 13mA$$

Calculate auxiliary winding RMS current (I_{ARMS})

$I_{ARMS} = I_{APK}\sqrt{\frac{D_{MAG}}{3}} \approx 5.0mA$

For this transformer we allow for 3% efficiency loss from the transformer (P_{T1})

$P_{T1} = P_{OUT} \times 0.03 = 150mW$

Recalculate remaining power budget

$P_{BUDGET} = P_{BUDGET} - P_{T1} \approx 1.53W$

A Wurth Electronik transformer was designed for this application, part number 750312723, which has the following specifications:

$a_1 = 15.33$

$a_2 = 3.83$

$L_{PM} = 925uH$

$L_{LK} = 16uH$, primary leakage inductance

Input Capacitor Selection ($C_{IN} = C_A + C_B$):

Calculate input capacitor charge time (t_{CH}) based on 40% input capacitor ripple voltage.

$$t_{CH} = \frac{1 - \sin^{-1}\left(\frac{V_{INMIN}\sqrt{2} - V_{INMIN}\sqrt{2}\times 0.6}{V_{INMIN}\sqrt{2}}\right)}{4\times 47Hz} = 3.4ms$$

Calculate flyback average primary current (I_{PT1}) during input capacitor discharge.

$$I_{PT1} = \frac{\frac{P_{OUT}}{\eta\times V_{INMIN}\sqrt{2}} + \frac{P_{OUT}}{\eta\times V_{INMIN}\sqrt{2}\times 0.6}}{2} = 72mA$$

Calculate total input capacitance (C_{IN}) based on minimum flyback input voltage and 40% ripple voltage across the input capacitor.

$T_{RL} = \frac{1}{2\times 47Hz} \approx 11ms$, longest period of the rectified line voltage

$V_{INRIPPLE} = V_{INMIN}\times\sqrt{2}\times 0.4 \approx 50.9V$, input ripple to the flyback converter

$$C_{IN} = \frac{I_{PT1}(T_{RL} - t_{CH})}{V_{INRIPPLE}} \approx 10uF$$

$$C_A = C_B = \frac{C_{IN}}{2} = 5uF$$

Calculate input capacitor (C_A) RMS current (I_{C_ARMS}) based on 40% input capacitor ripple voltage.

$I_{CINP} = \frac{2\times(C_A + C_B)\times V_{INMIN}\sqrt{2}\times 0.4}{t_{CH}} \approx 311mA$, peak input capacitor charge current (I_{CINP})

$$I_{CA\_RMS} = \sqrt{\left(\frac{I_{CINP}}{2}\sqrt{\frac{t_{CH}}{3\times T_{RL}}}\right)^2 + \left(\frac{I_{CINP}}{2}\sqrt{\frac{T_{RL} - t_{CH}}{3\times T_{RL}}}\right)^2 - \left(\frac{I_{PT1}}{2}\right)^2} \approx 82mA$$

Estimate of capacitor C_B's low frequency ($1/T_{RL}$) RMS current (I_{CB_LFRMS})

$$I_{CB\_LFRMS} = I_{CA\_RMS}$$

Estimate of C_B's high frequency RMS current (I_{CB_HFRMS})

$$I_{CB\_HFRMS} = \sqrt{\left(I_{PPK}\sqrt{\frac{D_{MAX}}{3}}\right)^2 - \left(I_{PPK}\frac{D_{MAX}}{2}\right)^2} \approx 122mA$$

Estimate of C_B's total RMS current (I_{CB_RMS})

$$I_{CB\_RMS} = \sqrt{\left(I_{CB\_LFRMS}\right)^2 + \left(I_{CB\_HFRMS}\right)^2} \approx 147mA$$

For this design 4.7uF, 400V electrolytic capacitors, from Nichicon part number UVR2G4R7MPD were chosen for the design.

$$C_A = C_B = 4.7uF$$

These capacitors had a measured ESR of 6 ohms at 105 kHz

$ESR_{CA} = ESR_{CB} = 6\Omega$

Recalculate remaining power budget based on power dissipation by the ESRs in the input capacitors.

$$P_{BUDGET} = P_{BUDGET} - \left(I_{CA\_RMS}\right)^2 \times ESR_{CA} - \left(I_{CB\_RMS}\right)^2 \times ESR_{CB} \approx 1.36W$$

Filter Inductor (L_A):
Filter inductor (L_A) is used for EMI filtering. In this design it is just a place holder and the design has not been optimized for EMI. 470uH inductor from Bourns was chosen, part number RLB0608-471KL. This inductor has a DCR of 6.5 ohms.

$$DCR = 6.5\Omega$$

Recalculate power budget based on DCR losses

$$P_{BUDGET} = P_{BUDGET} - \left(I_{PRMS}\right)^2 \times DCR \approx 1.212W$$

Fusible Resistor (R_L):
To limit the inrush current during power and for safety a 10 ohm, 3W fusible resistor from Bourn, part number PWR4522AS10R0JA was placed at the input of this design.

$$R_L = 10\Omega$$

Recalculate power budget based on estimated R_L losses

$$P_{BUDGET} = P_{BUDGET} - \left(I_{PRMS}\right)^2 \times R_L \approx 0.984W$$

Trickle Charge Resistor (R_T):
To reduce no load power losses R_T and to keep no load power to a minimum, three 5.11MΩ are used in series for R_T

$$R_T = 5.11M\Omega \times 3 = 15.33M\Omega$$

$$P_{RT} = \frac{\left(V_{INMAX}\sqrt{2}\right)^2}{R_T} \approx 9.2mW$$, Total trickle charge resistor power dissipation

Recalculate power budget

$$P_{BUDGET} = P_{BUDGET} - P_{RT} \approx 0.974W$$

VDD Capacitor Selection (C_{DD}):
The C_{DD} is selected with the following equation based on the desired startup time (dt_{CDDS}) of the UCC28700 controller and knowing the start current (I_{START}), as well as, the UCC28700 device startup threshold ($V_{VDD(on)}$). For this design a 330nF capacitor was selected.

$$dt_{CDDS} = 1s$$

$$I_{START} = 1.5uA$$

$$V_{VDD(on)} = 21V$$

$$C_{DD} = \frac{\left(\frac{V_{INMIN}\sqrt{2}}{R_T} - I_{START}\right) \times dt_{CDDS}}{V_{VDD(on)}} = 324nF \approx 330nF$$

Note after C_{DD} has been charged up to the device turn on threshold ($V_{VDD(on)}$), the UCC28700 will initiate three small gate drive pulses (DRV) and start sensing current and voltage. (Please refer to figure 2) If a fault is detected such as an input under voltage or any other fault, the UCC28700 will terminate

the gate drive pulses and discharge C_{DD} to initiate an under voltage lockout. This capacitor will be discharged with the run current of the UCC28700 (I_{RUN}) intil the V_{DD} turnoff ($V_{VDD(off)}$) threshold is reached. Note the C_{DD} discharge time (t_{CDDD}) from this forced soft start can be calculated knowing the controller run current (I_{RUN}) without out gate driver switching and the controller's VDD turnoff threshold ($V_{VDD(off)}$) and the following equations. If no fault is detected, the UCC28700 will continue driving Q_A and controlling the input and output currents [1] and a soft start will not be initiated.

$$I_{RUN} = 2.1mA$$

$$V_{VDD(off)} = 8V$$

$$dt_{CDD} = C_{DD} \frac{V_{VDD(on)} - V_{VDD(off)}}{\left(\frac{V_{INMAX}\sqrt{2}}{R_T} - I_{RUN} \right)} = 71ms$$

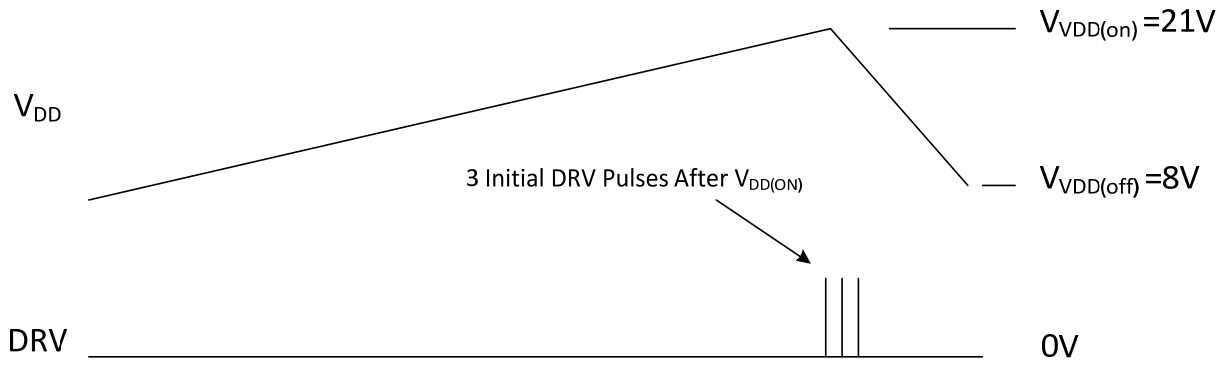

Figure 2, VDD and DRV at Startup with Fault

Current Sense Resistor (R_{CS}):
For this design 2.05 ohm resistor was selected based on a nominal maximum current sense signal of 0.75V.

$$R_{CS} = \frac{0.75V}{I_{PPK}} = 1.965\Omega \approx 2.05ohm$$

$P_{RCS} = (I_{PRMS})^2 \times R_{CS} = 0.046W$, nominal current sense resistor power dissipation

Recalculate power budget

$$P_{BUDGET} = P_{BUDGET} - P_{RCS} \approx 0.928W$$

Select Output Diode (D_G):

Calculate diode reverse voltage (V_{RDG})

$$V_{RDG} = V_{OUT} + V_{INMAX}\sqrt{2}\frac{1}{a_1} \approx 29.45V$$

Calculate peak output diode (I_{DGPK})

$$I_{DGPK} = I_{SPK} = 4.7A$$

For this design we selected a 3A, 40V schottky rectifier with a forward voltage drop (V_{FDG}) of 0.31V.

$$V_{FDG} = 0.31V$$

Estimated diode power loss (P_{DG})

$$P_{DG} = \frac{P_{OUT} \times V_{FDG}}{V_{OUT}} \approx 0.31\text{W}$$

Recalculate power budget

$$P_{BUDGET} = P_{BUDGET} - P_{DG} \approx 0.618W$$

Select Output Capacitors (C_{OUT}):

Select output ESR based on 90% of the allowable output ripple voltage

$$ESR_{COUT} = \frac{V_{RIPPLE} \times 0.9}{I_{SPK}} = \frac{100mV \times 0.9}{4.7A} = 19m\Omega$$

For this design the output capacitor (C_{OUT}) was selected to prevent V_{OUT} from dropping below the minimum output voltage during transients (V_{OTRM}).

$$V_{OTRM} = 4.1V$$

$$C_{OUT} \geq \frac{2ms \times \frac{P_{OUT}}{V_{OUT} \times 2}}{V_{OUT} - V_{OTRM}} = 1.1mF$$

For this design two 560uF capacitors were used in parallel on the output, with an ESR of 13mΩ each.

$$C_{OUT} = 2 \times 560uF = 1.12mF$$

$$ESR_{COUT} = \frac{13m\Omega}{2} = 6.5m\Omega$$

Estimate total output capacitor RMS current (I_{COUT_RMS})

$$I_{COUT\_RMS} = \sqrt{\left[\frac{I_{SPK} \times \sqrt{D_{MAG}}}{\sqrt{3}}\right]^2 - \left(\frac{P_{OUT}}{V_{OUT}}\right)^2} \approx 1.46A$$

Estimate total output capacitor loss (P_{COUT})

$$P_{COUT} = \left(I_{COUT\_RMS}\right)^2 \times ESR_{COUT} = 14mW$$

Recalculate power budget

$$P_{BUDGET} = P_{BUDGET} - P_{COUT} \approx 0.604W$$

Select FET Q_A:

For this design we had chosen a 600V rated MOSFET with the following characteristics:

$R_{DSON} = 4.5ohm$, FET Q_A on resistance

$C_{OSS} = 8.5\,pF$, average FET drain to source capacitance

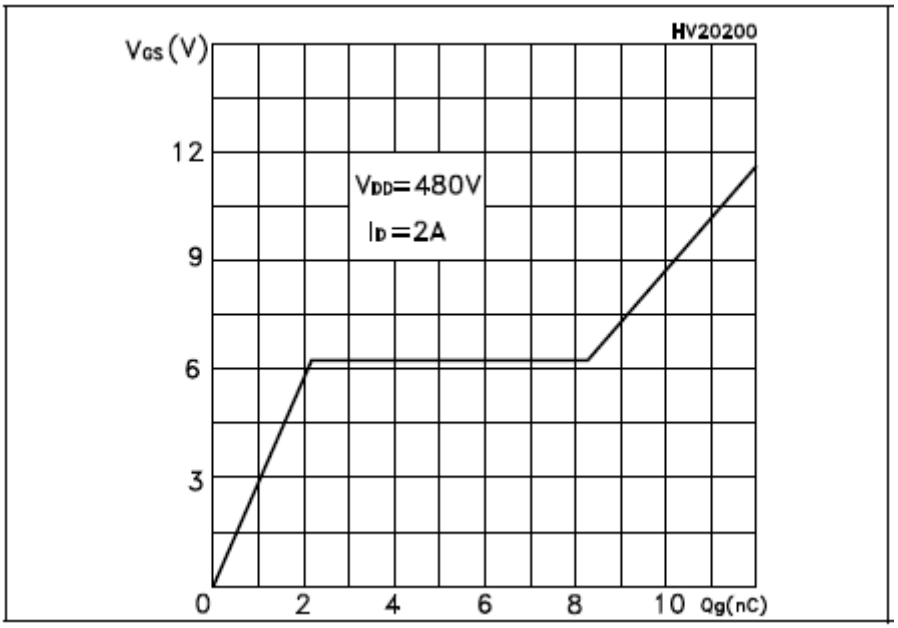

Figure 3, Gate Charge vs V_{gs}

Estimate FET losses (P_{QA})

$I_{DRIVE} = 0.35A$, maximum FET gate drive current

$Q_g = 9nC$, gate charge just above the miller plateau

$t_r = Q_g \frac{2}{I_{DRIVE}} \approx 52ns$, estimated FET V_{ds} rise and fall time

Estimate FET power loss by driving the FET's gate (P_g)

$Q_{g1} = 12nC$, Gate charge at 12V drive clamp

$V_g = 12V$

$P_g = 12V \times Q_{g1} \times f_{MAX} = 15mW$

Calculate the average input voltage to the flyback at the maximum input voltage (V_{INMAX}).

$$V_{FLY} = V_{INMAX} \times \sqrt{2} - \frac{V_{INRIPPLE}}{2} - 2 \times V_{FDA} \approx 347V$$

Estimate FET average switching loss (P_{SW})

$$P_{SW} = V_{FLY} - (V_{OUT} + V_{VDG}) \times a_1 \frac{I_{PPK} \times t_r \times f_{MAX}}{2} \approx 269mW$$

Estimated FET Coss power dissipation (P_{COSS})

$C_{OSS} = 8.5pF$, average FET drain to source capacitance

$$P_{COSS} = \frac{C_{OSS}}{2} \times (V_{FLY})^2 \times f_{MAX} \approx 54mW$$

Calculate power loss from Rdson (P_{RDSON})

$$P_{RDSON} = (I_{PRMS})^2 \times R_{DSON} = 0.1W$$

Estimate total FET losses (P_{QA})

$$P_{QA} = P_{RDSON} + P_{SW} + P_g + P_{COSS} \approx 441mW$$

Recalculate the power budget

$$P_{BUDGET} = P_{BUDGET} - P_{QA} \approx 163mW$$

Setup Zener Clamp to Protect FET Q_A:

$V_Z = 82V$, Zener Clamp Voltage (D_Z)

$V_{ds\_MAX} = 600V$, FET maximum drain to source voltage

$V_{CLAMP} = V_{ds\_MAX} \times 0.9 - V_{INMAX}\sqrt{2} \approx 165.2V$, Available Clamp Voltage to Protect FET Q_A

$$R_S = \frac{V_{CLAMP} - 0.6 - V_Z}{I_{PPK}} \approx 216.5\Omega$$

Select a standard resistor for the design.

$R_S = 215\Omega$

Estimate Zener Clamp/L_{LK} power dissipation (P_{LK})

$$P_{LLK} = \frac{L_{LPK} \times (I_{PPK})^2 \times f_{MAX}}{2} = 122mW$$

Recalculate power budget

$$P_{BUDGET} = P_{BUDGET} - P_{LLK} \approx 40mW$$

Select VS voltage divider (R_{S1}, R_{S2}):

$I_{VSL(run)} = 220uA$ VS Line-sense run current

Note R_{S1} so the converter will go into under voltage lockout when the input is below 80% of the minimum specified input voltage.

$$R_{S1} = \frac{\frac{a_2}{a_1} V_{INMIN} \sqrt{2} \times 0.8}{I_{VSL(run)}} \approx 115.6k\Omega$$

Select a standard resistor for the design

$$R_{S1} = 121k\Omega$$

$$R_{S2} = \frac{4V}{\frac{(V_{OUT} + V_{DG}) \times a_2 - 4V}{R_{S1}}} \approx 27.7k\Omega$$

Calculated R_{S2} is a starting point and will need to be adjusted in circuit. To have a 5V regulated output this resistor was adjusted to 30.1kΩ

$$R_{S2} = 30.1k\Omega$$

Calculate VS divider power dissipation (P_{VS})

$$P_{VS} = \frac{\left(\sqrt{D_{MAX}} (V_{OUT} + V_{DG}) a_2\right)^2}{(R_{S1} + R_{S2})} \approx 1.3mW$$

Select auxiliary diode (D_E) for this design that had a forward voltage drop (V_{DE}) of 0.6V.

$$V_{DE} = 0.6V$$

$V_{DD} = (V_{OUT} + V_{DG}) \times a_2 - V_{DE} \approx 20.8V$, UCC28700 supply voltage at V_{DD}

$V_{RDE} = V_{DD} + V_{INMAX} \sqrt{2} \times \frac{a_2}{a_1} \approx 115V$, maximum reverse voltage across V_{DE}

$I_{RUN} = 2.1mA$, UCC28700 bias current when gate drive = 0V

$I_{DD} = \frac{P_g + I_{RUN} \times V_{VDD}}{V_{DD}} \approx 2.8mA$, Estimated UCC28700 VDD current.

Calculate D_E power dissipation (P_{DE})

$P_{DE} = I_{DD} \times V_{DE} \approx 1.7mW$

Recalculated power budget

$P_{BUDGET} = P_{BUDGET} - P_{VS} - P_{DE} \approx 037mW$

Preload Resistor Selection (R_Z):
To keep the output voltage from climbing at no load a pre-load resistor is required. This is generally a trial an error process. For this designs the preload resistor that kept the output regulated under no load conditions was 3.01 kΩ.

$R_Z = 3.01K$

Calculate R_Z power dissipation (P_{RZ})

$P_{RZ} = \frac{(V_{OUT})^2}{R_Z} \approx 8.3mW$

Recalculated power budget and there is 29 mW of margin left in the power budget to meet the efficiency requirements of the design. Note in production designs, more margin might be required. Also note these calculations are estimations and the final design may need to be adjusted to hit efficiency and regulation requirements.

$P_{BUDGET} = P_{BUDGET} - P_{RZ} \approx 29mW$

Internal Blanking

The UCC2870X controller regulates the output voltage by sensing the auxiliary (Aux) winding. This removes the need for opto isolator feedback scheme reducing the cost of the design. However, this voltage control feedback scheme is susceptible to leakage spikes at the switch node that occur in most flyback converters. This signal is coupled through the turns ratio of the transformer (T1) and shows up on the Aux winding during t_{LK_RESET} , please refer to figure 4 for details.

To help insure the leakage spike on the Aux winding does not cause a control issues, the UCC2870X blanks (t_B) the Aux signal to the controller for 500 ns to 1.5 us depending on loading. Please see the data sheet details [1]. **Note the ringing on the auxiliary winding needs to be less than 100mV peak to peak after t_B. Snubbing circuitry on the secondary and/or auxiliary winding may be required to reduce ringing.**

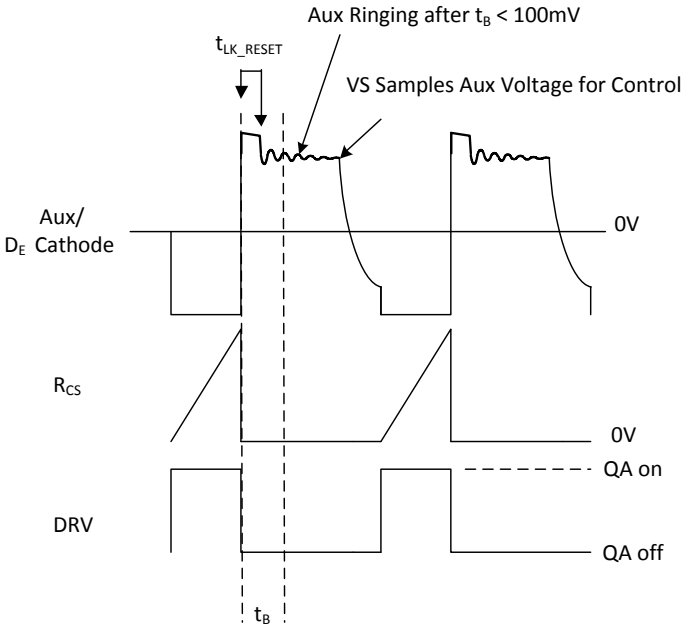

Figure 4, Auxiliary Winding VS Blanking

To ensure the leakage spike does not cause control issues it needs to be dissipated before the Aux blanking (t_B) has terminated. The tank frequency (f_{LC}) between the switch node capacitance (C_{SWN}) and the transformer leakage inductance (L_{LK}) should be greater than 1MHz.

$$f_{LC} = \frac{1}{2 \times \pi \times \sqrt{L_{LK} \times C_{SWN}}}$$

$$f_{LC} \geq \frac{1}{2 \times 500ns} = 1MHz$$

Select line compensation resistor R_{LC}:

Resistor R_{LC} provides offset to the peak current comparator input (CS). R_{LC} is adjusted to terminate the gate drive signal (B) early to prevent primary current (A) from over shooting [1]. Please refer to figures 5 and 6 for details.

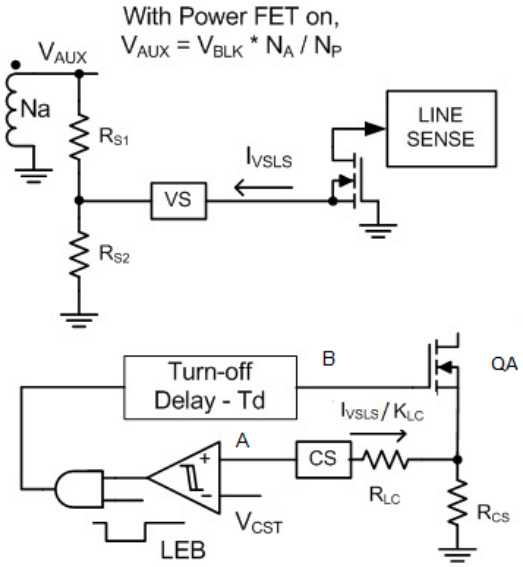

Figure 5, Peak Current Limit Comparator

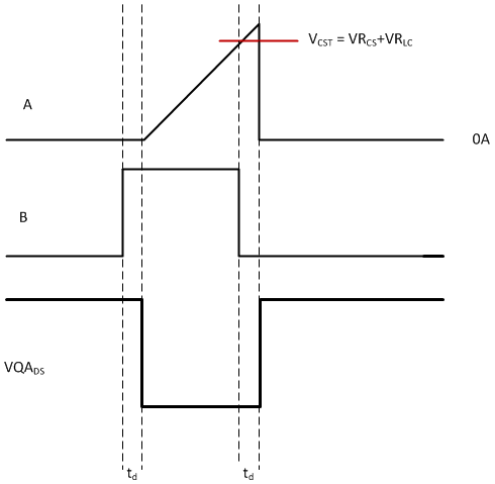

Figure 6, CS(A), QA_g(B), VQA_{DS} Signals

$K_{LC} = 25$, Line Compensating Ratio [1]

Calculate R_{LC} initial resistor setting based on QA_{DS} rise and fall time (t_r)

$$R_{LC} = \frac{K_{LC} \times R_{S1} \times R_{CS} \times t_r \times a1/a2}{L_{PM}} \approx 1.38k\Omega$$, Starting Point for R_{LC}

In circuit adjust R_{LC} so the maximum output current is (I_{OUT}). For this design RLC was set to 4.64 kΩ.

$R_{LC} = 4.64k\Omega$

Estimate no load input power (P_{NL}):

$f_{MIN} = 1kHz$, Minimum operating frequency

$P_g = V_g \times Q_g \times f_{MIN} = 144uW$, gate drive power dissipation at f_{MIN}

$I_{WAIT} = 85uA$, VDD input current at 1 kHz operating frequency [1]

$P_{VDD} = P_g + I_{WAIT} \times V_{DD} \approx 1.9mW$, Estimated UCC28700 power dissipation at f_{MIN}

Estimate switching losses (P_{SWFM}) at high line at f_{MIN}

$$P_{SWFM} = V_{FLY} - (V_{OUT} - V_{VDG}) \times a1 \frac{\frac{I_{PPK}}{3} \times t_r \times f_{MIN}}{2} \approx 945uW$$

$P_{COSS} = \frac{C_{OSS}}{2} \times (V_{FLY})^2 \times f_{MIN} \approx 0.5mW$, estimated C_{OSS} losses at f_{MIN}

$P_{LLK} = \frac{L_{LPK} \times \left(\frac{I_{PPK}}{3}\right)^2 \times f_{MIN}}{2} \approx 129uW$, estimate of leakage power dissipation at no load

The estimated no load input power (P_{NL}) is roughly 22 mW. In the actual 5W design the no load input power was roughly 20 mW at 230V RMS input voltage.

$P_{RZ} = 8.3mW$

$P_{RT} = 9.2mW$

$P_{NL} = P_{VDD} + P_{SWFM} + P_{COSS} + P_{RZ} + P_{RT} + P_{LLK} \approx 22mW$

5W EVM Schematic:

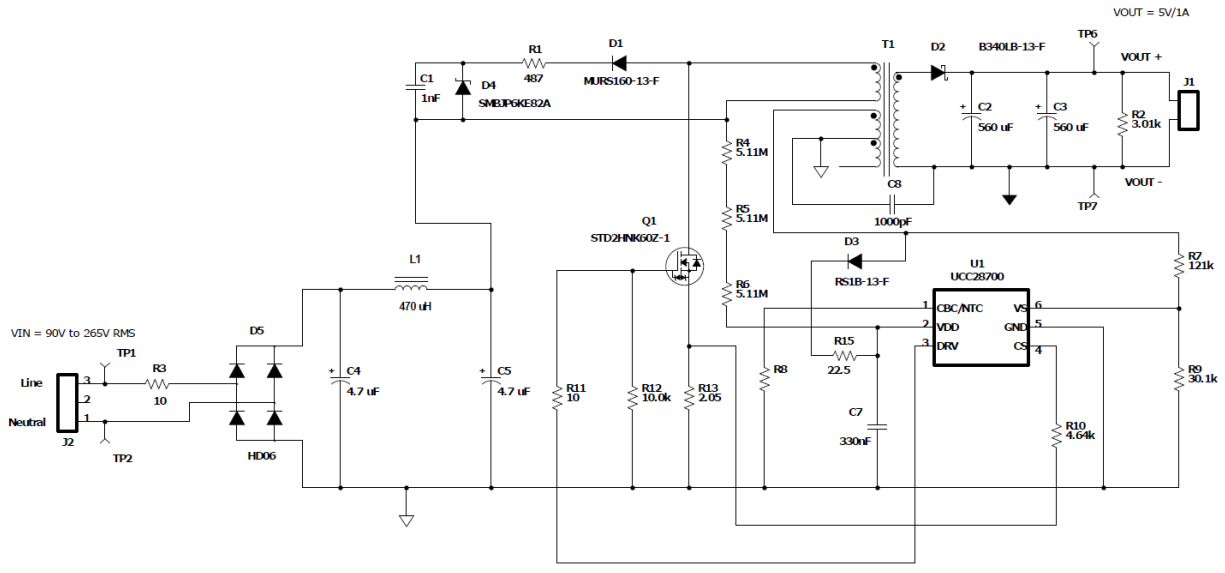

Figure 7, Schematic

Efficiency:

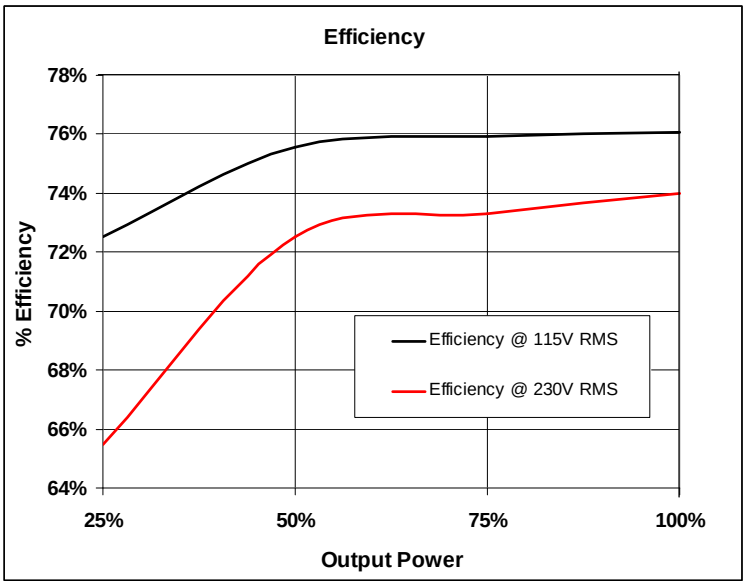

Figure 8, Efficiency

Load Transient at 115V RMS

CH1 = I_{OUT}, CH4 = V_{OUT} with a 5V offset

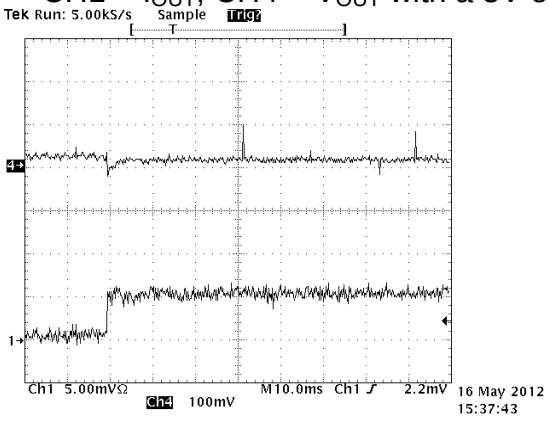

Figure 9, 0.1 to 0.6A load step

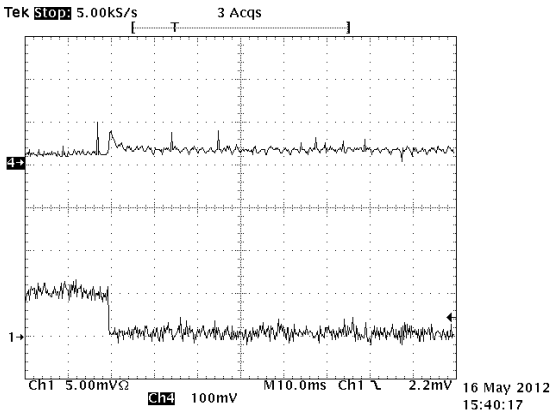

Figure 10, 0.6 to 0.1A load step

Load Transient at 230V RMS

a. CH1 = I_{OUT}, CH4 = V_{OUT} with a 5V offset

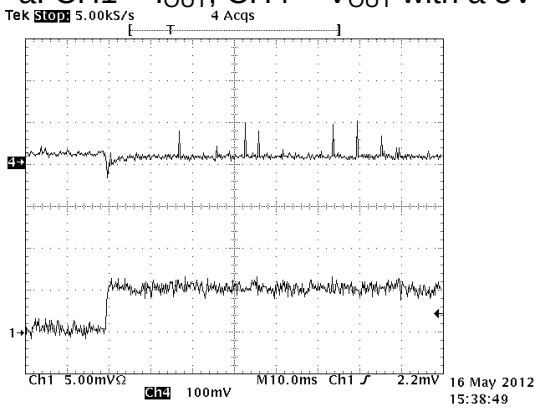

Figure 11, 0.1 to 0.6A load step

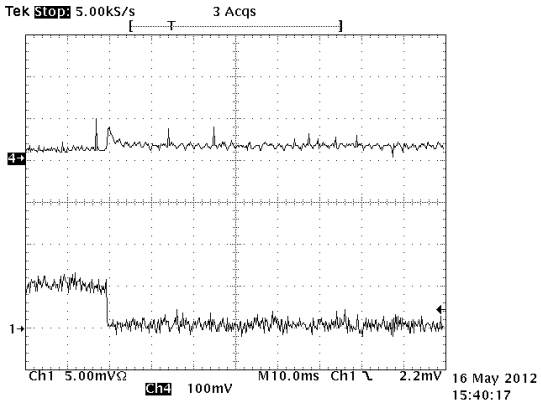

Figure 12, 0.6 to 0.1A load step

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