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External Slope Compensation for UCC2897A in Some Special Applications

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ABSTRACT

This paper introduces an external slope compensation circuit for the UCC2897A. It is helpful in some special applications where there is a need to set a minimum DC bias (>2.5V) at the UCC2897A FB pin. Circuit analysis and test result are given in this paper.

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1 Introduction

The slope compensation in peak current mode control has been used widely to cancel the sub-harmonic oscillation and to resolve stability issues. A power supply based on UCC2897A is configured to peak current mode control. However, different external feedback control circuitry may bring up the issue of achievable minimum duty cycle. With flexible configuration of slope compensation for UCC2897A, usually one can obtain the required minimum pulse width easily.

In some special applications such as the one shown in Figure 2, UCC2897A FB pin is biased by a minimum DC voltage (>2.5V). Then minimum pulse width issue arises with the internal slope compensation on this condition. When this happens, we suggest an external slope compensation circuit by floating RSLOPE pin to disable the internal compensation, adding Rs between VREF pin and CS pin to get the external slope compensation. Figure 1 shows our suggested external slope compensation circuit to be used when the FB has a DC bias (>2.5V).

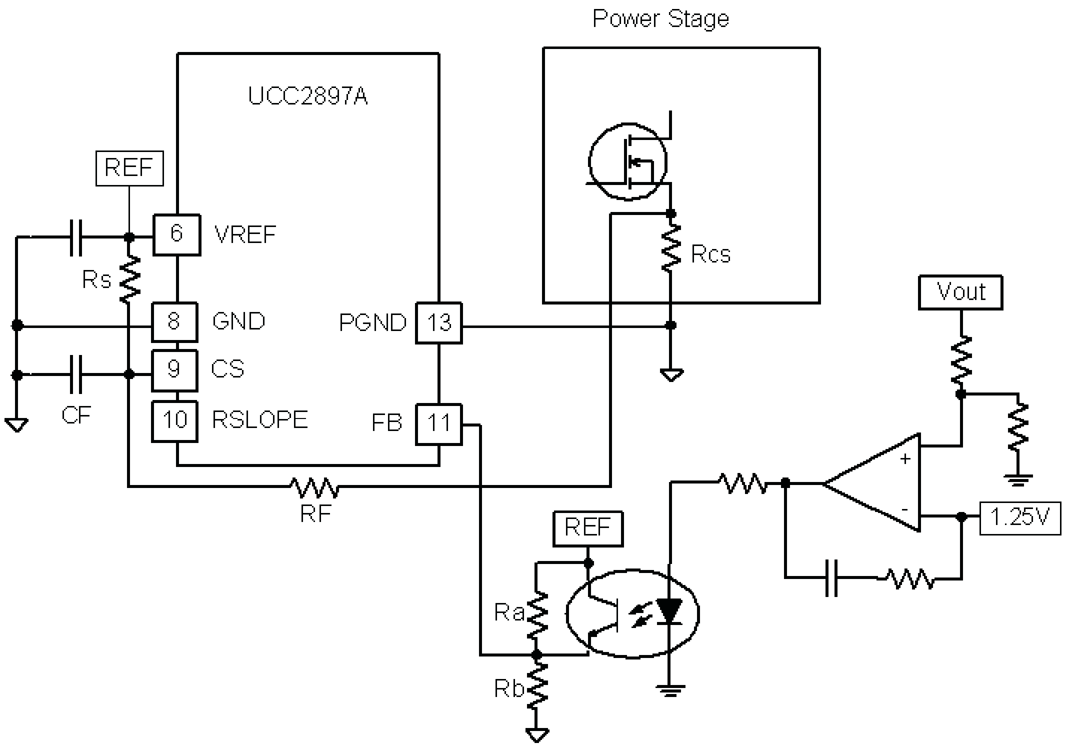

Figure 1. External Slope Compensation When FB has a DC Bias (>2.5V)

2 Minimum Pulse Width Issue When the FB has a Minimum DC Bias (>2.5V)

If the internal slope compensation signal of Figure 2 is used, UCC2897A presents minimum pulse width limitation due to the delay of the internal compensation.

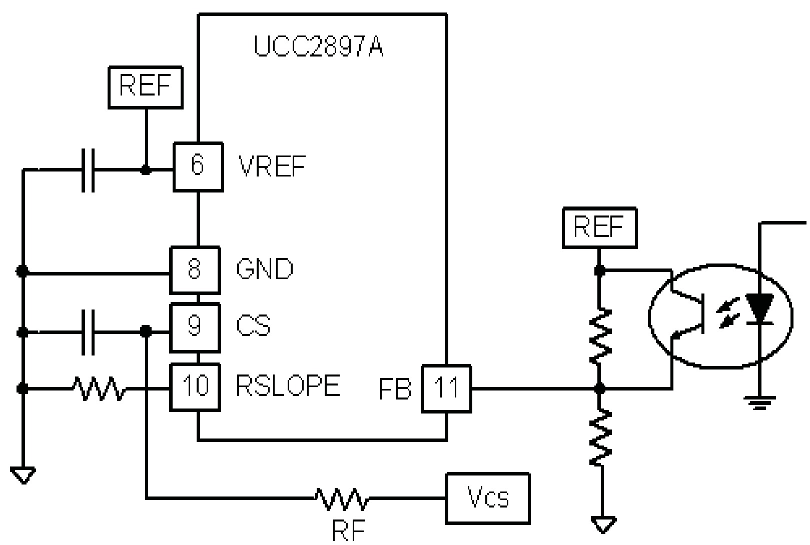

Figure 2. Internal Compensation When FB has a DC Bias

In Figure 2, the minimum DC bias for "FB" voltage is reached with the zero OPT (Opto-coupler) current.

$$\text{Minimum } V_{bias} = FB_{I(OPT)} = 0 \quad (1)$$

Figure 3 shows part of the functional block diagram for the UCC2897A. The current signal for the $5 \times I_{SLOPE}$ current source has a delay compared with the RSLOPE signal.

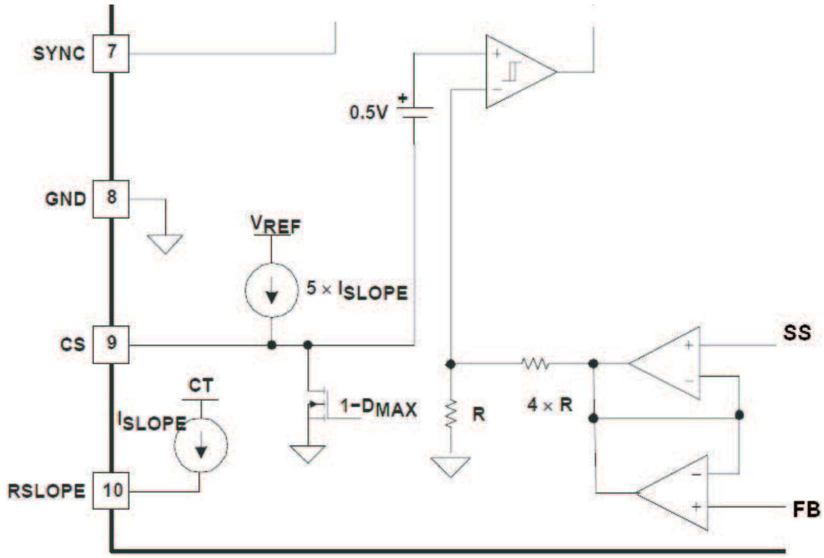

Figure 3. Part of the Functional Block Diagram for the UCC2897A

A 2.7-VDC bias voltage present on the FB pin requires the CS pin to reach 40mv, computed by:

$$0.2 \text{ X Vbias} -0.5 = 0.2 \text{ X } 2.7 -0.5 = 40\text{mV} \tag{2}$$

in order to turn off the main switch. Due to the internal delay the pulse width cannot be narrowed down to what is needed, as shown in Figure 4.

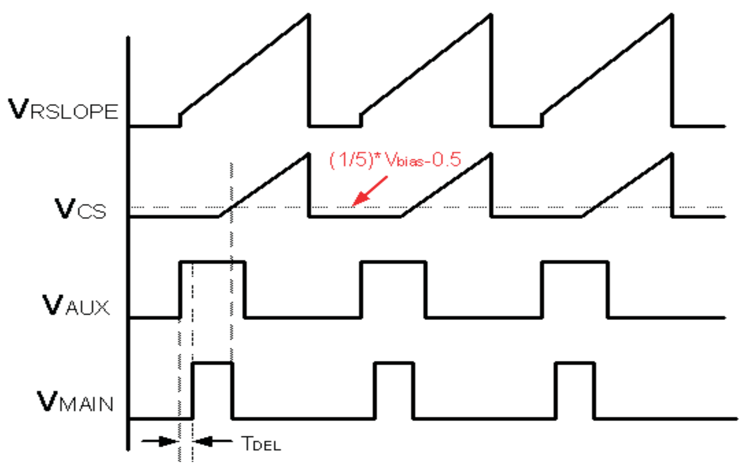

Figure 4. Waveforms With V_{bias} at the FB Pin

However, when FB voltage is not present, the DC bias in that regard can vary between VREF and 0VDC. Figure 5 shows minimum pulse width can be achieved from the internal slope signal.

$$\text{Minimum } V_{bias} = FB_{I(OPT)\ =\ max} \leq 2.5\text{ V} \tag{3}$$

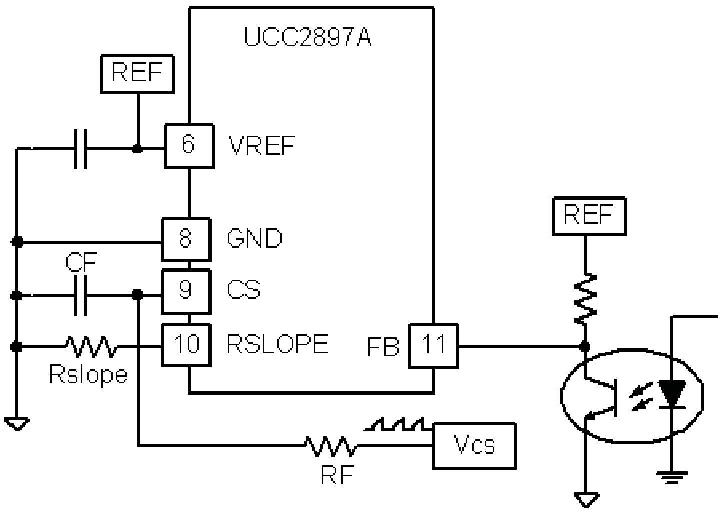

Figure 5. No DC Bias Feedback Circuit With Internal Slope Compensation

3 External Slope Compensation Circuit Design

The circuit shown in Figure 6 provides an external slope compensation that can help meet the minimum pulse width requirement when DC bias is present on FB pin. In such a case, let RSLOPE pin float to disable the internal compensation, and add RS between the VREF pin and CS pin to get the external slope compensation.

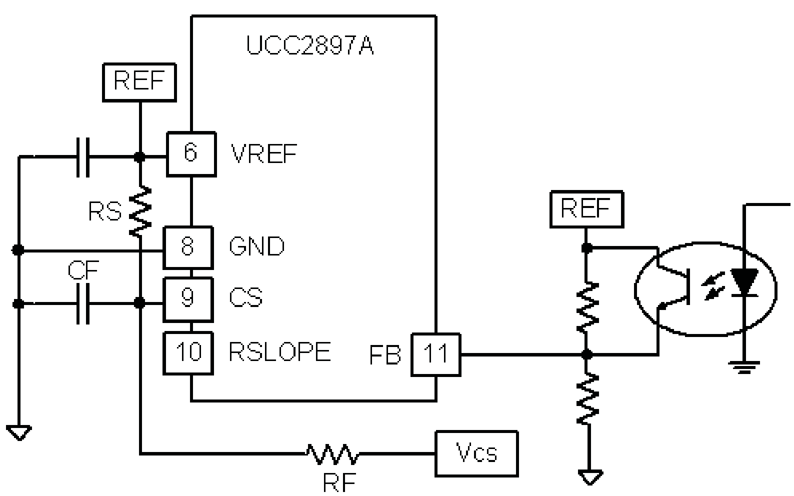

Figure 6. External Compensation Circuit

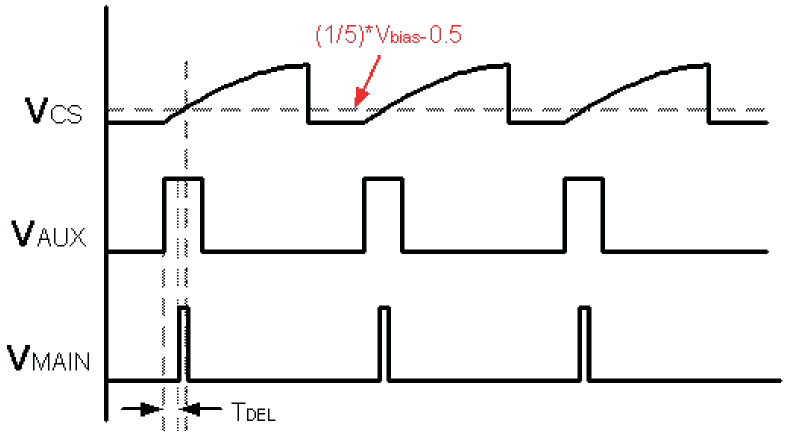

Figure 7. The Waveform for External Compensation

As shown in Figure 7, when adding the external slope compensation to the circuit, the compensation signal can rise up at the CS pin immediately; as such, the suggested slope compensation can achieve a stable and required narrow pulse width.

Figure 8 is the waveform with the internal slope compensation, captured from an actual circuit described by Figure 2. The test condition was: switching frequency = 391kHz, FB bias voltage = 2.76V, RSLOPE = 95kΩ, RF = 1.4kΩ, CF = 150pF.

Figure 9 is the waveform with the proposed external slope compensation, captured on the same circuit except for changes providing the external slope compensation; where RS = 300kΩ, CF = 150pF, and RF = 15kΩ.

With the proposed external slope compensation, the achieved minimum duty cycle is 6% while with the internal compensation, the minimum duty cycle can only be 16%.

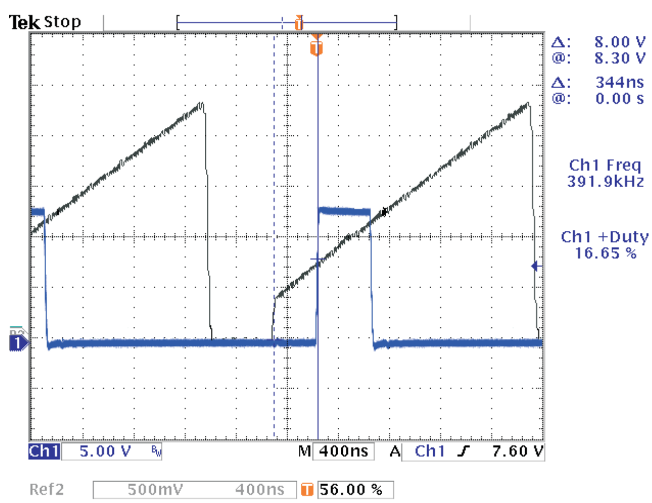

Figure 8. Waveform With Internal Compensation When FB has 2.76V Voltage Bias

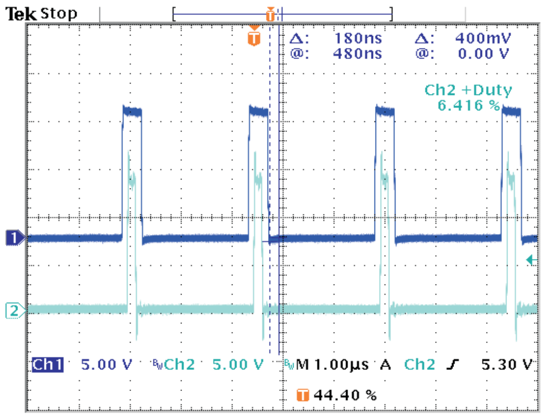

Figure 9. Waveform With External Compensation When FB has 2.76V Voltage Bias

4 Conclusion

The proposed external slope compensation can achieve the required minimum pulse width when the FB pin of the UCC2897A presents a DC bias.