Application Report
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bq78PL114 System Design Guidelines

James Moran — *PMP - BMS High-Cell and Emerging*

ABSTRACT

This application report provides a system-level functional description of the bq78PL114 circuitry and describes recommended system design and printed-circuit board layout techniques to ensure best performance.

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1 Introduction

The purpose of this document is to communicate the important technical details to design engineers creating Battery Management Units (BMU) based on the bq78PL114 controller by Texas Instruments. This allows the designer to make application-specific decisions regarding the design of the BMU printed-circuit board (PCB) and pack construction. The report includes system level design, BMU subcircuit descriptions and PCB design and layout guidelines. The example system consists of a four-series cell pack. These recommendations can be applied to high-number-series cell count where one or more bq76PL102 dual-cell, Li-ion battery monitors are added.

CAUTION

Two firmware versions are available for the bq78PL114. The differences in circuit design between the two versions are subtle. The orderable device is called bq78PL114 and includes firmware (FW) 4452 installed. The bq78PL114 can be upgraded by the user to FW5000 and then is referred to as bq78PL114S12. The part name bq78PL114 is used when common features are described. Differences are identified by the use of separate part numbers. The major differences that affect hardware design involve maximum cell count, sense resistor selection, temperature sensor operation, and SOCi display options. Consult Section 5 for additional information to supplement this material.

2 System Design

The design of the connections from the BMU PCB to the battery pack is important to ensure the desired level of performance. The following text discusses power, cell voltage sense, and temperature sensor connections.

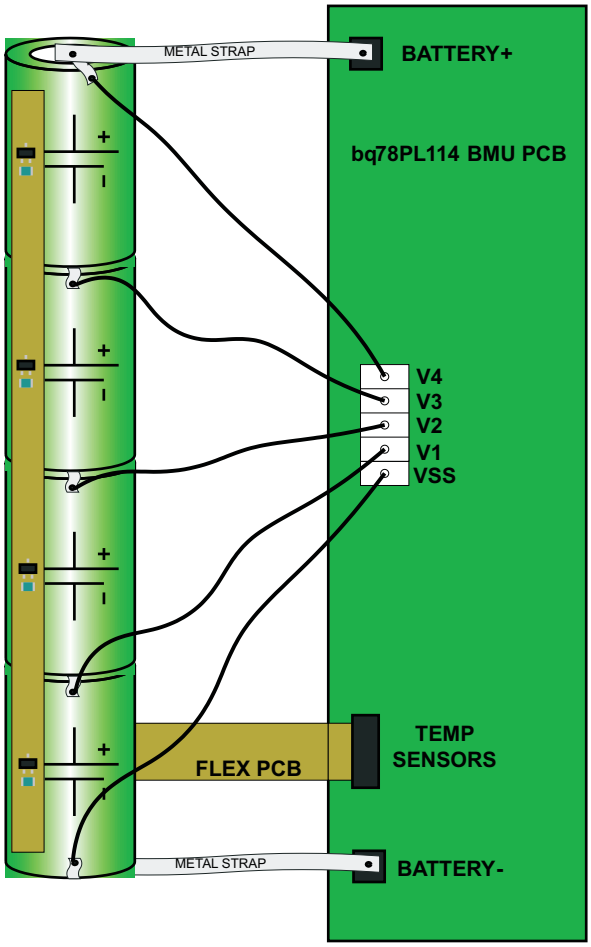

Figure 1. Battery to BMU Power, Cell Voltage, and Temperature Connections

2.1 Battery Power Connections

The connection to the top and bottom of the battery is called BATTERY+ and BATTERY–, respectively. Both connections require a very low impedance to minimize voltage drop. Typical connection impedances attempt to equal that of the pack disconnect MOSFETs and current sense resistor. These are typically in the tens of milliohms. The impedance created by the BATTERY± connections, particularly the inductive component, can create large voltage swings when connected to high-frequency switched loads. Properly minimizing this connection inductance reduces the level of transient voltage suppression devices required on the BMU PCB and throughout the host system.

The bq78PL114 does not connect directly to BATTERY+. The design of the BATTERY+ connection and related performance is up to the user's discretion and typical industry practices.

The BATTERY– connection does have a specific design criterion relating to the bq78PL114 operation. The voltage drop developed along the connection from BATTERY– to the sense resistor must not exceed 100 mV under charge current conditions. This 100 mV includes the voltage drop associated with the battery wires or straps and PCB copper traces and any PCB connections. The voltage drop just described is drawn as voltage V_{ab} in Figure 2. V_a specifies the connection location of V_{ss}. In other words, the voltage drop from V_{ss} to the BATTERY- side of the sense resistor is less that 100 mV during charge periods.

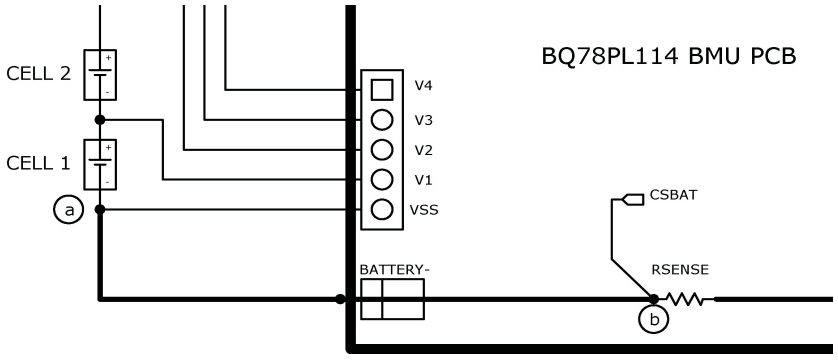

Figure 2. Battery–Connection Voltage Drop Requirements: V_{ab} < 100 mV During Charge

2.2 Cell Temperature Sensing

The bq78PL114 BMU permits individual sensing of cell temperatures using a low-cost dual diode and a filter capacitor. Dual diode MMBD4148SE by Fairchild Semiconductor and others is the diode that has been characterized for use with the bq78PL114. Avoid using other diodes because they may have a different performance curve over temperature.

Pack temperature information is used for gas gauging and safety-monitoring functions. The number of temperature sensors can vary based on individual application requirements. At least one temperature sensor measurement point is required for the bq78PL114 BMU to function properly.

Distributing sensors throughout the pack on a per-cell basis has the benefit of being able to detect extreme temperature fluctuations faster than using a single pack sensor. This can result in the detection and avoidance of a catastrophic cell failure event before it happens.

Cell temperature sensors can be physically implemented in a few different ways. For instance, a flexible PCB array can be created to conveniently distribute the sensors throughout the pack without complicated wire harnesses. This flexible circuit array then can terminate back at the main BMU PCB. This is shown in Figure 1.

Although temperature sensors are referenced to a cell voltage, VSS or V2, for instance, avoid creating a temperature sensor design that terminates the cathode of the sensor at the cell tab of its reference. This creates a large signal loop area that can conduct noise on the temperature sensor signal. The recommended method is to have both sensor signal lines travel closely in parallel from the bq78PL114 all the way to the measurement location (cells). The best way to do this is to include both the sensor source (XT1, 2, 3, or 4) and the return (VSS or V2) on the temperature sensor PCB.

2.3 Cell Voltage Sense Connections

Measurement accuracy of individual cell voltages has a direct impact on BMU performance. Cell voltages are used to determine certain gas gauging parameters as well as determine fault and safety conditions. Monitoring these critical voltages requires a physical connection to each cell terminal that ensures highest measurement accuracy. Any voltage drop induced by the method and/or physical location of the connections to the cells is interpreted as a part of the total cell voltage.

Highest accuracy cell voltage sensing requires connections to the cell terminals that minimize the series voltage drop due to battery current. This is commonly referred to as a Kelvin Connection (see Figure 3). For optimum performance in almost all applications, the bq78PL114 BMU requires n+3 connections, where n is equal to the number of series connected cells in the pack. The physical location of the connection point in the pack usually has the most impact on cell voltage accuracy. See Figure 3.

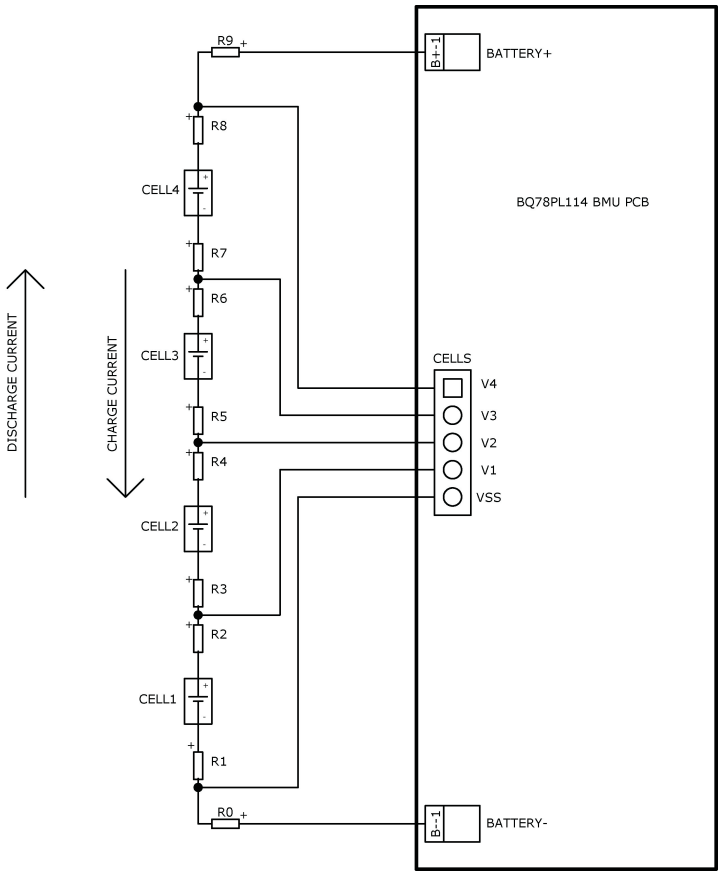

Figure 3. Schematic of Battery Sense Connections and System Impedances

Consider the ideal case where CELLs 1–4 always have the same internal impedance and the impedances shown as R1– R8 also are equal and approach zero. (The impedances in the diagram are shown as lumped parameters. Physical battery packs have connections that typically have uniformly distributed impedances.) All the cell voltage measurements are of equal value at any battery current in this ideal case. Practical designs strive to mimic the ideal case but fall short by some degree. Impedances R0 and R9 usually have values that are higher than R1–R8 due to physical and possibly material cost constraints.

The impedances R1–R8 produce the undesirable effect of increasing the measured cell voltages during charge and lowering the measured cell voltages during discharge. Observe the following simple analysis (Figure 4).

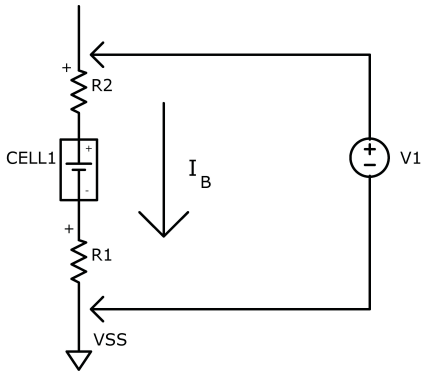

Figure 4. Effect of Impedance on V1 Voltage Measurement

The measured voltage at cell 1 is determined to be:

$$+V_1 - R_2(I_B) - CELL1 - R_1(I_B) = V_{SS}$$

OR

$$(V_1 - V_{SS}) = CELL1 + (R_1 + R_2)(I_B) \quad (1)$$

The sign of battery current is positive during charge: Battery Current (I_B = +I).

$$(V_1 - V_{SS}) = CELL1 + (R_1 + R_2)(+I) \quad (2)$$

This shows that the impedances R1 and R2 result in a positive cell voltage error. The sign of the battery current is negative during discharge: Battery Current (I_B = –I). So, using this in Equation 1 results in,

$$+V_1 - R_2(-I) - CELL1 - R_1(-I) = V_{SS}$$

OR

$$(V_1 - V_{SS}) = CELL1 - (R_1 + R_2)(I) \quad (3)$$

This shows that the impedances R1 and R2 contribute to a negative cell voltage error during battery discharge.

In almost all cases, the middle cells are connected with a short length of metal strapping. For these, locate the cell sense point in the middle of the metal strap as shown in Figure 1. This splits the voltage drop due to the strap impedance equally between the two cell voltage measurements. Equalizing the cell voltage error between cells due to strap impedance ensures the best discharge and charge performance at the pack level. This can be done, for example, by making impedances R1 to R8 in Figure 3 all equal and as close to zero as possible.

The impedance of the Kelvin sense wire connection is not considered here because the current flowing in these connections is usually many orders of magnitude lower than the battery current and produces negligible errors. In addition, cell voltage measurement does not occur during the time when PowerPump™ balancing is active.

Here is a small case study of trade-offs in system design:

It may seem advantageous to minimize the number of connections for the sake of cost. For instance, the BATTERY+ connection is at the top cell in the stack and passes load current to the BMU circuit to be switched on/off by the pack disconnect MOSFETs. Material cost can be saved by using this single connection also as the top cell input to the bq78PL114 (pin V4) in place of a second, Kelvin-style connection. The resistive and inductive drops that are seen by this load-carrying connection (wire or strap) can be in the range of 10 s to 100 s of millivolts. As a result of this cost-saving measure, the top cell voltage reading can have a voltage measurement offset proportional to pack current. Some low-current applications may produce a tolerable error.

3 Circuit Description

Two reference schematics are used to demonstrate the functionality of the bq78PL114. One is based on firmware 5000 and is referred to as the bq78PL114S12. The second is based on firmware 4452 and is referred to as bq78PL114. Both schematics appear in Appendix A. See the reference schematics and the bq78PL114 data sheet for recommended component values when not listed in the circuit descriptions.

3.1 Device Ground Connection (VSS)

The ground reference for the bq78PL114 is VSS, located on pin 48, as well as the metal pad under the QFN-48 package. This is likely the most important circuit net in the BMU. VSS must be connected directly to the voltage reference of the lowest cell in the battery. See the preceding discussion on cell connections for details. A separate connection point must be used to bring this VSS reference to the BMU circuit. It is not recommended to tap off of the BATTERY– PCB connection to make the VSS connection.

3.2 Power to Device and Decoupling Capacitors

The four pins labeled V1, V2, V3, and V4 are used for cell voltage sensing as well as powering the bq78PL114. Unused cell inputs must be shorted to the connection below it. Each cell input requires a capacitance local to the bq78PL114 to provide power supply decoupling. Typical low ESR, low-cost, ceramic SMD capacitors are suitable in this application.

3.3 VLDO Circuits

Two internally generated reference voltages called VLDO1 and VLDO2 are brought external for connection to bypass capacitors. VLDO1 is referenced to VSS and VLDO2 is referenced to V2. A local capacitance is required across each VLDO pin for correct operation. Typical low ESR, low-cost, ceramic capacitors are suitable in this application. VLDO1 can be used to provide power to external circuits, such as logic circuits, requiring only a few milliamps of current.

3.4 Reset Circuit

The hardware reset input of the bq78PL114, RSTN, is an active-low type input. The signal requires an RC filter network connected to VLDO1 to maintain a stable, high-logic level to the device during operation. The RC filter time constant primarily depends on the level of noise that can be exposed to the VLDO1 circuit net in each specific application.

3.5 PowerLAN™ Circuit

The dual cell-monitoring circuitry inside the bq78PL114 needs to be capacitively coupled to the internal gateway controller of the bq78PL114 to create an internal PowerLAN™ network (see Figure 5).

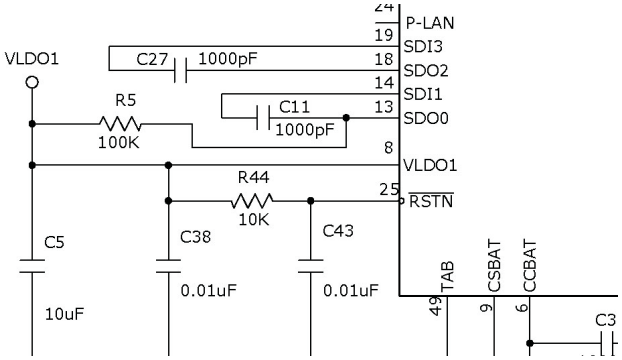

Figure 5. PowerLAN™ Circuitry

First, the SDO0 pin is pulled up to VLDO1 through a 100-kΩ resistor. This resistor initializes the bus after a device reset. Then, each PowerLAN™ node is connected through a 1000-pF capacitor. This allows circuitry of different reference voltages to communicate.

Larger series cell count systems require that the P-LAN pin be capacitively coupled up to an external bq76PL102 through a 1000-pF capacitor to expand the PowerLAN™ network to above four cells.

3.6 Current Sense for Gauging and Safety

The current sense circuits monitor the battery current via a sense resistor for the purposes of gas gauging and safety.

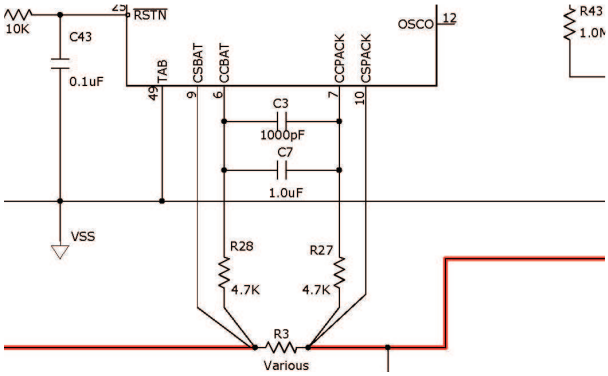

Figure 6. Current Measurement Circuit

A voltage in the millivolt range is generated across the sense resistor that is proportional to the discharge or charge current. The generated voltage is sampled at inputs CCBAT and CCPACK and converted to an instantaneous current value and coulomb reading by the bq78PL114. The CCBAT and CCPACK pins must each have a nominal 4.7-kΩ series resistor for signal conditioning. This input may also need a differential filter capacitor depending on the frequency content of the sampled signal. The digital sampling frequency of the gas gauge is approximately 13 kHz. Choose a capacitor value that provides an appropriate level of attenuation of signals at this frequency to avoid signal aliasing.

The voltage drop across the sense resistor is also monitored by the bq78PL114 at inputs CSBAT and CSPACK to provide SmartSafety™ features like short-circuit protection and others. These fast-acting inputs have user-configurable trip-delay-times and consequently do not require any signal filtering.

The choice of sense resistor type has an influence on BMU current measurement performance. The FW4452 permits the use of a 5-mΩ resistor. In FW5000, the value of the sense resistor is programmable by the user over a wide range of values. A ±1% tolerance resistor is recommended for most applications. Also, the resistor's temperature coefficient (ppm/°C) causes the resistance, and consequently the voltage measured, to change as the temperature changes. A resistor with a low-temperature coefficient is less influenced by changes in ambient temperature. System-level calibration of battery current via the bqWizard™ or similar software is then performed prior to use to achieve measurement performance values listed in bq78PL114 data sheet.

3.7 Pack Disconnect Switches and Control

Pack disconnect switches are needed to block battery current in both directions — charge and discharge. The intended circuit topology to do this is two P-channel MOSFETs in a common drain configuration. See Figure 7 for details.

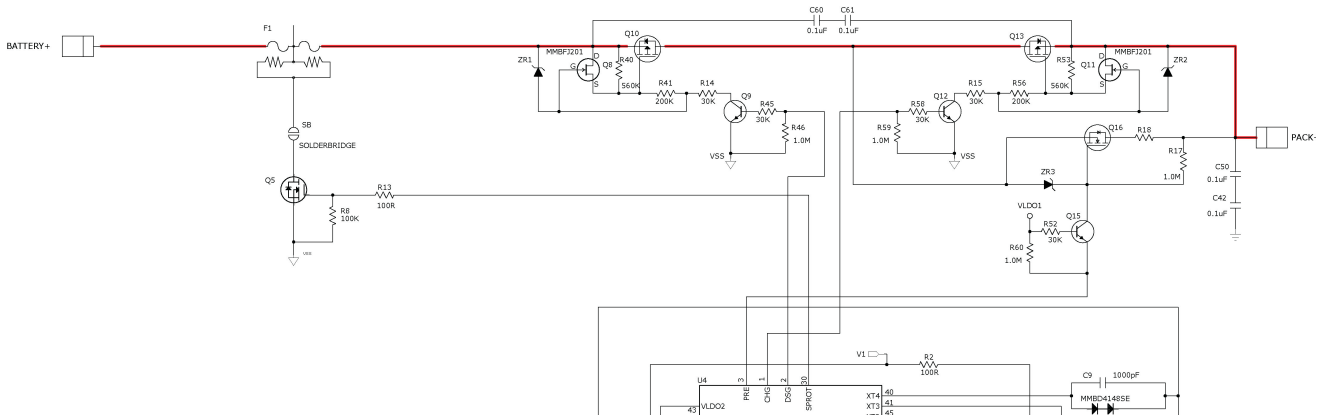

Figure 7. Pack Disconnect Switches

The discharge and charge control switches are discussed first. The precharge switch is discussed later.

A description of how the bq78PL114 controls charge, discharge, and precharge current is shown in Table 1. Logic levels are HIGH = VLDO1 and LOW = VSS. The table shows the logic used to control each state independently. All possible operating states are not shown. For example, a valid operating state occurs where discharge current is allowed to flow, and the charge switch is either HIGH or LOW.

Table 1. Pack Disconnect Control Summary

	DSG (1)	CHG (1)	PRE (1)
Stop Discharge	LOW	X	X
Allow Discharge	HIGH	X	X
Stop Charge	X	LOW	X
Allow Charge	X	HIGH	X
Stop Precharge	X	X	LOW
Allow Precharge	X	X	HIGH

(1) X = May be HIGH or LOW.

Important design criteria for the selection of the switches are series resistance, called R_{DSOn}, power dissipation, and switching time, particularly turnoff time. The power loss in the switch circuit is entirely up to the discretion of the designer. An R_{DSOn} rating of less than 10 mΩ is desirable.

The turnoff time of the discharge switch is of particular importance because it needs to stop fault conditions, like a short circuit, quickly before any damage to the BMU, external equipment, and/or the battery occurs. Because R_{DSOn} is generally inversely proportional to gate capacitance and consequently turnoff time, additional steps were taken in the gate drive circuit to achieve a fast turnoff time. This refers to the use of JFETs Q8 and Q11. This topology can achieve turnoff times in the 10s to 100s of microseconds for MOSFETs having 1000s of picofarads of gate capacitance (Ciss). All of the resistor values can be adjusted away from the nominal values listed to achieve different levels of current consumption and switching performance.

The precharge switch is used to provide a conditioning charge current to a depleted battery. This switch has much lower performance standards when it comes to turnoff time and R_{DSOn} rating compared to the discharge and charge switches. The circuit centered around MOSFET Q16 is controlled by the bq78PL114 to be active up to approximately 3 VDC per cell. After this point, the full-charge current is applied through the charge switch. This performance is user configurable through a programmable parameter (precharge voltage).

A design consideration of the precharge switch circuit is that it be operational when the bq78PL114 is in shutdown mode so that it provides the conditioning charge current specified by the cell manufacturer (typically C/20 to C/10 A). The PRE pin is high Z in shutdown mode. Given the logic of the PRE pin, an N-channel MOSFET was used to achieve this function. It may be necessary, particularly in systems that are four series cells and higher, to add a Zener diode to clamp the voltage across the gate to source terminals of the precharge MOSFET. This can be seen in Figure 7 as the device labeled ZR3. A heavily depleted battery can be at 2 V/cell, whereas the charger voltage is at 4.2 V/cell. The gate-to-source voltage in a 12-series cell system can momentarily be as high as [(4.2 - 2) x 12] = 26.4 VDC. This is typically in excess of the V_{GS} rating of many low-cost N-CH MOSFETs.

The PRE pin is set high to enable precharge. Assuming that the bq78PL114 does not shut off precharge, the gate threshold voltage (Vgsth) of the N-channel MOSFET determines when the device can no longer provide precharge current. For instance, a typical V_{GSth} of 2 VDC means that precharge current is available from a battery voltage from zero up to within 2 V of the charger voltage.

Resistor R18 sets the maximum precharge current. The maximum precharge current occurs when the battery is at zero volts and the charger voltage is applied. Note, it is generally not recommended to let the battery voltage go to zero voltage for any appreciable length of time.

3.8 SPROT (Fuse) Control

The SPROT pin is an active-high output pin that is at the VLDO1 logic level, 2.5 V (see Figure 8). This output is set high when the safety logic of the bq78PL114 determines that a condition(s) exists whereby the best course of action is to permanently disrupt the flow of battery current. The SPROT pin is intended to drive a buffer circuit which in turn activates a chemical fuse, trigger a crowbar circuit, or simply provide a logic signal to another battery power control mechanism. Notice that a solder bridge was added between the fuse and the switch (Q5). This allows circuit testing of the fuse blow circuit in production without actually opening the fuse. After testing is complete, the solder bridge is closed prior to shipment.

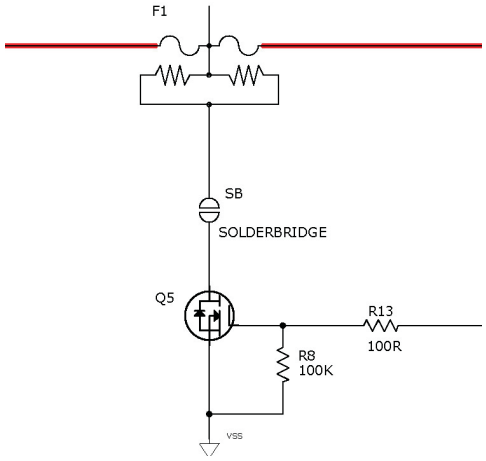

Figure 8. Chemical Fuse Circuit

The chemical or thermal fuse option is commonly available in applications up to maximum voltage of 32 VDC and currents up to 12 A. Higher power applications requiring the ability to activate a fuse need an alternative approach such as using a high-power device (TRIAC perhaps) to crowbar (short-circuit) the battery fuse to disrupt battery current. Details of this circuit are not discussed in this report.

3.9 PowerPump™ Cell Balancing

The Texas Instruments application report *PowerPump™ Balancing* (SLUA524) provides a detailed explanation of the active cell-balancing circuitry. The cell-balancing circuitry in both reference designs is configured to achieve 75 mA to 100 mA of average balancing current. The FW5000 has the ability to make adjustments to the cell-balancing performance through user configuration. The FW4452 is fixed at one level of performance.

Device power for the bq78PL114 and the bq76PL102 is sourced from certain cell voltages within the battery. This creates a current drain on some cells and not others, typically in the 100s of µA during active mode. It is recommended that the PowerPump™ cell balancing be activated in all applications to safeguard against this minor current draw.

3.10 SOCi Display and Pushbutton

The relative state of charge of the pack can be visually indicated to the user if desired. If no display is desired, do not connect to the display-related pins (LED1-5, LEDEN, PSH, BP, TP, and FIELD). The SOCi (State of Charge indication) display is commonly implemented using five LEDs. The bq78PL114S12 can support a segmented LCD or a segmented EPD. In the case of the LED display, a pushbutton is used to activate the LEDs. The LCD and EPD do not use the pushbutton to activate the display.

3.11 Pushbutton/LED Enable (Pin 31)

Operation of pin 31 depends on the firmware installed in the bq78PL114. In the case of the FW5000 for bq78PL114S12, this pin is a straight-forward, active-low pushbutton input. When it is pressed, the SOCi LEDs illuminate to show state of charge.

In the case of the bq78PL114 with FW4452, this pin has two uses. First, it is a capacitively sensed, active-low pushbutton input to activate the SOCi LED display. Capacitor C4 in Figure 9 must be 0.1 µF for proper operation of the circuit. Second, it is an LED enable output that is held high (VLDO1 level) to shut off transistors Q14 and Q17 and consequently any LED indication during temperature measurements. Temperature measurements occur approximately every second. Without the LEDEN function, LED1 and LED2 blink during temperature measurements. Temperature multiplexing in the bq78PL114 (FW4452) is explained in the temperature sensor subcircuit section that follows.

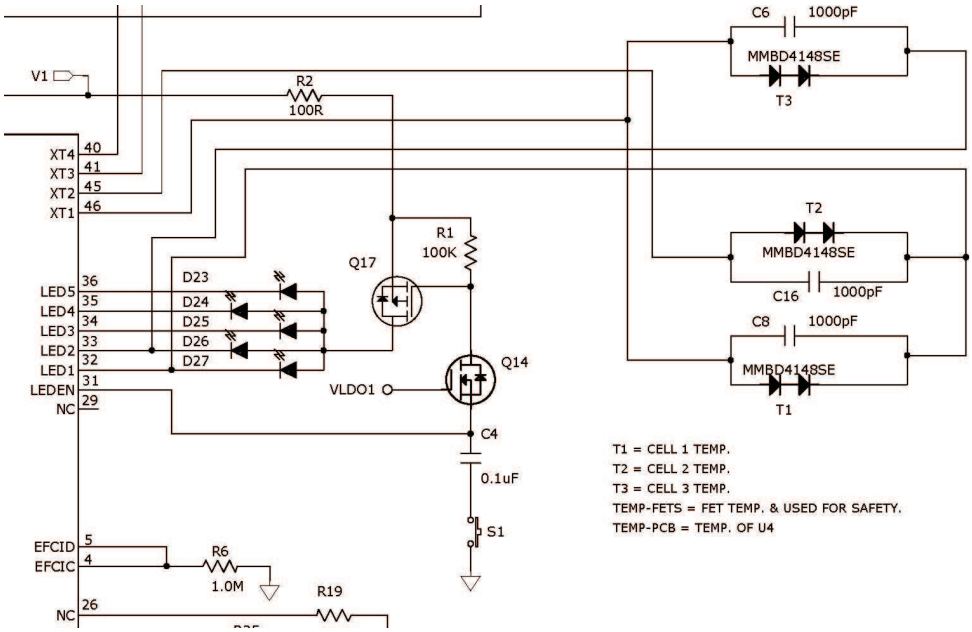

Figure 9. Pushbutton Circuit and LED SOCi Display for bq78PL114 With FW4452

3.12 LEDs

The state of charge of the pack (SOCi) is available on the five LED pins. Each pin is an open-drain output that is current limited. Each LED output is pulled to ground to illuminate the LED connected to it. Depending on the aesthetic requirements of the application, a common anode current-limiting resistor, like R2 shown in Figure 9, may be needed to reduce the brightness of the LEDs. The LED pins can tolerate up to 5 V, so powering the LEDs from cell 1 voltage affords a low component-count solution.

The LED SOCi display circuit for the FW5000 is shown in Figure 10. The LED pins and pin 31 are single purpose and require fewer parts to implement the SOCi and temperature sensor functions.

3.13 LCD

For details on the LCD option in the bq78PL114S12, see the bq78PL114 data sheet (SLUS850) and technical reference manual (SLUU330), or contact Texas Instruments application support for assistance.

3.14 EPD

For details on the EPD option in the bq78PL114S12, see the bq78PL114 data sheet and technical reference manual, or contact Texas Instruments application support for assistance.

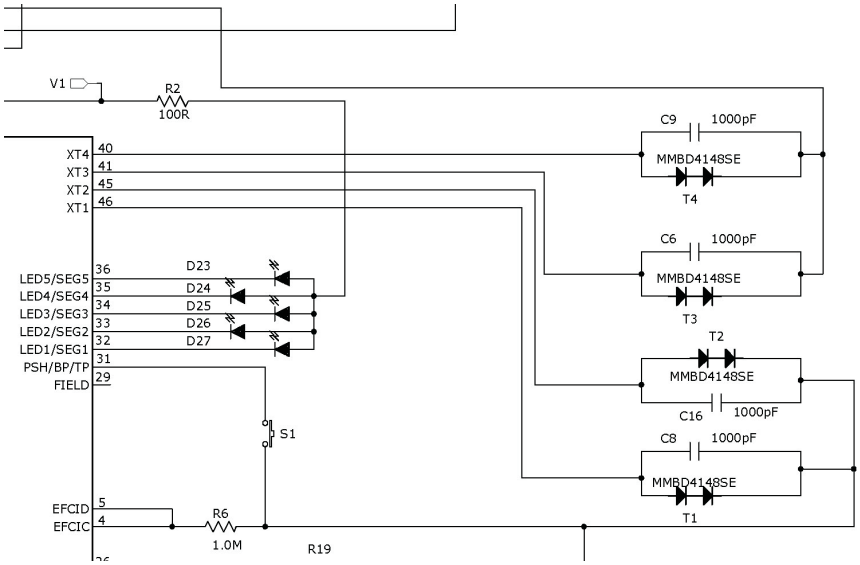

Figure 10. LED-Based SOCi Indicator Circuit Using bq78PL114S12 With FW5000

3.15 Temperature Sensors

The circuit design for the two versions of the bq78PL114 relating to the temperature sensors are different. Default temperature sensor configurations for FW4452 and FW5000 are summarized in the Table 2.

Table 2. Temperature Sensor Mapping

Temperatures	FW4452 bq78PL114 Anode / Cathode	FW5000 bq78PL114S12 Anode / Cathode
Cell 1	XT1 / LED1	XT1 / VSS
Cell 2	XT2 / LED1	XT2 / VSS
Cell 3	XT1 / LED2	XT3 / V2
Cell 4	XT2 / LED2	XT4 / V2
Device	XT3 / V2	Internal
BMU PCB	XT4 / V2	Internal

FW4452 in the bq78PL114 does not use the internal temperature sensor for device and PCB temperature monitoring. Consequently, it dedicates XT3 and XT4 to those functions and multiplexes the four cell temperatures with the LED1 and LED2 functions. Temperature sensor mapping is fixed in FW4452 and is user configurable in FW5000. For instance, FW5000 allows all temperature measurement mappings to be assigned to the single internal sensor for a reduced part count solution.

Figure 11 shows a side-by-side comparison of the two temperature sensor circuits. Temperature sensor/LED multiplexing is on the left.

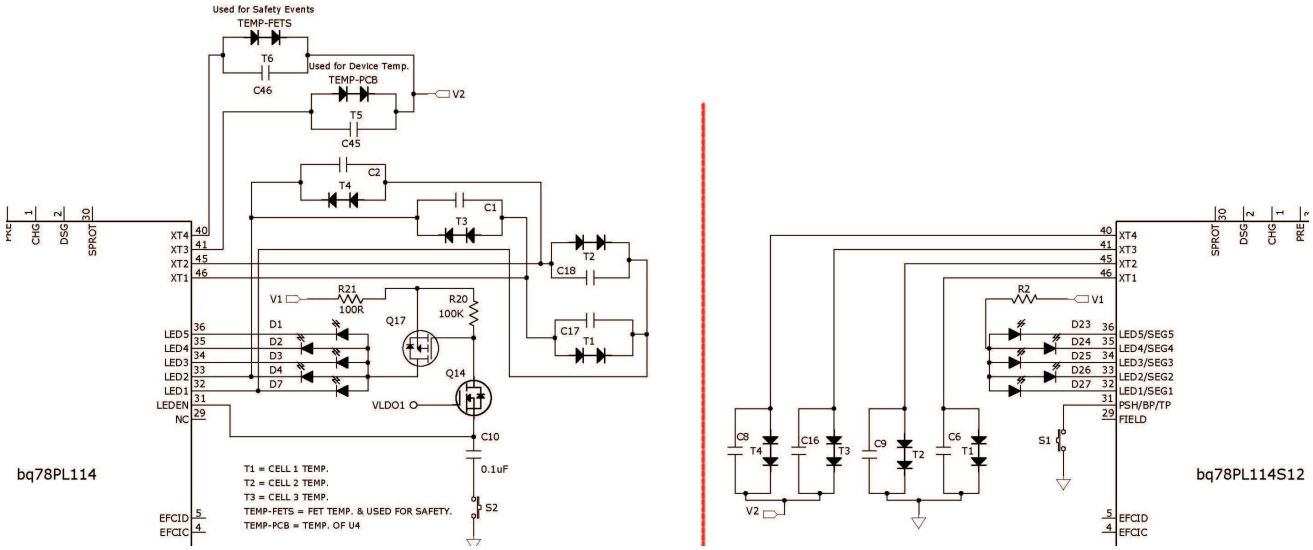

Figure 11. Temperature Sensor Multiplexing vs Nonmultiplexing (S12)

3.16 SMBus

The SMBus interface is used to communicate with a host device in a smart battery style implementation during normal operation. It is also used to configure the device during production and download firmware in the case of the bq78PL114S12. The Zener diode and series resistance on each pin is intended for ESD protection if the connector is going to be exposed in the application.

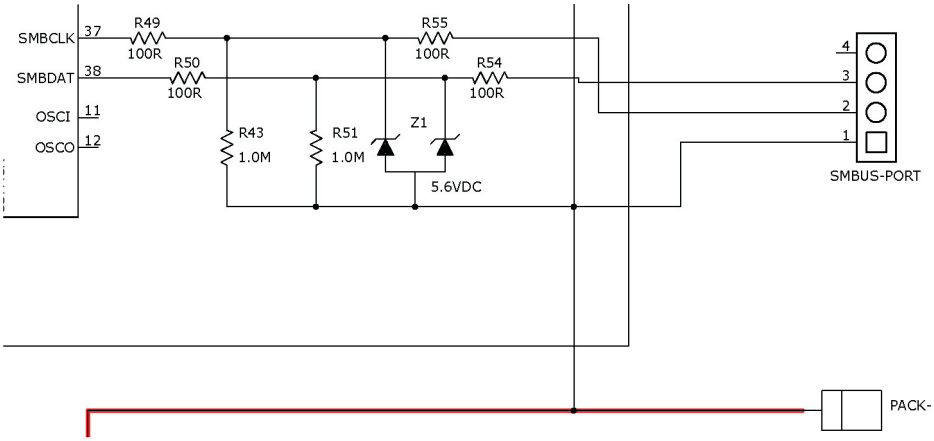

Figure 12. SMBus Interface Circuit

3.17 External FET Control Interface (EFCIx)

The EFCIx pins (EFCID, EFCIC) are inputs that allow the host system to override the status of the pack disconnect switch control pins CHG and DSG. The signal polarity for these pins is user configurable via a control register. Figure 13 shows a recommended design for the active-high polarity setting. The Zener diode and series resistance on each pin is intended for ESD protection if the connector is going to be exposed in the application. These inputs also may be used during production testing to verify operation of the pack disconnect switches. A single, high-value resistor must be used to pull down both pins when not in use.

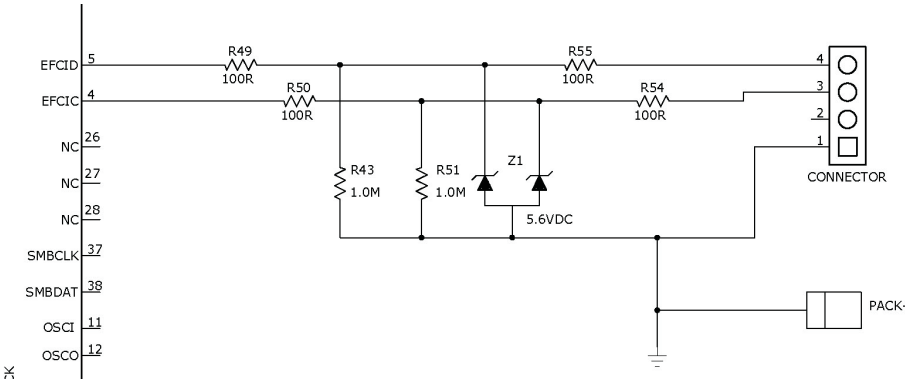

Figure 13. EFCIx Interface Circuit

3.18 ESD/Transient Protection

ESD protection capacitors are located in two areas of the BMU circuit. The purpose of the capacitors in both cases is to route ESD pulses to the high capacitance of the battery to be attenuated. First, two series capacitors are located differentially across the PACK+ and PACK– connections. Second, two series capacitors are located in parallel to the pack disconnect switches. A pair of series capacitors is used in place of a single capacitor to avoid a single fault possibility.

The level of ESD protection required varies based on application. In general, any pin of the bq78PL114 that may be exposed to ESD pulses from the outside must have some level of protection beyond the intrinsic protection of the device.

4 Printed-Circuit Board Layout Recommendations

The typical PCB layout for portable power applications requires high density and high performance at a minimum cost. The following PCB layout guidelines can assist in achieving these goals. The underlying layout design goals are:

- Separate the noisy, high-power signals from the critical µA/mV precision signals of the measurement system.
- Establish a star ground for VSS that minimizes the noise of the system ground (GND).
- Provide sufficient thermal dissipation for power components.
- Use techniques that minimize the affects of ESD strikes.

The PCB layout figures consist of partially or incrementally laid-out circuits. The intention of each figure is to demonstrate one or more layout recommendations. The conclusion of the report shows a completed layout that demonstrates the recommendations.

4.1 Introduction

The BMU circuit contains precision measurement circuitry, high-current disconnect switches, and high-frequency switching circuits for PowerPump™ cell balancing. A four-layer PCB construction is generally recommended for most applications to ensure signal integrity. The two additional layers are usually reserved for large copper planes that can be used for VSS, cell voltages, and passing battery current. Each application dictates the circuit density required, and this has an impact on the number of copper layers used.

The QFN-48 package of the bq78PL114 has a center-to-center 0,5-mm pin spacing, approximately 20 mils. Many of the signal levels in the bq78PL114 operate differentially at 5 V or less. Because designs can go up to 12 cells in series, or over 50 VDC, care must be taken to identify and group the different nets by voltage level and assign appropriate clearances and widths to each.

4.2 Single-Point BMU Ground Scheme (VSS)

The ground of the bq78PL114 BMU is called VSS. The PCB layout must be set up so that all VSS signals return to a single point via a star ground configuration. The location of the star point on the PCB is where the reference to cell 1 enters the board; see Figure 14. This figure has a portion of the layout obscured to focus attention on the area under discussion. VSS enters the PCB at the fifth terminal of the connector labeled CELLS.

Note that the VSS copper plane (green color) does not extend all over the PCB. It is only in areas where circuitry is referenced to VSS. The VSS plane is purposefully separated from the high-current path of the system ground net and away from the BATTERY+ net. The PowerPump™ balancing circuitry is located close to the VSS star ground so that any switching noise and pumping current can be quickly routed to VSS and off the PCB.

Table 3. PCB Layer Colors

Design Layer	Color
Top Side (1)	Red
Internal Layer 1 (2)	Green
Internal Layer 2 (3)	Grey
Bottom Side (4)	Blue
Top Silkscreen	Black
Board Outline	Green

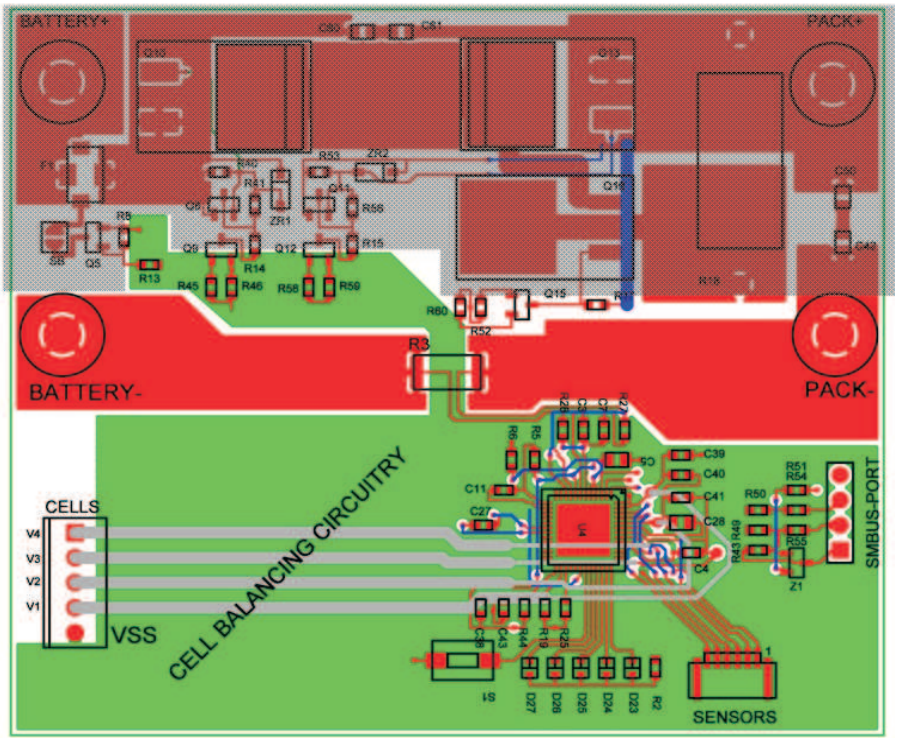

Figure 14. VSS Star Ground and Internal Copper Plane

4.3 VLDO1, VLDO2, and RSTN Nets

The VLDO1, VLDO2, and RSTN nets must be kept local to the bq78PL114. Although VLDO1 and VLDO2 are considered a VDD-like net, it is not recommended to devote a large copper plane to them. Keeping these nets and their decoupling capacitors as close as possible to the bq78PL114 and using at least 10-mil to 20-mil trace widths up to the pins is all that is required.

The RSTN net controls the device reset. As such, avoid routing this signal and its filter capacitor far from the bq78PL114. See Figure 14 for details that show how all of the ancillary components are kept close to the bq78PL114 to support short-trace lengths.

4.4 PowerLAN™ Signals

In this design, the PowerLAN™ signals (SDIx, SDOx, and PLAN) are local to the bq78PL114 because it is only a four-cell system. Bus capacitance is not a problem because signal paths are close to the bq78PL114. When larger series cell count systems are developed, care must be taken to not introduce too much distributed capacitance on the communication bus. Designs must avoid creating bus capacitance between devices, bq78PL114 and bq76PL102, that create in excess of 100 pF of load capacitance.

4.5 Current Sense Circuit Layout

Figure 15 shows the recommended method to connect the bq78PL114 current sense circuitry to the sense resistor R3. Notice that the two signal lines from R28 and R27 connect to R3 on the inside of the SMD pads. This is also referred to as a Kelvin connection – like the cell tab connections for cell voltage measurement. This connection has virtually no additional voltage drop due to load current running through PCB copper.

Consider that a 1-oz ounce copper PCB has a resistance per square mil of approximately 0.5 mΩ. So, with a load current of 30 A, a sense resistor of 1 mΩ and 1 square mil of copper added to the resistance of the resistor, the current reading can be as high 45 A, instead of 30 A. System level calibration of the current measurement circuit, through the bqWizard™ or similar software, is a regular part of BMU preparation. Although this can calibrate out copper resistance, it is still a highly recommended practice to use a Kelvin connection for current sense.

The signal paths for the two current sense traces (CCBATT and CCPACK) must run parallel to each other so that they create the smallest loop area. This minimizes the susceptibility to radiated noise coupling onto this millivolt level signal.

The CSPACK and CSBATT signals that measure current for the SmartSafety™ features must also create a minimum loop area when routed. It is best to have the CSBATT and CSPACK signals intersect the CCBATT and CCPACK signals just after the 4.7-kΩ resistors (R27 and R28), rather than tracking four traces all the way to the sense resistor R3.

Although CSPACK is really the system ground (GND), it is to be routed as shown in Figure 15. Do not connect any other GND trace to the trace that connects CSPACK to the GND side of R3. The reason is that any current flowing in the CSPACK trace can show up as an error in the current reading made between CSPACK and CSBATT.

Lastly, the high-current loop formed by the pathway from BATTERY± to PACK± is designed so that it does not encompass the bq78PL114. This is accomplished by positioning the sense resistor R3 and its connections to BATTERY– and PACK– above the bq78PL114 circuitry.

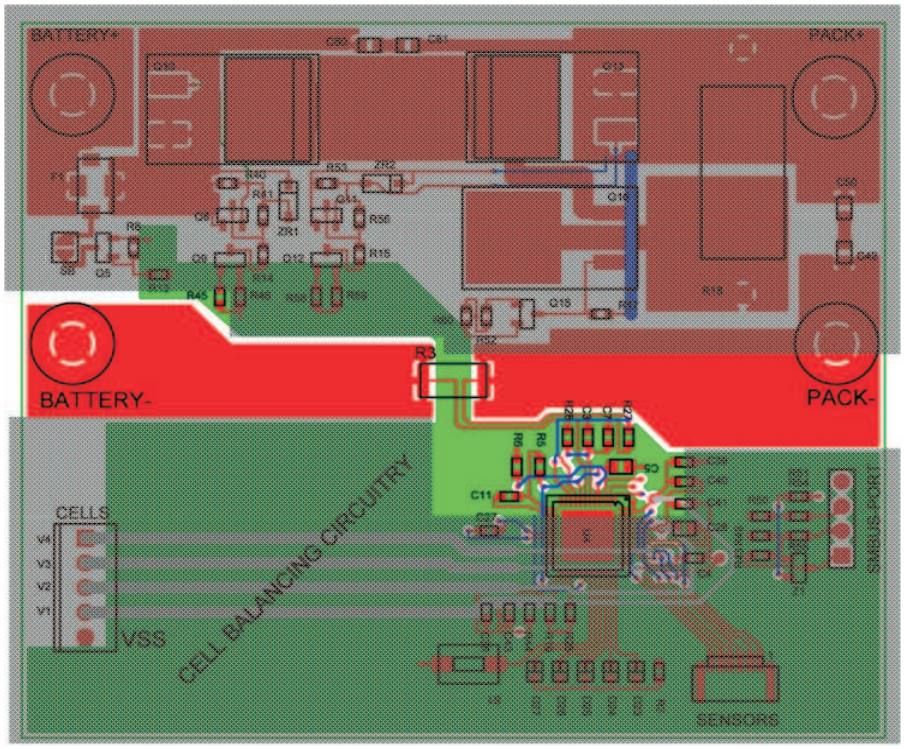

Figure 15. Layout of Current Sense Resistor and Sense Signal Lines (CCBAT, CCPACK, etc.)

4.6 System (Pack) Ground Reference (GND)

The System Ground net (GND) carries battery current and is the system-side reference for signals like SMBus and EFCIx. The connection to this net is commonly called PACK–. Minimizing impedance of this net results in low heat generation and a lower voltage drop from battery to system. This net is one of the primary nets used to direct ESD pulses away from the sensitive measurement circuitry to either the battery or back into the host system for dissipation. See Figure 15 to see how the GND net is routed from the sense resistor R3 to the PACK– connector.

4.7 Cell Voltages

The cell voltages are monitored by the bq78PL114 and also used to power the device. The connection of V1, V2, V3, and V4 to the device must be low impedance. See Figure 14 for an example of direct routing of these cell voltages to the bq78PL114. Later, these traces are adjusted to accommodate the PowerPump™ balancing circuitry. Measurement of cell voltages and temperatures and PowerPump™ cell balancing occur during mutually exclusive intervals. Cell balancing currents can be run on the same path as the V1–V4 input signals as a result and permits denser system designs.

4.8 Temperature Sensor Layout and Routing

Each temperature sensor signal pair, for instance XT1 and VSS, must be routed so that they enclose the minimum loop area. See Figure 16 for a close up of this signal routing. This minimizes the susceptibility to radiated noise signals generated elsewhere in the system. The designer must determine if the VSS ground plane is sufficient to act as the return path for the XT1 and XT2 currents or if separate VSS traces must be created to run alongside of the XT1 and XT2 signals to act as a shield.

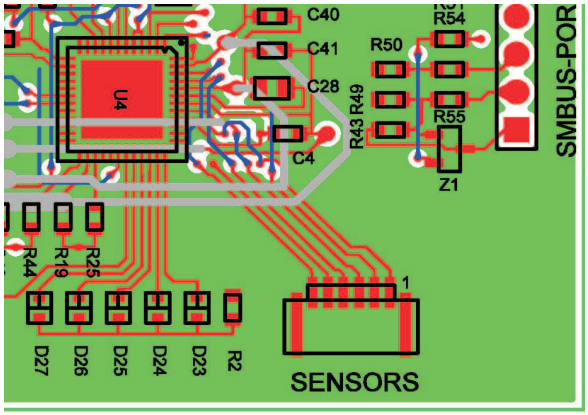

Figure 16. Layout of Temperature Sensor Signals

The XT3 and XT4 signals are returned through the V2 net. These must have a separate, parallel V2 return trace flanking them because it is unlikely that a significant V2 copper plane is on the BMU PCB to act as the return path. As shown in Figure 16, the V2 return for XT3 and XT4 travels alongside these signals and terminates at the local V2 connection of the bq78PL114, not back at the CELLS connector.

These techniques also hold for any remote sensors that may be designed using discrete wires, flexible PCB or rigid PCB.

4.9 PowerPump™ Cell-Balancing Circuitry

The PowerPump™ balancing circuitry is added to the layout. Figure 17 shows each layer of the layout, excluding the pack disconnect circuit section. Some adjustments to temperature sensor routing, VSS copper planes, and cell voltage signal routing to the bq78PL114 were made from above. Copper pours were created for each cell voltage to reduce signal path impedance in the balancing circuit.

Table 4. Cell Voltage Net Colors of Figure 17

Circuit Net	Color
VSS	Green
V1	Light Blue
V2	Grey
V3	Purple
V4	Brown

PCB layout of the PowerPump™ cell-balancing circuitry must follow the same rules that apply to typical high-frequency switching power converter circuits. The pulse-width modulated circuit signals have square edges and consequently have high-frequency components. The inductor signals in particular carry peak currents that are many times higher than the average pumping current. Peak inductor currents depend on the inductor value.

To minimize the generation of noise and make the circuit as efficient as possible, the PowerPump™ circuit components must be placed and routed so that the loop area created by the inductor, capacitor, and transistor signal loop is as small as possible. The widest possible traces must be used to minimize voltage drop. The best method of connecting the cell voltages to the PowerPump™ circuit is through a wide copper plane, on inner or outer layers, that is local to the MOSFET/inductor/capacitor current loop. This is demonstrated in Figure 17.

The PowerPump™ control signals, P1N, P2S, P3S, P3N, and P4S, must have the shortest possible path to the gate of their respective MOSFET. The return path for the control signal is best accomplished using a copper plane connected to the signal reference. The reference for P1N, P2S, and P2N is VSS. The reference for P3S, P3N, and P4S is V2.

Heat dissipation in this circuit is generally not a concern due to the use of the high-frequency switching topology and low on-resistance MOSFETs. As an example, a MOSFET with an R_{DSon} of 0.25 Ω and junction-to-ambient resistance of 130°C/W operating at average current of 0.250 A only has a temperature rise of a few degrees. The high efficiency/low heat dissipation of this cell-balancing circuit, compared to an equivalent resistive bleed balancing circuit, supports a very dense layout. This is an advantage in high cell-count systems.

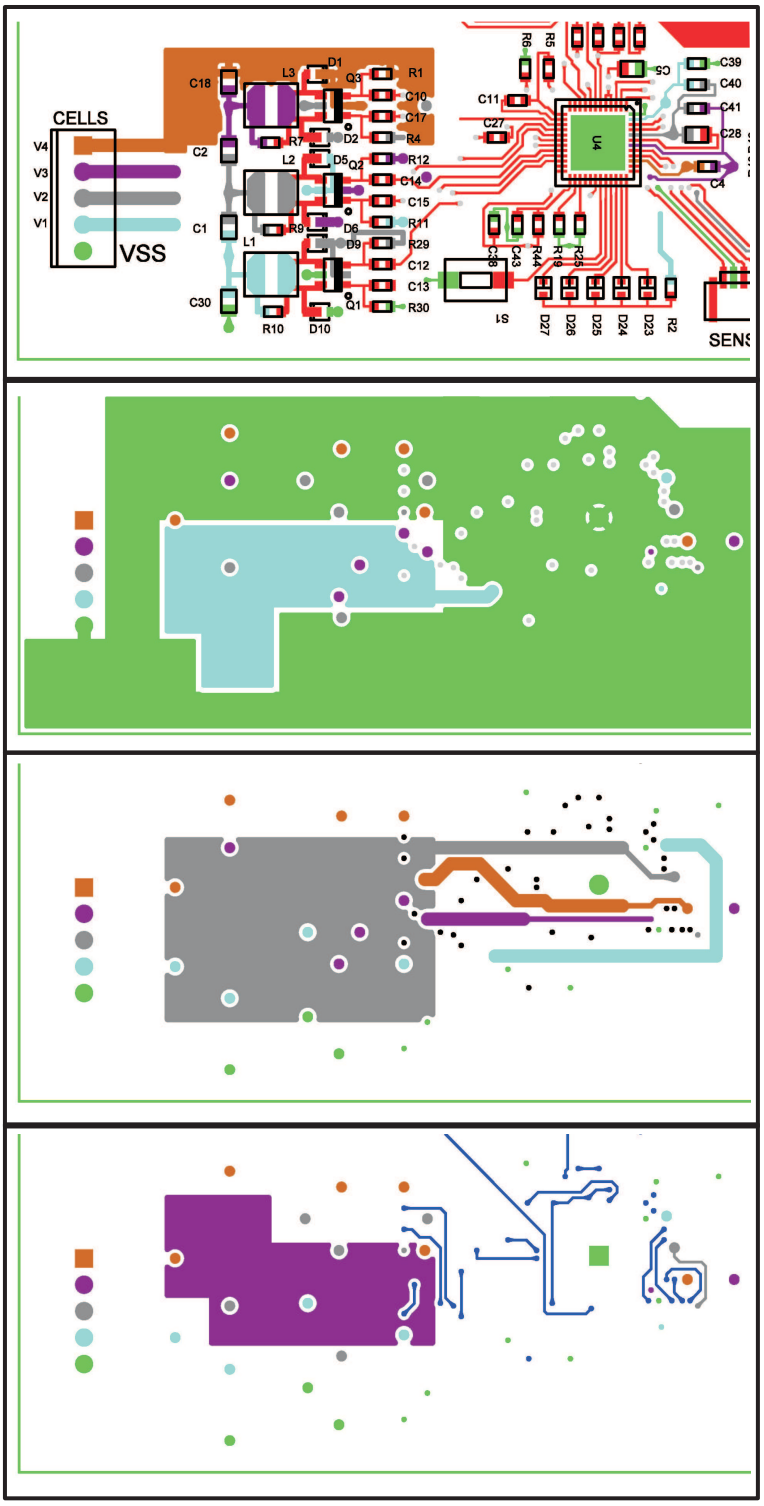

Figure 17. Top, Inner 1, Inner 2, and Bottom Layers With PowerPump™ Circuit Added

4.10 Pack Connections to BMU

Connections of BATTERY+, BATTERY–, PACK+, and PACK– to the BMU must be substantial. The typical connection rating needs to continually pass tens of amperes (if not more) with a low voltage drop and low heat dissipation. A common technique is to solder the wire or strap directly to the PCB and then to have two or more copper planes connect to the connection point. These connections, if positioned near the pack disconnect switches, can be used to pull heat away from the MOSFETs.

4.11 Pack Disconnect Switches

Because the pack disconnect switches carry battery current, they obviously need to be laid out to minimize impedance. Any impedance diminishes pack efficiency by reducing run time under load. Figure 18 through Figure 22 show a completed layout that incorporates the Pack Disconnect switches (MOSFETs).

The power path through MOSFETs Q10 and Q13 shows the use of copper pours on multiple layers to carry current at low impedance. Stitching vias were used to link the layers together. This provides a robust connection of the various parallel copper layers. Most designs require the maximum use of board area to carry battery current.

4.12 Bypass Capacitors

Bypass capacitors C60, C61, C50, and C42 are used to send energy from noise pulses, either ESD or load transients, around the BMU circuitry and to either system ground or to the battery for attenuation. C60 and C61 are across the MOSFETs, and C50 and C42 are across the PACK connection. Physical location and layout of these capacitors is important. Any impedance reduces the effectiveness of the capacitors. Use wide copper traces or copper planes to rout these capacitors. For example, C42 is connected to GND through a copper plane on the bottom layer. See Figure 21 for details of this example.

4.13 Conclusions

NOTE: It is important to note that this application report uses PCB layout figures that were created for instructional purposes. The fabrication of a physical printed-circuit board was not performed. The design practices and recommendations herein have been successfully implemented in other similar BMU designs.

The bq78PL114 BMU layout was presented as a progression to clearly show certain layout techniques without presenting the reader with multiple layers and traces all at once. Note that some of the design features of the earlier figures changed in the final layout. The following summary lists some of the changes.

- Connection between R3 and BATTERY – connection shown in Figure 14 was improved with an identical copper plane on all layers. These were connected with a field of stitching vias to maximize effectiveness of parallel planes.
- Connection between R3 and PACK- (GND) connection shown in Figure 14 was improved with an identical copper plane on all layers. These were connected with a field of stitching vias to maximize effectiveness of parallel planes.
- The direct traces for cell voltage connections from the CELLS connector to the bq78PL114 were changed after the PowerPump™ circuitry was added and routed. All four layers were used to create copper areas for each voltage. These copper areas reduced signal net impedances throughout the balancing circuit as well as maintaining the connection requirements to the bq78PL114.
- The VSS copper plane was pulled back from underneath the balancing circuitry to allow room for the cell voltage copper areas.
- Note that the QFN-48 PCB decal of the bq78PL114 has a single oversized via in the center pad to connect the device to the VSS copper plane. The via was made large to provide a convenient method for removing the device with a soldering iron tip if damage occurred during experimentation, as well as a means to re-solder the center pad without using reflow techniques. This large size via is recommended only in the prototype design stage. The center pad is primarily used to provide a

connection to VSS, not for thermal dissipation. One standard via in the center of the pad is sufficient to connect the device to VSS. A via diameter of 0.008 inch reduces the instances of solder paste from being drawn through the via.

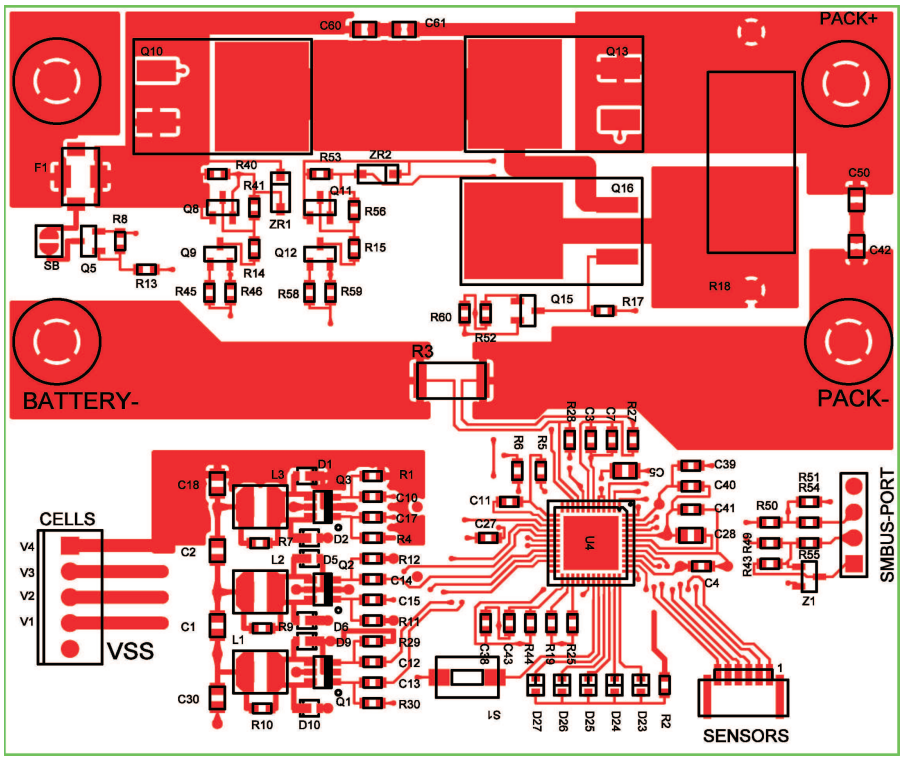

Figure 18. Top Layer of Finished Design

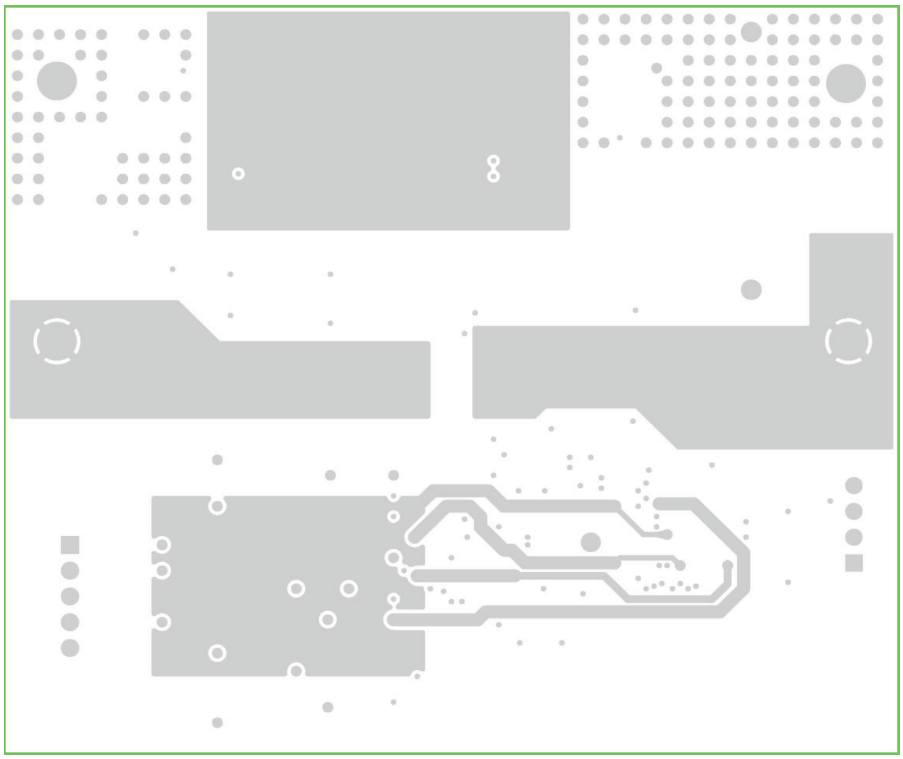

Figure 19. Inner Layer 1 of Finished Design

Figure 20. Inner Layer 2 of Finished Design

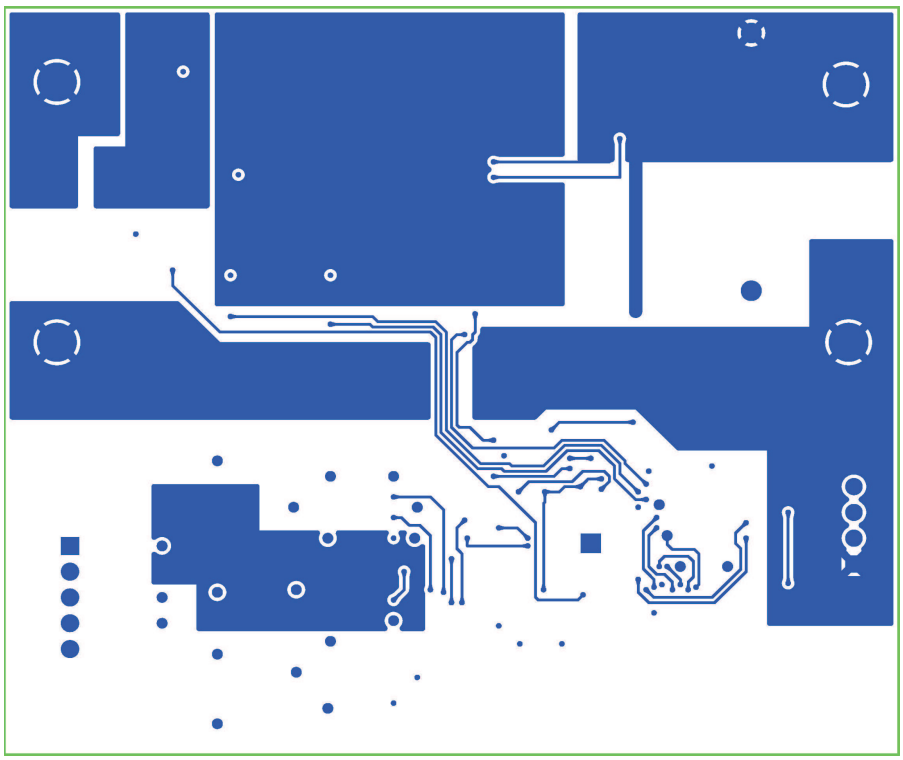

Figure 21. Bottom Layer of Finished Design

SIZE	QTY	SYM	PLATED	TOL
0.05	1		YES	+/−0.003
0.02	378		YES	+/−0.003
0.1	4		YES	+/−0.003
0.039	4		YES	+/−0.003
0.045	2	A	YES	+/−0.003
0.04331	5	B	YES	+/−0.003
0.01	73	C	YES	+/−0.003

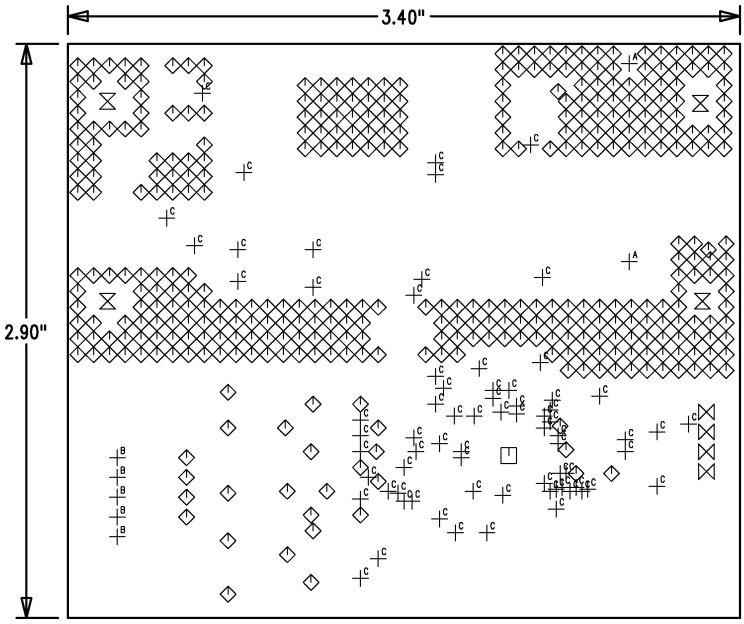

Figure 22. Drill Drawing

5 References

Related product documentation follows:

1. *PowerLAN™ Master Gateway Battery Management Controller with PowerPump™ Cell Balancing Technology* data sheet (SLUS850).
2. *PowerPump™ Balancing* application report (SLUA524).
3. *bq78PL114 and bq78PL114S12 Technical Reference Manual* (SLUU330)
4. *bq78PL114 8S EVM* user's guide (SLUU335).
5. *PowerLAN Dual-Cell Li-Ion Battery Monitor With PowerPump™ Cell Balancing* data sheet (SLUS887)
6. *Avoiding ESD and EMI Problems in bq20zxx Battery Pack Electronics* application report (SLUA368).
7. *QFN Layout Guidelines* application report (SLOA122)

Appendix A Reference Design Schematics

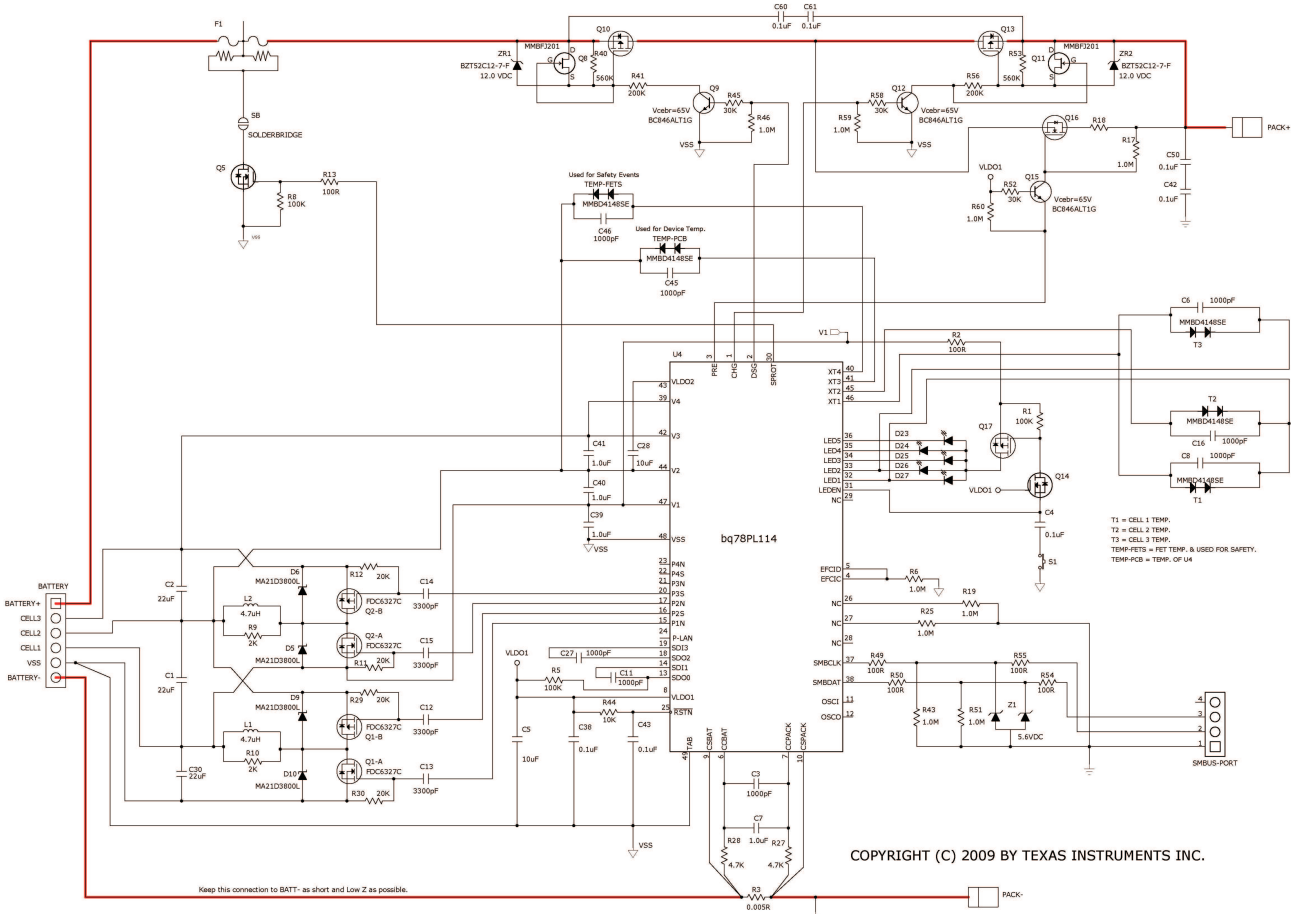

Figure 23. Reference Design With Three Series Cells and FW4452

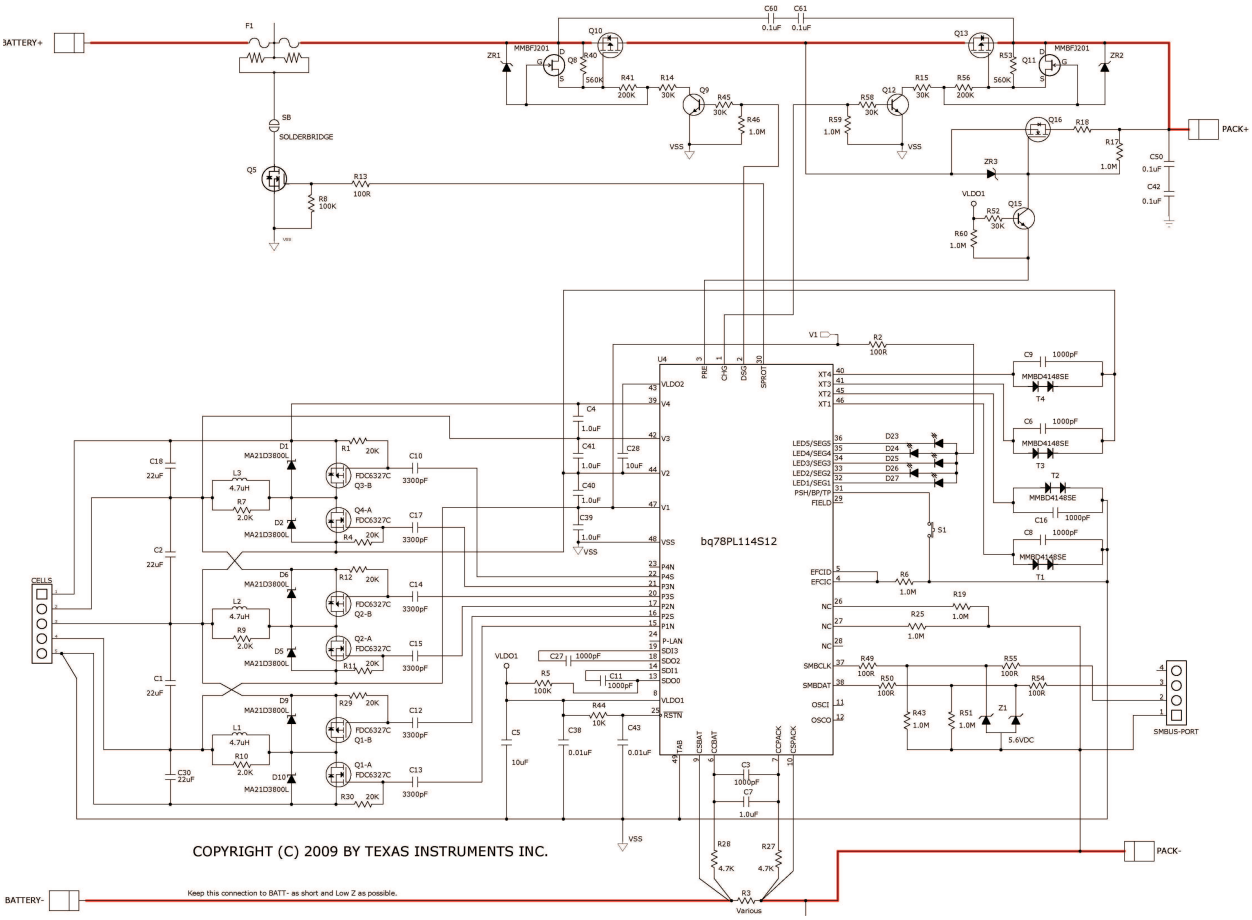

Figure 24. Reference Design With Four Cells and bq78PL114S12 (FW5000)

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