Application Report
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PowerPump™ Balancing

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ABSTRACT

Pack based charging and discharging schemes cannot fully address the problems associated with capacity imbalance of the series cells. Balancing at the cell level is needed to maximize pack performance. PowerPump™ Cell Balancing is a feature provided in the bq78PL114 and bq76PL102 PowerLAN™ devices that transfers charge between cells using a boost-type power converter topology. Results are faster and heat generation far less than traditional resistor bleed balancing. This document discusses the PowerPump cell balancing operation and application circuit design.

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1 Introduction

Lithium-ion battery packs consist of cells connected in series and parallel, typically. The packs are charged with a constant voltage and under some current limit. For example, a 4 series-2 parallel pack (4S2P) would typically be charged at 16.8 V at a 3-A limit. Cell voltage imbalance in lithium-ion battery packs can cause a charger to shut off before all cells are fully and equally charged. Likewise, during discharge, a cell voltage imbalance could cause a battery's run time to terminate early. This is due to the common use of a Pack Under voltage cutoff to stop battery current flow. Pack-based charging and discharging cannot address the problems associated with an imbalance of the series cell voltages.

The effect of cell imbalance is analogous to a chain only being as strong as its weakest link. Cells can in time become imbalanced due to a variety of reasons. For example, high-density packaging requirements coupled with high-performance electronics could cause a temperature gradient across a battery pack. If the host electronics are run from line power for extended periods of time, the hotter cells in the battery self-discharge at a higher rate than the lower-temperature cells. This could result in cell imbalance as the higher voltage cells, not in need of charging, receive the same charge current as the lower voltage cells because the cumulative Pack Voltage is low. When the higher voltage cells cause the constant voltage charger to stop, the lower cells are left at a diminished capacity. Cell imbalance can also occur naturally over time due to manufacturing inconsistencies from cell to cell.

The advanced PowerPump cell balancing system in the PowerLAN lithium-ion battery-management products safeguards against cell imbalance. A typical PowerLAN lithium-ion battery-management system consists of one bq78PL114 master gateway controller and possibly one or more bq76PL102 dual-cell monitoring devices. The bq78PL114 is used for three or four series cell packs and the bq78PL114 and one or more bq76PL102 would be used if the pack size is over four series cells. The control of PowerPump cell balancing resides in the bq78PL114. Both devices contain PowerPump circuits for each cell connected – the bq78PL114 contains four PowerPump circuits and the bq76PL102 contains two. PowerPump device hardware and external components allow each cell to pump north or south to the other cells in the battery.

A block diagram example of an eight series cell PowerLAN battery-management system with one bq78PL114 and two bq76PL102s is shown in Figure 1. The circuit used as the basis for this discussion is shown in Figure 2. This circuit represents the bq76PL102 (U1) and attached PowerPump circuit block shown in Figure 1. This detailed circuit drawing is referred to as a PowerLAN *node*. The bulk of the discussion focuses on the PowerPump circuit within each PowerLAN node. This can be applied to any pack size that is within the limitations of the PowerLAN devices.

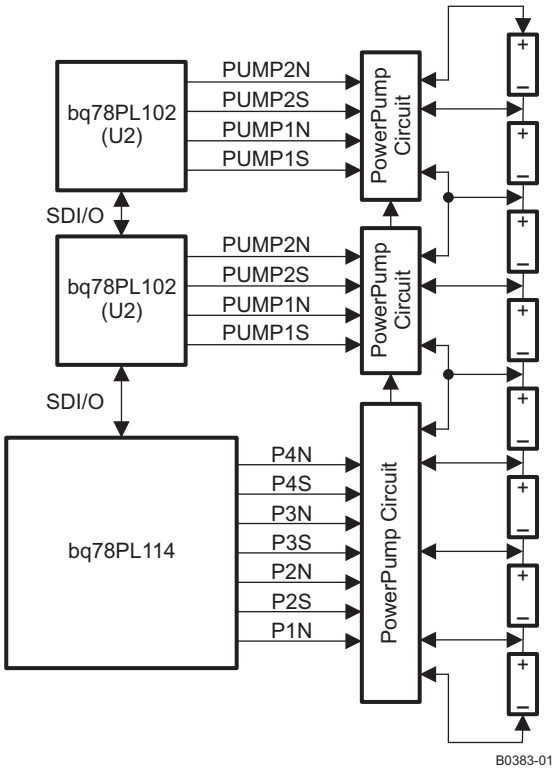

Figure 1. PowerLAN Eight Cell Battery Management Block Diagram With PowerPump Balancing

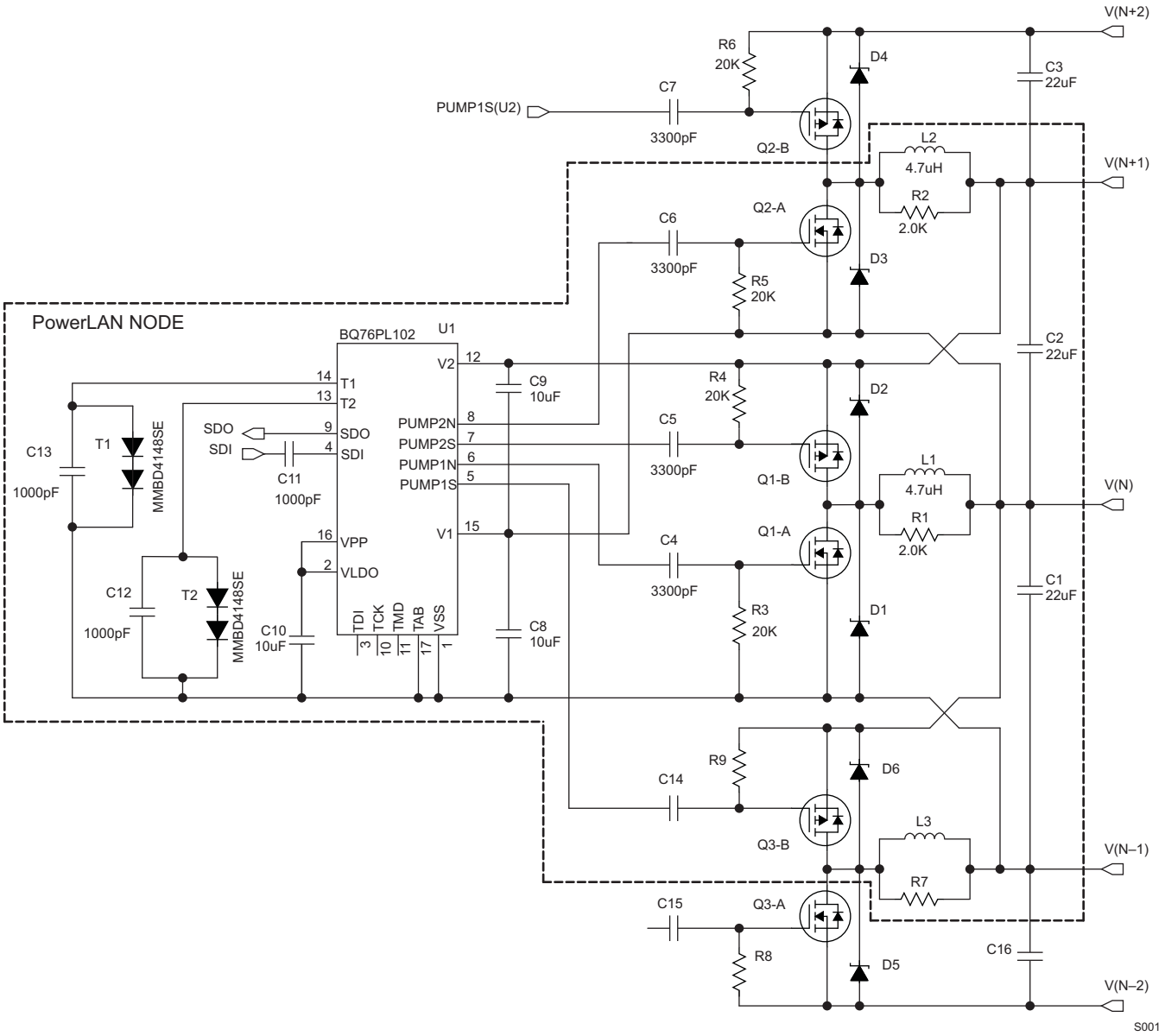

Figure 2. bq76PL102 PowerLAN Dual-Cell Battery-Monitor Circuit

2 Balancing Signal Descriptions

The PowerPump balancing control signals, called PUMPxy in the bq76PL102 and Pxy in the bq78PL114, are designed to pulse width modulate (PWM) the gate of either an external N-channel or P-channel MOSFET, through a level-shifting series capacitor. x = cell numbers 1 or 2 and y = direction N(orth) or S(outh). These MOSFETs act in pairs to control the flow of charge of each cell *north* or *south*. North is the direction towards the top of the cell stack and south is in the direction of battery ground. For example, PUMP2S causes charge from cell two to flow South to cell 1. How charge is shuttled from cell to cell using an inductor is described later.

The electrical characteristics of the PowerPump control signals are summarized in Table 1.

Table 1. PowerPump Electrical Characteristics (for bq76PL102)

DESCRIPTION	PARAMETER	MIN	TYP	MAX	UNITS
Cell voltages	V1, V2	2.5	3.6	4.7	V
PUMP1S, PUMP2S high drive	V_{OH} (I_{OUT} = 10 µA)	0.9 V1			V
PUMP1S, PUMP2S low drive	V_{OL} (I_{OUT} = –200 µA)			0.1 V1	V
PUMP1N, PUMP2N high drive	V_{OH} (I_{OUT} = 200 µA)	0.9 V1			V
PUMP1N, PUMP2N low drive	V_{OL} (I_{OUT} = –10 µA)			0.1 V1	V
PUMP1S, PUMP2S source current	I_{OH} (V_{OH} = V1 – 0.8 V)	250			µA
PUMP1N, PUMP2N sink current	I_{OL} (V_{OH} = V1 + 0.2 V)	–250			µA
Signal rise time	C_{Load} = 300 pF			100	ns
Signal FET fall time	C_{Load} = 300 pF			100	ns
Frequency	f_P		204.8		kHz
PWM duty cycle	D				
	PUMP1S, PUMP2S		67%		
	PUMP1N, PUMP2N		33%		

The frequency and duty cycle of each pump gate drive signal is set by the bq78PL114. Oscilloscope plots of typical bq76PL102 PowerPump signals are shown in Figure 3.

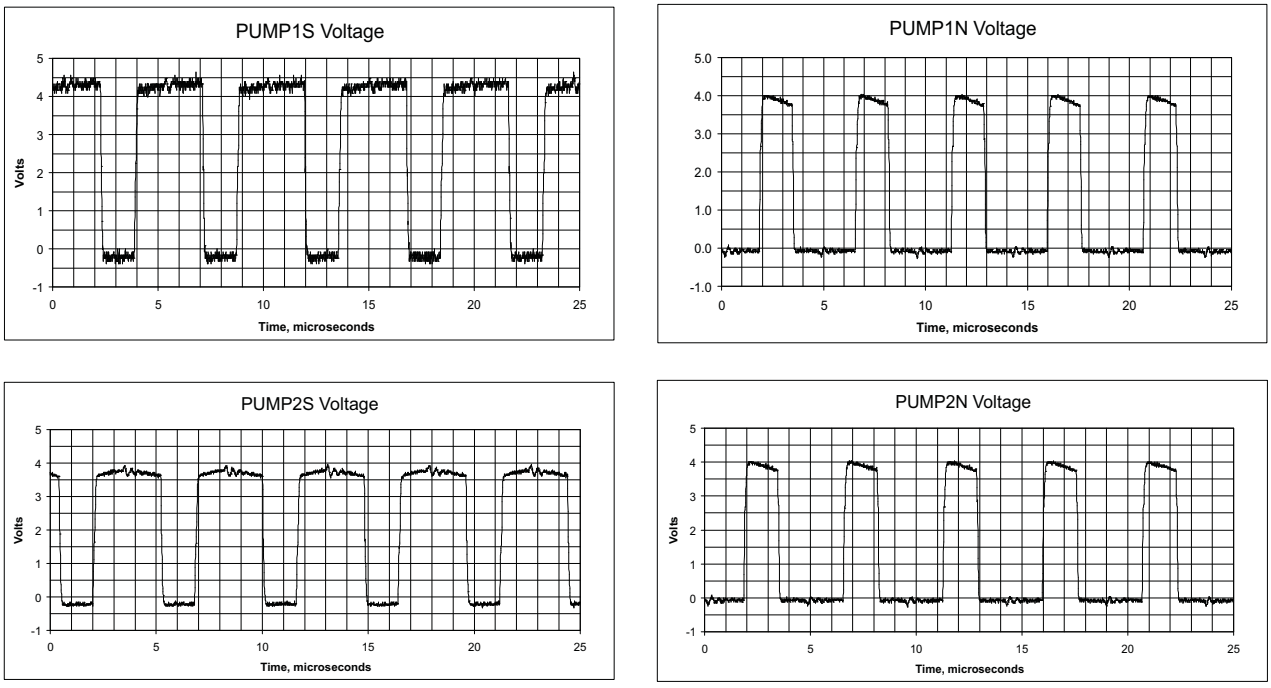

Figure 3. PowerPump Control-Signal Waveforms

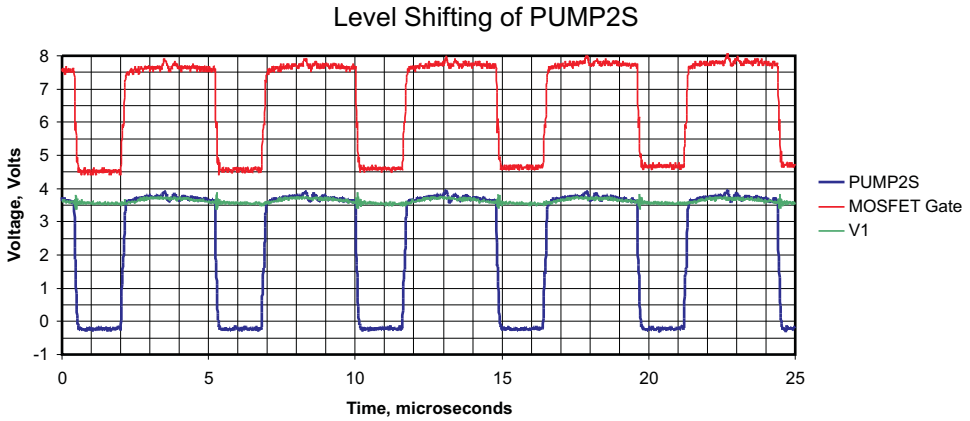

Figure 4. Capacitor-Level-Shifted PowerPump Control Signal PUMP2S

In the bq76PL102, PowerPump signals are referenced to VSS and derived from the cell voltage at the V1 pin. In the schematic, Figure 2, the PowerPump balancing transistors Q2 and Q3 are referenced to voltages that are higher than V1. A series capacitor is used to level-shift the signal to drive the gates of each MOSFET. An example is shown in Figure 4. The gate of Q2 is biased at the V2 voltage, approximately 7.5 V, whereas the PUMP2S signal is based by V1, approximately 3.6 V. This simple level shifting allows the use of low-voltage PUMPxy pins and low-Vgs MOSFETs, as the swing in Vgs voltage is less than a single cell voltage level (V1). The capacitor C5 and the input capacitance (Ciss) of the MOSFET Q2 (~330pF) form a capacitive divider that reduces the drive level by a small amount. The effective duty cycle is also reduced. This reduction, about 10% in this case, should be taken into consideration when selecting the N/P-channel MOSFETs.

3 Cell Balancing Algorithms and Settings

The PowerPump balancing activity is controlled by the bq78PL114. There are three PowerPump cell balancing algorithms provided:

- Terminal voltage: uses instantaneous voltage as input to balancing algorithm – basic algorithm.
- State of Charge: Uses cell State of Charge (SOC) as input to balancing algorithm – reduces cell balancing time during charge, cell capacities match at end of charge, and compensates for OCV differences
- Open Circuit Voltage (OCV): Uses cell Open Circuit Voltage (OCV) as input to balancing algorithm – factors in cell impedance to maintain balance.

Algorithm selection is accomplished through the Algorithm Enable register in the bq78PL114.

The bq78PL114 operates on 2-second cycles. PowerPump cell balancing and cell voltage, temperature and current measurements occur during mutually exclusive periods within the 2-second system cycle time. Because of this, there is an important and fixed parameter that must be applied when calculating PowerPump balancing performance called PowerPump algorithm-Duty-Cycle. The Algorithm-Duty-Cycle is the ratio of the time spent balancing to the 2-second system cycle time. For the bq78PL114 operating with eight series cells, this is approximately 750 ms out of every 2-second cycle, or 37.5%. For the case where only four series cells are used, the time is about 1000 ms or 50%.

The times given are actually the total time of two balancing-time windows within each 2-second period. Later in this paper, when the average PowerPump cell balancing current is determined, it must be multiplied by the Algorithm-Duty-Cycle to determine the true average PowerPump current delivered during each 2-second system cycle.

Users can adjust a few algorithm parameters to suit their application needs:

- The Minimum Differential for Cell Balancing setting is the cell voltage imbalance, in millivolts, needed before PowerPump balancing starts. The default value is 10 mV. Therefore, PowerPump cell balancing would be active as long as two or more cells are greater than 10 mV apart. This 10 mV can refer to an actual or adjusted terminal voltage, depending on the algorithm selected.

- The Cell Balancing Lower Voltage cutoff is a derived value that can be indirectly set by the user. The equation for the cutoff is:

  (Lowest Voltage Cell – Discharge Completion Voltage Qualifier/Number of Cells) > Minimum Differential for Balancing
- Enabling of a SuperPump mode (bq78PL114S12 Only) to increase the PowerPump Algorithm Duty-Cycle. The Algorithm Enable register in the bq78PL114S12 allows the user to configure SuperPump mode in 1 to 16 different levels. The level corresponds to the number of times temperature measurements are skipped during each 2-second system cycle time. Skipping temperature measurements allows for more time available for PowerPump balancing. See the *bq78PL114 Technical Reference Manual* (SLUU330) for more details.

Again, the foregoing cell voltage can refer to either actual terminal voltage or adjusted voltage, depending on the algorithm selected.

The PowerPump balancing algorithm does not have an upper cell-voltage limit. The upper limit is indirectly governed by the SmartSafety features of the bq78PL114, such as Cell Over Voltage (COV) Threshold. The bq78PL114 SmartSafety serves to prevent the cells from reaching a dangerous high voltage under charge. SmartSafety in the bq78PL114 also protects against an unrecoverable cell imbalance condition as set by the Cell Imbalance Fail Voltage parameter. PowerPump cell balancing is also halted during SmartSafety events that cause a fuse blow condition (SPROT). See the *bq78PL114 Technical Reference Manual* (SLUU330) for more details.

4 Balancing Circuit Operation

Given the previously described details of the PUMPxy control signals and the PowerPump algorithm, one could easily use circuit analysis software, i.e., SPICE, to create a quite accurate model of the performance of the PowerPump charge transfer circuitry and ultimately calculate the average current passed from one cell to the next. This is the essential goal of the analysis – to compute the average current pumped from cell to cell.

Explanation of the PowerPump circuit operation, particularly how the inductor is used to transfer charge from one cell to the next is explained. The circuit in Figure 5 shows a PowerPump transistor pair similar to the one in Figure 2 and is the basis for the discussion. The single case of *Pumping Cell 2 South* during one period ($t_P = 1/f_P$) of the PUMP2S signal, $(204.8\ kHz)^{-1} = 4.88$ microseconds, is examined. This is indicative of how the other PUMPxy channels operate.

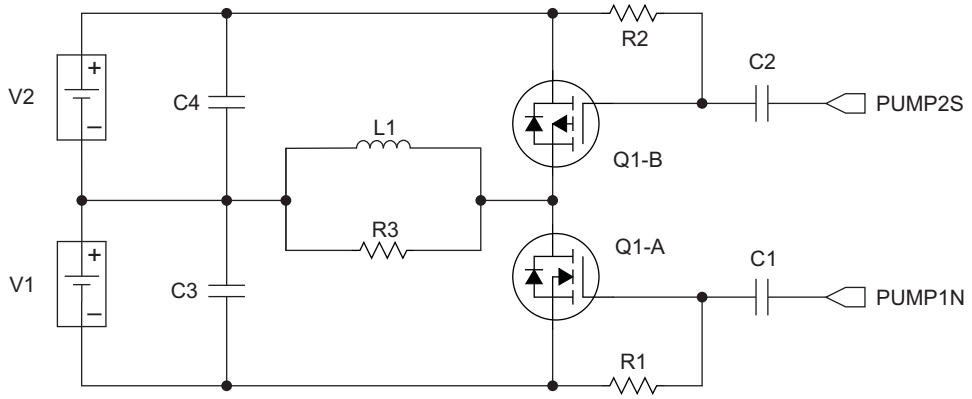

Figure 5. PowerPump Circuit Example – Pump Cell 2 South(P2S)

The PUMP2S signal is active when the control algorithm moves energy from cell V2 to cell V1, because cell V1 is lower than cell V2 by an amount greater than the Minimum Differential for Cell Balancing. Figure 4 shows the PUMP2S signal and the level-shifted signal applied to the gate of transistor Q1-B (in Figure 5).

This power converter circuit operates in the discontinuous mode and at a less than 50% duty cycle to maintain a controlled current flow. Within each PWM period there are three separate regions of analysis:

- Inductor charge from high cell
- Inductor discharge to low cell
- Inductor turnoff

4.1 Inductor Charge From High Cell

Goals of the circuit analysis in the *Inductor Charge From High Cell* phase are peak inductor current, average current from higher cell, capacitor ripple voltage, and capacitor value.

The circuit model of the Q1-B gate control is shown in Figure 6. The PUMP2S pin pulls down the capacitor C2 to the V1 reference voltage and causes the gate to source voltage of Q1-B to exceed the Vgsth rating of the MOSFET. The MOSFET conducts and operates in the saturation region where it can be simply modeled as a resistor equal to the drain to source resistance, $r_{DS(on)}$. The MOSFET is controlled on for a period of time equal to the duty cycle times the pump period or, $D \times 1/F_P = 0.33 \times 4.88\mu s = 1.61\mu s = t_{ON}$. Figure 7 shows the simplified output circuit model when L1 is being charged from V2.

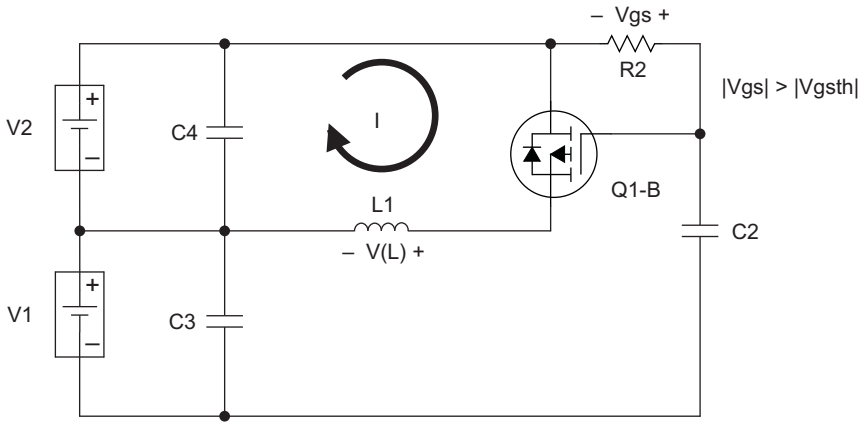

Figure 6. Circuit Model of Gate Control at Q1-B

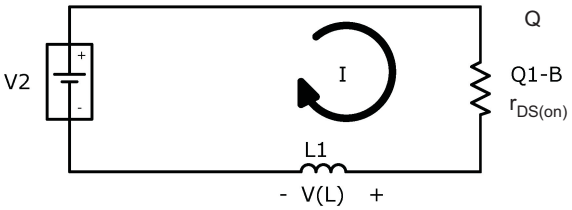

Figure 7. Simplified Model of Circuit During Inductor Charge Phase

The general solution of the inductor current during this time is:

$$i_L(t = 0 \rightarrow t_{ON}) = Ae^{-t\frac{r_{DS(on)}}{L}} + \frac{V2}{r_{DS(on)}} \quad (1)$$

The resistance, $r_{DS(on)}$, can be expanded to include other non-ideal circuit parameters such as PCB trace resistance, inductor resistance and others for a more exact solution. The complete solution is:

$$i_L(t = 0 \rightarrow t_{ON}) = -\frac{V2}{r_{DS(on)}}e^{-t\frac{r_{DS(on)}}{L}} + \frac{V2}{r_{DS}(on)} = \frac{V2}{r_{DS(on)}}\left(1 - e^{-t\frac{r_{DS(on)}}{L}}\right) \quad (2)$$

The value of the inductor peak current, I_{PEAK}, during inductor charge time is one of the circuit parameters used to select an inductor. An inductor having an I_{SAT} rating greater than the value of I_{PEAK} should be used. The peak current occurs at the end of this time period and can be found by setting $t = t_{ON}$ in Equation 2.

$$i_L(t = t_{ON}) = \frac{V2}{r_{DS(on)}}\left(1 - e^{-t_{ON}\frac{r_{DS(on)}}{L}}\right) = I_{PEAK} \quad (3)$$

This calculation assumes no loss in voltage level from the V2 current source. This equation can be iterated with different values of $r_{DS(on)}$ and L to specify peak current I_{PEAK}. A plot of a typical current ramp during this period is shown in Figure 8.

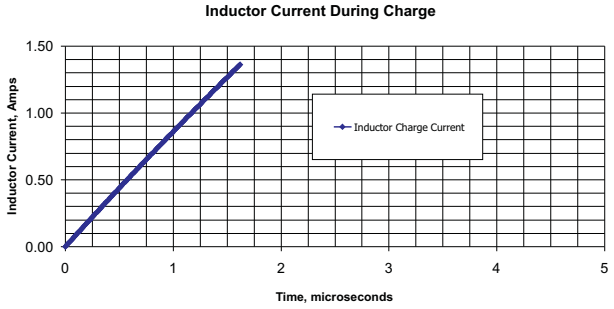

Figure 8. Plot of Inductor Current During Inductor Charge Time

The average current taken from the higher charge cell during each PUMP period is the area under the inductor current curve in Figure 8 spread over the full period $1/F_P$. This can be approximated by:

$$I_{AVE} = \frac{\frac{1}{2} I_{PEAK} t_{ON}}{t_P} \quad (4)$$

The basic assumption during the foregoing analysis was that the source cell voltage, V2, is an ideal source and that there were no voltage losses from this source to the inductor. In a standard application, cell V2 could be located several inches (or more) from the PowerPump circuit. High-frequency currents associated with the pump switching action would be sourced from V2 over the many inches of circuit trace and wire and would be subject to inductive and resistive losses. The capacitor, C4, is used as a local high-frequency current source during the time period t_{ON}. A high-frequency current loop is created by C4, L1, and $r_{DS(on)}$. See Figure 9.

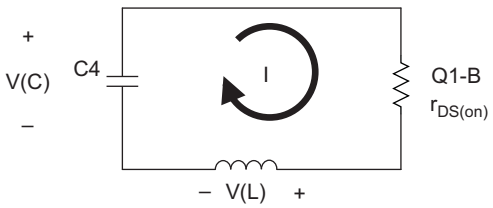

Figure 9. Model of Circuit Showing Capacitor as High-Frequency Current Source

The capacitor value is obtained through an iterative method taking the following steps:

1. Use average current from cell, assuming no ripple voltage, determined from above:

$$I_{AVE}(t = 0 \rightarrow t_{ON}) = \frac{\frac{1}{2} I_{PEAK} t_{ON}}{t_P} \quad (5)$$

2. Use Equation 6 to determine capacitor value based on allowable ripple voltage (dV_C).

$$I_{AVE} = C \times \left(\frac{dV_C}{dt}\right)$$

$$C = I_{AVE} \times \left(\frac{T_{ON}}{dV_C}\right) \quad (6)$$

For example, I_{AVE} = 0.250 A, TON = 1.61 µs, and dV_C = 0.1 V

Then,

$$C = 0.250\,A \times \left(\frac{1.61\,\mu s}{0.1\,V} \right) = 4\,\mu F \tag{7}$$

3. Subtract the ripple voltage, dV_C, from the value of V2 in Equation 3 to get a new I_{PEAK}. Then recalculate the average current using Equation 5.
4. If this new value of I_{AVE} is acceptable, end calculations. If not, start over at step 1 but adjust ripple voltage dV_C to a lower value.

The capacitor ESR should be considered when selecting a capacitor. An ESR less than or equal to the equivalent resistance of the circuit in Figure 9 should provide good performance. This will allow the capacitor voltage to recharge in a time equal to or less than the amount of time it took to discharge it. Common ceramic capacitors should work in most applications.

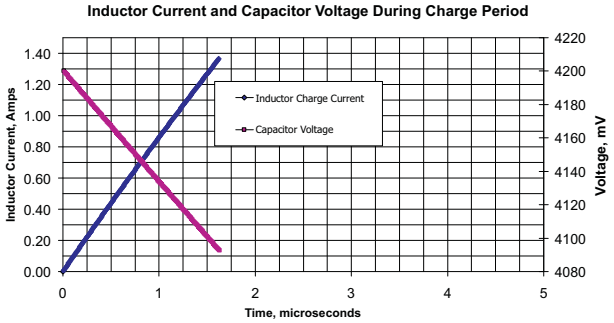

Figure 10. Inductor Current and Capacitor Voltage During Inductor Charge Phase

4.2 Inductor Discharge to Low Cell

Goals of the circuit analysis in the *Inductor Discharge to Low Cell* phase is the average current pumped to lower cell and the inductor value.

After the time period, t_{ON}, the MOSFET Q1-B is turned off. The current in inductor L1 continues to flow in the same direction, but the voltage polarity changes. The inductor voltage rises until the body diode of MOSFET Q1-A is forward biased and the inductor voltage, now referenced to the bottom of V1, charges cell V1. This is shown in Figure 11.

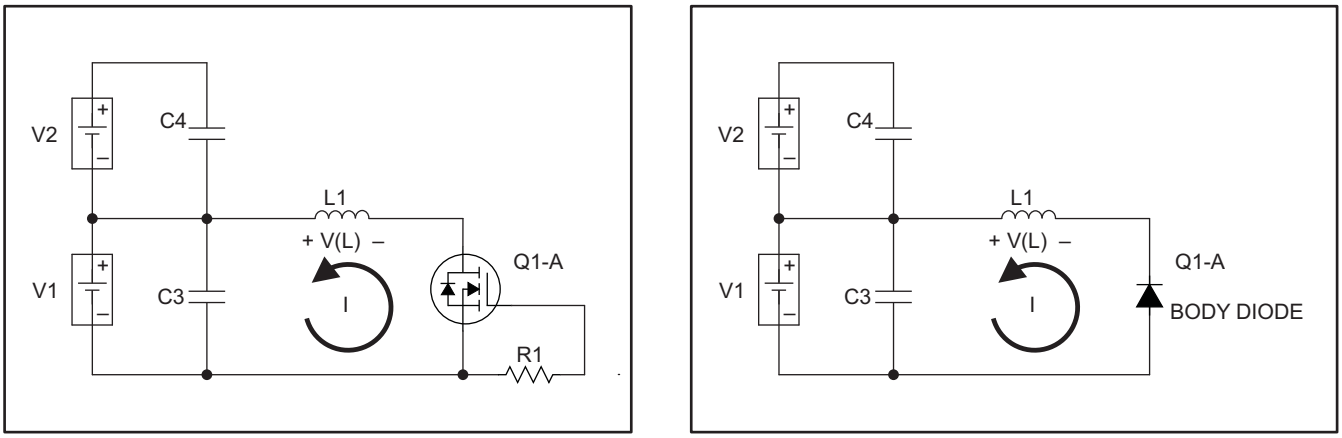

Figure 11. Equivalent Circuit Model Used to Determine Inductor Discharge Current Into V1

The current in the inductor flows into cell V1 until the body diode of Q1-A is no longer forward biased. t_{OFF} is the amount of time, starting from t_{ON}, when the body diode of Q1-A is no longer biased and the inductor discharge current no longer flows to cell V1. Figure 12 shows the definitions of t_{OFF} and t_{ON}.

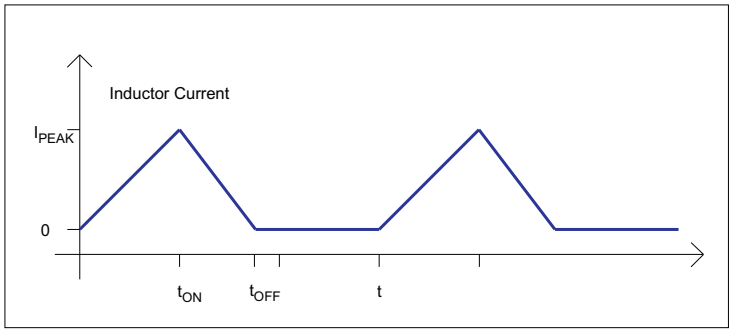

Figure 12. Inductor Current Waveform

The expression for the inductor current during the time from t_{ON} to t_{OFF}:

$$I_L(t: t_{ON} \rightarrow t_{OFF}) = \left(I_L(t = t_{ON}) + \left(\frac{V1 + V_f}{R_{PCB}}\right)\right)\left(e^{-(t - t_{ON})\frac{R_{PCB}}{L}}\right) - \left(\frac{V1 + V_f}{R_{PCB}}\right)$$

$$I_L(t: t_{ON} \rightarrow t_{OFF}) = \left(I_{PEAK} + \left(\frac{V1 + V_f}{R_{PCB}}\right)\right)\left(e^{-(t - t_{ON})\frac{R_{PCB}}{L}}\right) - \left(\frac{V1 + V_f}{R_{PCB}}\right) \quad (8)$$

R_{PCB} represents the very low resistance of the PCB traces connecting L1, Q1-B body diode and the capacitor. This results in the following curve.

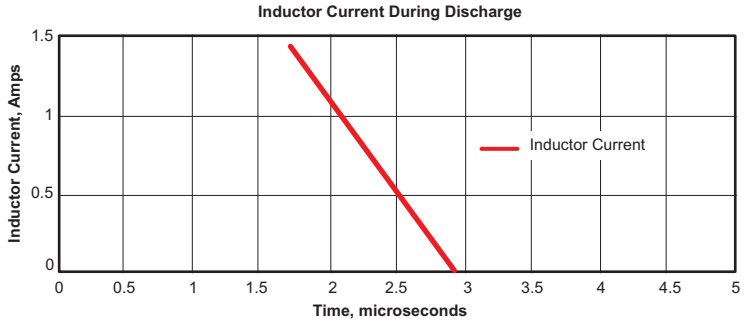

Figure 13. Plot of Inductor Current During Discharge Time

The average current delivered to cell V1 is the area under the curve of Figure 13. The time when the body diode is no longer forward biased and shuts down the inductor is needed to determine the average current delivered. The inductor voltage rises from the nominal V2 (referenced to V1) to more than the sum of V1 and the diode forward bias voltage. t_{OFF} is the time when the diode shuts off and V_F is the diode forward bias voltage then:

$$V_L(t) = L\frac{dI_L}{dt} = L\frac{\Delta I_L}{t_{OFF} - t_{ON}} = V1 + V_F$$

$$t_{OFF} - t_{ON} = L\frac{\Delta I_L}{V1 + V_F} \quad (9)$$

This is a result of the inductor volt-second balance concept. The time ($t_{OFF} - t_{ON}$) is less than t_{ON} if (V1 + V_F) is greater than V2. Therefore, the average current discharged into cell V1 is:

$$I_{AVE} = \frac{\frac{1}{2}I_{PEAK}(t_{OFF} - t_{ON})}{t_P} \quad (10)$$

The inductor current flow in the two stages of operation is summarized in the following plot, Figure 14.

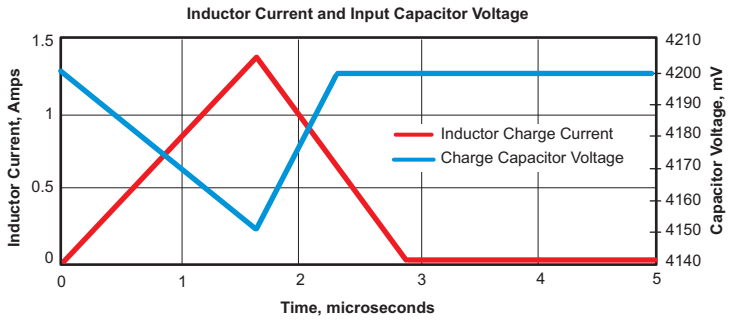

Figure 14. Plot of Inductor Current and Capacitor Voltage During One Pump Cycle

Based on the foregoing analysis, the forward voltage drop of the body diode within Q1-A, and Q1-B for that matter, influences the amount of current discharged into cell V1. The reference design in Figure 2 shows a Schottky diode (D1) in parallel with the body diode of Q1-A. The addition of this low-forward-voltage-drop diode in place of the body diode increases circuit efficiency.

4.3 Inductor Turnoff

After the body diode of Q1-A is no longer forward biased, the inductor current stops flowing into cell V1. See Figure 15 for the circuit model used during this time period.

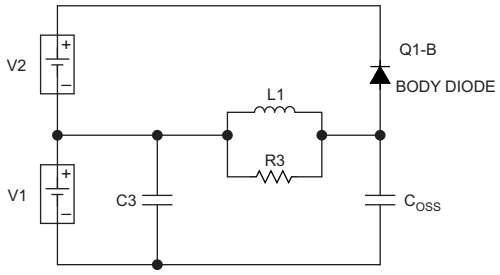

Figure 15. Circuit Model During Inductor Shutoff Period

The MOSFET Q1-A model is now reduced to only its output capacitance (C_{OSS}). The value of C_{OSS} is many orders of magnitude lower than C3. The remaining energy in the inductor *rings* out based on the effective capacitance and value of the resistor R3. The side of inductor L1 connected to the MOSFETs is momentarily pulled up to near V2 through the body diode of Q1-B (or external diode if added) and then oscillates with an exponentially decaying amplitude, characteristic of an under-damped system. The exponential decay rate is dependent on the value of R3 and L1 (i.e., the Q of the circuit).

This period of operation is used to specify a value for resistor R3. The first criterion is that the resistor not draw too much current during the two previous operating periods (inductor charge, discharge). The second criterion is that the resistor should be low enough to damp out the ringing of the circuit within the remaining time period, ($1/f_P - t_{OFF}$). A typical value for R3 is 2 kΩ.

A summary of the PowerPump signals is shown in Figure 16. The signals are aligned in time and demonstrate some of the high-frequency signal components that the foregoing basic circuit models do not include. The FET SWITCH trace shows all three stages of the operation of the inductor: charge, discharge, and turnoff. The PUMP2S PIN shows the pump duty cycle and the voltage level of the PUMP2S control signal. The PUMP2S GATE trace shows how the PUMP2S signal is shifted up to a level that properly biases a P-channel MOSFET gate.

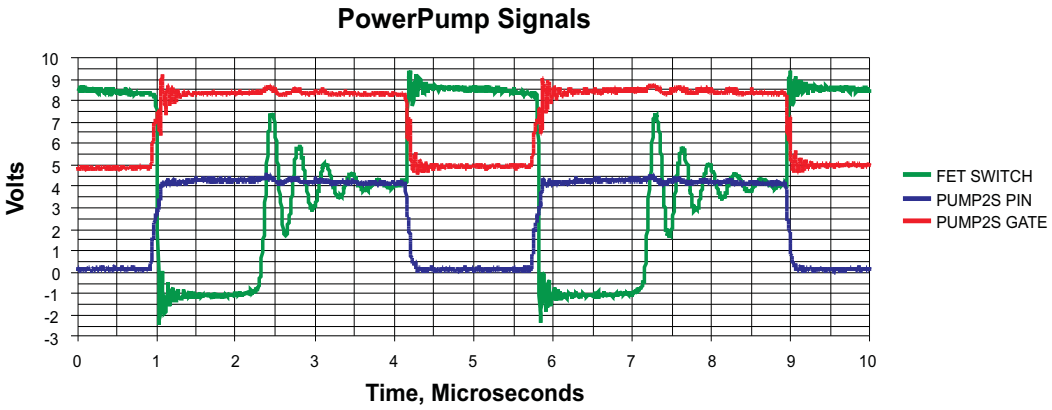

Figure 16. Summary of PowerPump Waveforms

5 PCB Layout Considerations

A PCB layout of the bq78PL102 schematic from Figure 2 is shown in Figure 17 and Figure 18. This is a cutaway of a larger PowerLAN reference design. The rest of the PCB is omitted and does not have much bearing on this particular discussion. The red color on the top layer and the blue color on the bottom layer are used to represent general circuit nets. The other colors represent the cell voltages: VSS, V(n), V(n+1) and V(n+2). A two-layer design is clearly possible, as evidenced by this design. Demand for smaller and smaller portable electronics may warrant a higher layer count.

PCB layout of the PowerPump cell balancing circuitry should follow the same rules that apply to typical high-frequency switching power-converter circuits. Figure 16 provide a good snapshot summary of the types of signals that are present in the circuit. These are high-frequency square-wave control signals and switched inductor signals. Both signals have high-frequency components due to square edges, and the inductor signal carries significantly more current. Peak inductor currents can be as high as 1 to 2 amperes, depending upon inductor value.

The PowerPump control signals, like PUMP2S, should have the shortest possible path to the gate of their respective MOSFET. The return path for the control signal is best accomplished using a copper plane connected to the signal reference. The reference for PUMP2S is VSS.

The higher-current inductor signals are the current loops described in Figure 6 through Figure 10. During the inductor-charge phase, capacitor C4, inductor L1, and MOSFET Q1-B form a high-frequency loop with large peak currents. To minimize the generation of noise and make the circuit as efficient as possible, these components should be placed and routed so that the loop area created by the signal path is as small as possible. The widest possible traces should be used to minimize voltage drop. The best method of connecting the cell voltages to the PowerPump circuit is through a wide copper plane, on an inner or outer layer, that is local to the MOSFET/inductor/capacitor current loop.

The above recommendations are reflected in the example PCB layout:

- PowerPump components are located as close as possible to each other (example Q1, L1 C1, D1) and connected with short, wide traces.
- Copper areas are created for signal-reference nets like V(n), V1(n+1), and V(n+2). Primary location is on the bottom layer. This minimizes the impedance of the return path for the high-frequency signals.

Heat dissipation in this circuit is generally not a concern, due to the use of the high-frequency switching topology and low-on-resistance MOSFETs. As an example, a MOSFET with an $r_{DS(on)}$ of 0.25 Ω and junction-to-ambient resistance 130°C operating at average current of 0.25 amperes has a temperature rise of a few degrees. The high efficiency/low heat dissipation of this cell balancing circuit, compared to an equivalent resistive-bleed balancing circuit, supports a dense layout. This is an advantage in high-cell-count systems.

Figure 17. Top-Layer View of bq76PL102 PowerPump Reference Circuit

Figure 18. Bottom-Layer View of bq76PL102 PowerPump Reference Circuit

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