Application Report
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UCC2895 Layout and Grounding Recommendations

John Bottrill

ABSTRACT

The UCC2895 family of Phase Shifted Full Bridge Power Converters Control Circuits are designed to provide efficient power conversion with minimal noise generation. This is accomplished by the resonant switching of the primary side voltages, which minimizes the switching losses and the voltage/current transients that would be present in a hard switched conventional full bridge power supply.

1 Overview

Though resonant converters minimize the generation of noise in power circuits, the designer must take care in the layout and grounding of the converter's control circuit to limit the noise introduced into the device. The UCC2895 has features to help with this.

Any significant noise on the incoming signal lines will result in misinterpretation by the control loop. Without a clear, strong control signal, the converter may not respond as desired. This application note explains how to avoid noise problems when using these controllers.

2 Grounding

There are two separate ground planes around the controller, the power ground plane and the signal ground plane. The ground connections to the power circuitry are accomplished over the power ground plane, which connects to the PGND pin. UCC2895 pins VCC, OUTA, OUTB, OUTC and OUTD are located over the power ground plane. The signal ground plane is reference for the control circuitry, including operational amplifiers, comparators, internal clocks and control logic, and is connected to the GND pin. Timing, compensation, and filtering components are located over the signal ground plane.

For best noise rejection, there must only be one ground connection from the GND pin to the PGND pin, located directly under the device. Figure 1 shows the recommended configuration of ground planes for the UCC2895. The power ground plane (enclosed in red) only connects to the signal or quiet ground plane (enclosed in green) by a large trace (blue) directly under the device. The power ground plane connects to the PGND pin and the driver, and from there to the negative side of the input power bulk capacitor. This bulk capacitor should be located as close as possible to the sources of the B and D switches in the H bridge.

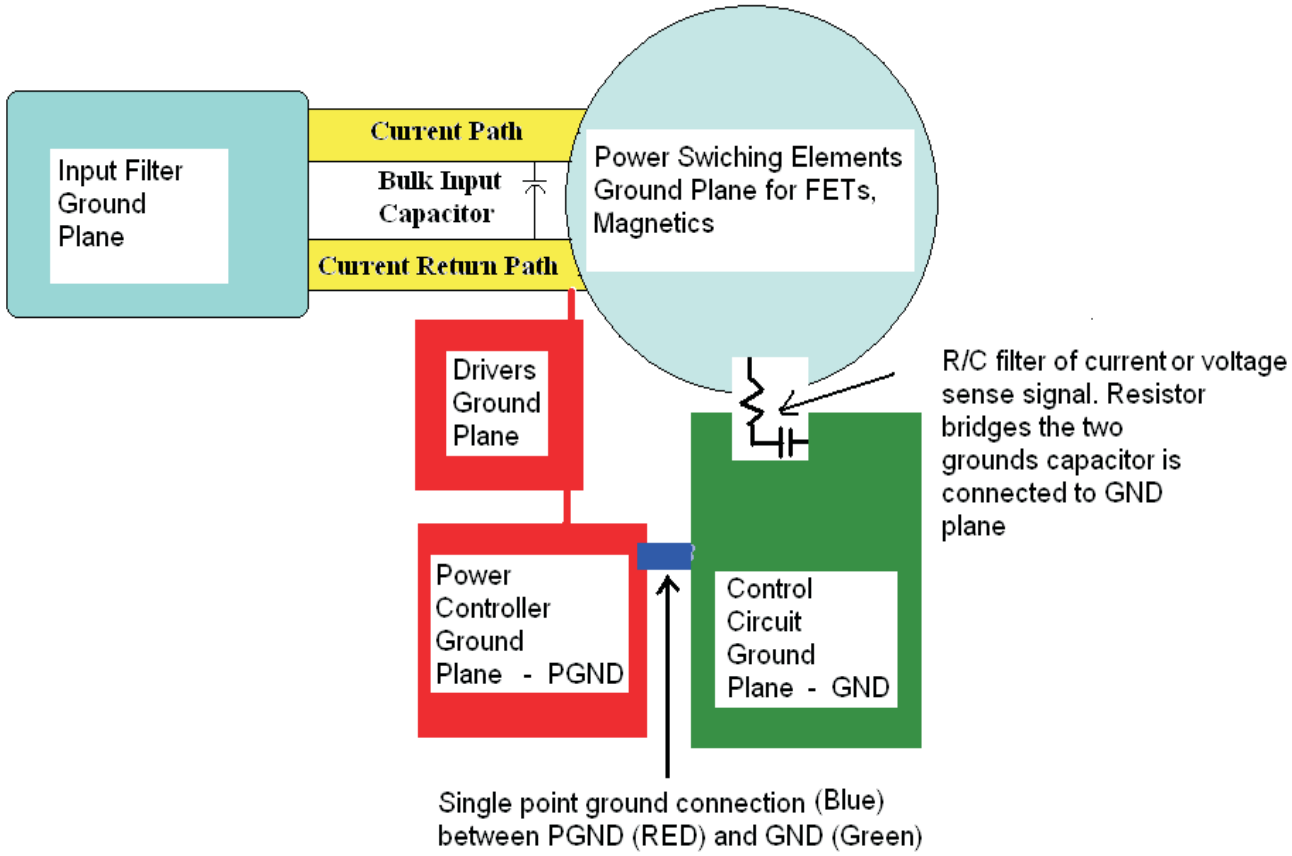

Figure 1. Visualization of Grounding in a Power Supply Built Using the UCC2895

Keeping the connection between the two planes to a single trace prevents the formation of any ground loops which can lead to circulating current and voltage errors.

The power ground plane is connected to the current return paths (yellow in Figure 1) of the power components such as the primary side bulk capacitor and the source of the lower FETs of the phase shifting bridge. Though the power ground plane connects to these components, it should not form part of the path for the return current to the converters input or the path from the FET output to the input capacitor. The input current return path has only one connection to the power ground plane and that plane is divided into two so that the driver-induced currents do not travel to or around the plane that is connected to PGND. This separation between the driver power plane and the UCC2895 PGND pin does not need to be a single trace. It can be accomplished by placing the driver between the UCC2895 and the FETs and then locating the returns for the drive signals over the power ground plane and as near as possible to the drive signal. This further limits the noise that the device will encounter.

3 Bypassing

There must be a substantial ceramic low ESR, low ESL capacitor directly across the VCC and PGND pins of the UCC2895, and another low ESR, low ESL capacitor across the drivers. An electrolytic capacitor located next to the ceramic capacitor from PGND pin to VCC of the UCC2895 is also highly recommended. These device pins and the gate drive device pins are adjacent to each other to facilitate placement close to the bypass capacitors and routing above the power ground plane, the return path for the UCC2895 drive currents.

The OUTx pins have currents with high peak current and high current slew rate. OUTx current comes from VCC of the device and returns to PGND, and require a low impedance source. High supply impedance would prevent the delivery of the current needed for fast switching. The low ESL/ESR capacitors that have been placed right across the VCC and PGND pins provide this low impedance source for these currents.

On the other side of the device are the REF and GND pins. REF is an internally generated voltage rail that provides power and critical thresholds to the control circuits, including amplifiers, comparators, clocks and control logic. These signals must be quiet to insure correct switching, so the REF bypass capacitor must be placed very close to the UCC2895 and routed directly to REF and GND with very short traces. Drive limitations within the device limit the amount of capacitance directly tied to this pin to 4.7 µF. If additional capacitance is desired it should be connected through a 100-Ω resistor.

VCC supplies current to the REF capacitor through an internal regulator. The negative side of the REF voltage supply is the GND pin. All control signals in the device are with respect to GND, not PGND. All drive voltages and currents out of the device are with respect to the PGND.

Because of the relative high impedance of the internal device connection between PGND and GND, it is important that this internal path not be relied on for carrying currents. Since multiple ground paths can result in circulating currents, the single solid ground track directly under the device must be the only connection between the two ground pins.

Any significant noise on the incoming signal lines will result in misinterpretation by the control loop. Without a clear strong control signal the converter may not respond as desired.

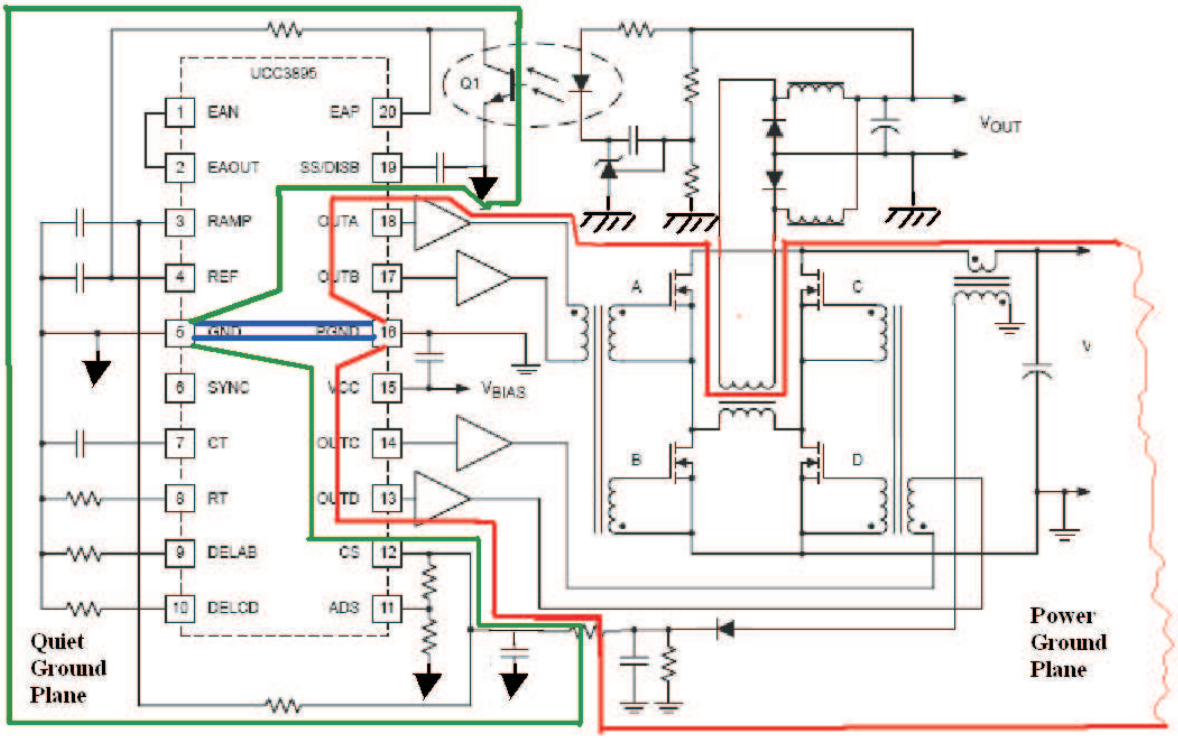

Figure 2. Location of the Appropriate Ground Plane for Each Component

In Figure 2, the detailed schematic diagram shows the appropriate ground plane for each component. Components in the green boundary are placed above signal ground plane and components above the red boundary are placed above the power ground plane.

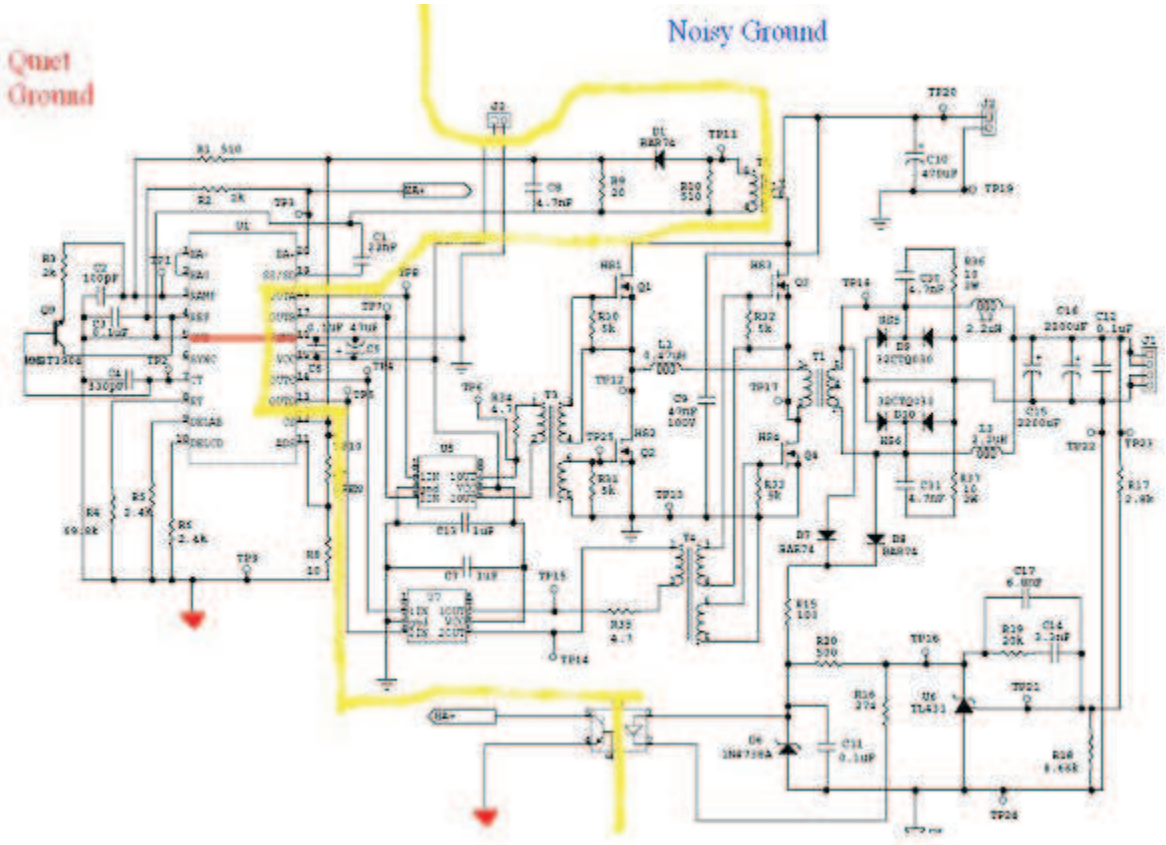

Figure 3. Separations of the Power and Signal Ground Planes for a Typical UCC2895 Converter

Figure 3 shows a typical power supply and highlights the separation between ground planes. Only signal lines that are bringing signals to the device should be near the signal ground plane. The REF pin is connected through a low ESR and low ESL pin capacitor directly to the GND pin and provides the filtering of the power for this circuit.

When the device initially powers up, the charge required to bring the REF capacitor C3 from 0 V to 5 V is drawn from the VCC capacitor, C5. During this charging time, C5 will droop by 5 V times the ratio of C3 to C5. C5 should be at least a factor of 10 times larger than the C3 so that the voltage on the VCC will dip by less than 0.5 V.

REF is used as the source for the high frequency currents to all the internal control circuitry within the device and the return path for that current is the GND pin. The dc current then finds its way to the power source through the single thick connection to the PGND pin. Any internal switching noise, such as CT discharge, is thus eliminated from the internal connection between the two grounds and minimizes the level of noise within the device.

4 Filtering

In a normal configuration, the voltage feedback signal and the current sense signal come from the power stage to the UCC2895. These signals must be laid out carefully to avoid noise and in some cases, these signals may also require filtering. Parallel traces can capacitively couple noise, so these traces must be routed at 90 degrees to any traces with high voltage slew rate. Where possible, these traces should be over quiet areas of the circuit.

The incoming voltage feedback signal may pickup noise and may have to go through an RC lowpass filter. This will improve the signal to noise ratio, as shown in Figure 1. The incoming signal goes through a resistor which is located at the start of the signal ground and bridges the gap between the power ground plane and the signal ground plane. The filter capacitor goes directly to signal ground immediately after the resistor. Figure 4 shows this layout. The filter roll off should be at least an order of magnitude higher than the voltage loop 0 dB crossover so that RC phase shift does not effect the control loop response.

Figure 2 is an expansion of Figure 1. The signal ground plane, shown by the green boundary, encloses all the components that must be located above the signal ground plane. These components use the signal ground plane for ground reference. The red boundary represents the edge of the power ground plane and it extends to include most of the components that would normally be located above the power ground plane, including the primary side of the driver transformers. The connection to the FET and switching ground plane is shown at the input bulk capacitor.

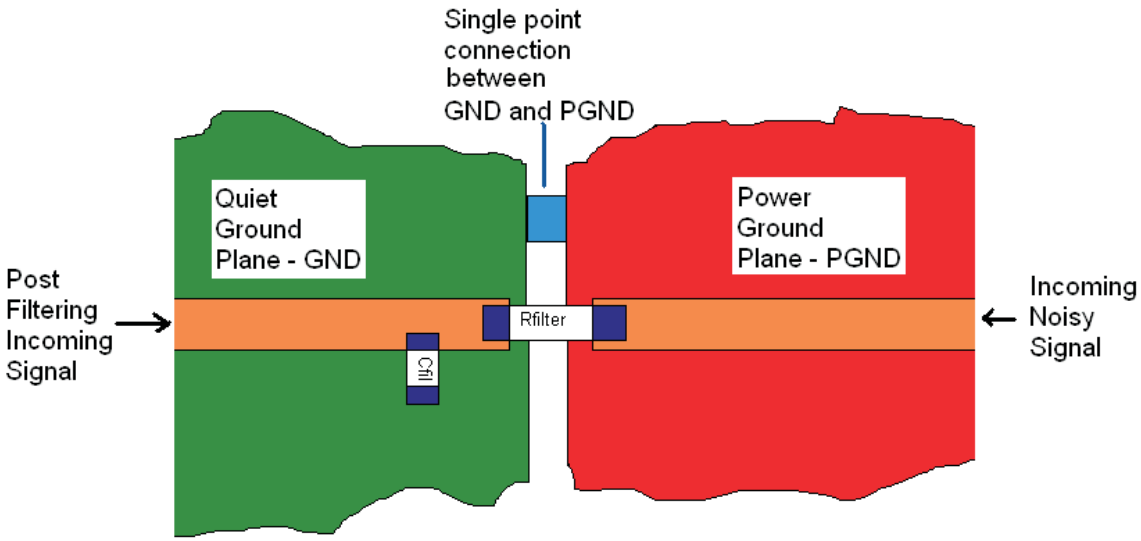

Figure 4. Incoming Signal Filter Placement

The same precautions may be necessary for the incoming current signal. Although a large RC filter is practical for the voltage sense signal, the current loop bandwidth and pulse-by-pulse current limiting restricts the current sense filter size to a much high frequency.

If the sync feature is used then that signal may also have to be filtered.

Another way the signal to noise ratio can be improved is to make certain that the signal that is presented to the device is as large as is practical. This automatically makes the signal to noise much higher than one that requires amplification at the control device. In fact, throughout the whole feedback chain the signal should be as high as is practical.

Still another method of improving the signal to noise ratio is to use relatively low impedance components in the feedback loop. Since most noise sources are relatively high impedance, using low impedance components will reduce the noise that is injected into the signal chain.

Care must also be taken that all signals do not exceed the absolute maximum limits for the device.

5 Overshoot and Undershoot Considerations

All traces have distributed capacitance and series inductance. Depending on node impedances, current slew rate and voltage slew rate, some nodes will exhibit resonance, which can lead to overshoot and undershoot. This is commonly called “ringing”. When terminals of an integrated circuit overshoot the power supply or undershoot ground, large currents can flow into the device, causing momentary malfunction, latch-up, or damage. The most likely signals on the UCC2895 to exhibit this are the OUTx pins, but ringing on any pin could potentially cause problems.

If a pin undershoots ground, for example, it can forward bias the junction formed by the pin’s protection circuit and substrate. This forward-biased junction will inject carriers into the device substrate, and these carriers could drift to other junctions and cause voltage drop that will lead to voltage errors in sensitive signals. If the forward-biased junction current is high enough, this current could cause other devices to turn on and potentially trigger a parasitic SCR, leading to latch-up. Mild latch-up will prevent the device from functioning properly until power is removed, but extreme latch-up cases can lead to excessive current flow in the integrated circuit and damage.

Although modern integrated circuits such as the UCC2895 are built using robust CMOS processes incorporating elaborate protection circuits to prevent malfunction and latch-up, the combination of sensitive analog circuits and power circuits on the same device means that there is always a potential for these issues. Every pin of the integrated circuit is connected to a junction. For some pins, this is an ESD protection diode. For other pins, this is the drain of a power MOSFET. This is illustrated in the cross-section shown in Figure 5.

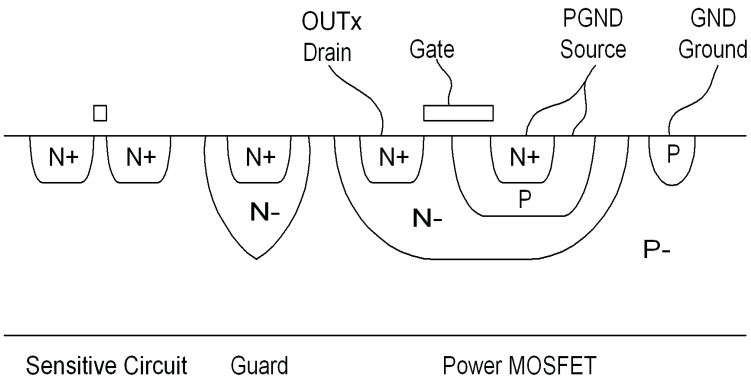

Figure 5. Cross Section of a Typical Integrated Circuit, (showing a power device and a sensitive device, separated by a guard)

In this representative cross-section, one low-side power MOSFET is shown, which represents the pull-down device connected to one of the gate driver output, OUTx. The drain of this power MOSFET is connected to the pin OUTx. In parallel with this power MOSFET is a diode from OUTx to PGND. If pin OUTx undershoots ground, this diode will conduct and inject electrons into the P- region. A large guard structure between the Power MOSFET and the sensitive circuits will collect most of these electrons, but if enough undershoot occurs, enough electrons could reach the sensitive circuit to cause malfunction.

The best way to minimize the risk of overshoot or undershoot is to minimize series inductance by routing high current signals through the shortest possible traces. If ringing is observed, it can be reduced by adding series damping resistance. Often, a series resistance of 5 Ω to 10 Ω is adequate to reduce ringing and in many cases, this series resistance will not degrade switching speed or other measures of performance. As a last resort, some overshoot or undershoot requires clamping with a low forward voltage drop Schottky diode.

6 Summary

The phase shifted full bridge power converter is an excellent topology for high efficiency power conversion. The UCC2895 controller makes implementation of such a power converter simple, provided that considerations are given to:

- Separation of the power and signal ground planes
- Correct connections to the power and signal ground planes
- Careful component placement
- Appropriate routing of sensitive signals
- Filtering of noisy signals
- Minimizing overshoot and undershoot

If all of the practices described here are followed, the phase shifted full bridge power supply should operate with no problems as a result of signal noise or grounding.

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