Application Report
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Design Considerations for the UCC28600

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ABSTRACT

The UCC28600 Quasi-Resonant Green-Mode Controller provides engineers with a cost-effective solution for designing energy efficient power supplies. Despite the 8-pin package, the device has many built-in advanced protection features. Because most of the pins on the device have dual functions, careful attention must be given to the design and layout of the circuit. What follows is a brief discussion and helpful hints that make the design process more successful.

1 The Design Calculator

It is expected that the engineer becomes acquainted with and uses the Design Calculator that is in the Tools and Software section of the UCC28600 product folder on the Texas Instruments website. This is an invaluable user-interactive tool that performs bracketed search routines and solve for the peak-primary current, the secondary RMS current, the duty cycle, actual switching frequency, and provide a mode map at any given operating condition.

The user is required to provide design requirements such as:

- Input Voltages
- Output Voltages
- Power Levels
- Efficiency Estimates
- Ripple Voltage
- Over-Voltage Thresholds
- Initial Selection of MOSFET Switching Device
- Initial Selection of the Output Rectifier
- Maximum Allowable Drain Voltage
  - As a function of the desired percentage of the reflected output voltage, referred to as the *snubber overshoot %*, cell C26 of the QR Design Tool

The design tool generates a recommended design that includes transformer parameters, component values for the current sense resistor, the power limit programming resistor, the over-voltage programming resistors, the output capacitor, the soft-start capacitor, snubber components, and the peak and RMS currents.

Some considerations when applying the spreadsheet:

1. The macros must be enabled for the spreadsheet to perform the I(find) function that generates I_{PEAK}. If the computer being used is set to a high security level, the spreadsheet will not ask the user if the macros should be enabled. If the result for I_{PEAK} is not a numerical value (i.e. cell G98) the macros have not been enabled. A medium level of security, or less, is required.
2. When using a power factor correction (PFC) input stage, the maximum input voltage, $V_{AC(max)}$ in cell C15 of the design tool spreadsheet, should reflect the actual voltage of the PFC output, i.e. the user should input a value in this cell that is equal to:

$$V_{AC(max)} = \frac{PFC_{OUT}}{\sqrt{2}}$$

   The actual converter will follow the high line profile whenever the PFC stage is enabled.
3. The spreadsheet imports the information from the first sheet, the QR Design Tool sheet, to the QR Simulator sheet but the user must input the actual values used for several key components. As a reminder, the recommended ideal values are automatically provided next to the input cells. Information, such as the actual transformer turns for each winding, and standard values for the current sense resistor (R_{CS}), the over voltage resistors (R_{OVP1} and R_{OVP2}) and the power limit resistor (R_{PL}) must be manually added to the simulator page. Note that the user may need to iterate two to three times as the actual standard values are entered and updated recommendations are given. Based upon these actual values, the simulator will generate mode maps showing the switching frequency, f_S, with respect to feedback voltage, input power, and primary current. The user is encouraged to modify the input information in order to generate a design that fits their individual requirements such as desired mode boundary transition.
4. The displayed operating modes maps on the QR Simulator sheet of the design tool show the theoretical transition point between each operating mode. The following figures show the labeled ranges where FFM is the frequency foldback mode, DCM is the discontinuous current mode, and QR is quasi-resonant mode. The mode at any given operating point is determined primarily by the voltage on the feedback (FB) pin. The design parameters that influence these boundary conditions are the magnetizing inductance, the reflected output voltage, and the input voltage range. The spreadsheet uses these parameters to calculate the feedback voltage:

$$V_{FB} = A_{CA(FB)}\left[I_{p(actual)}R_{CS} + \left(\frac{I_{PL}}{I_{OVP}}\right)\left(\frac{N_{BIAS}}{N_P}\right)\left(\frac{V_{BULK}}{R_{OVP1}}\right)\left(R_{PL}\right) + V_{CS(offset)}\right]$$

Where $A_{CA(FB)}$ is the current sense gain, typically equal to 2.5 V/V as shown in the electrical characteristics chart in the data sheet; I_{PL} is equal to the CS current during power limit, typically 150 µA as shown in the electrical characteristics in the data sheet, I_{OVP} is equal to the OVP current and is set to 300 µA, R_{CS} is the value of the current sense resistor, N_{BIAS} and N_P are the actual number of turns on the bias and primary windings , respectively, V_{BULK} is equal to the input voltage to the flyback, such as the output voltage of the PFC stage, R_{OVP1} and R_{PL} are the top OVP divider resistor and the power limit resistor, respectively, and the $V_{CS(offset)}$ is typically equal to 0.4 V as shown in the electrical characteristics chart in the data sheet. The $I_{P(actual)}$ is calculated by the I(find) macro in the Design Calculator spreadsheet and its value is bracketed with respect to the bulk input voltage, the magnetizing inductance, the reflected output voltage as defined by the user-selected snubber overshoot, and the input power. Careful selection of these design parameters reshape the mode maps and change the mode transition operating levels. An optimized design would include transition from the burst operating mode into FFM at less than 10% to 15% of the overall maximum output power.

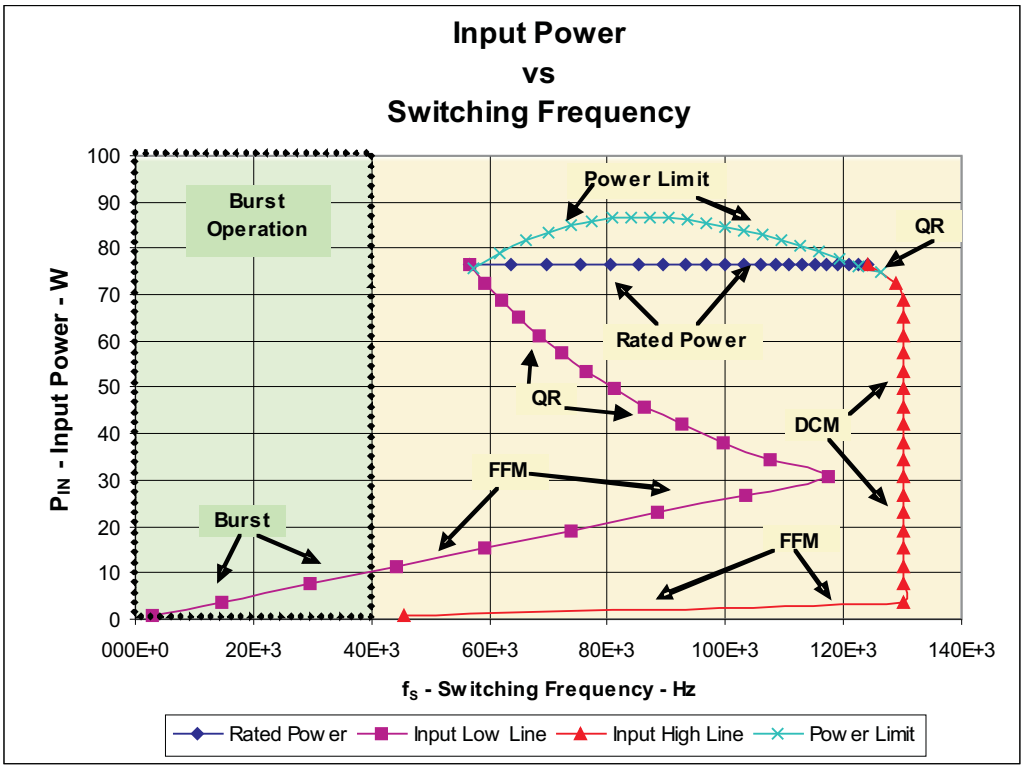

Figure 1. Boundaries with Respect to Input Power

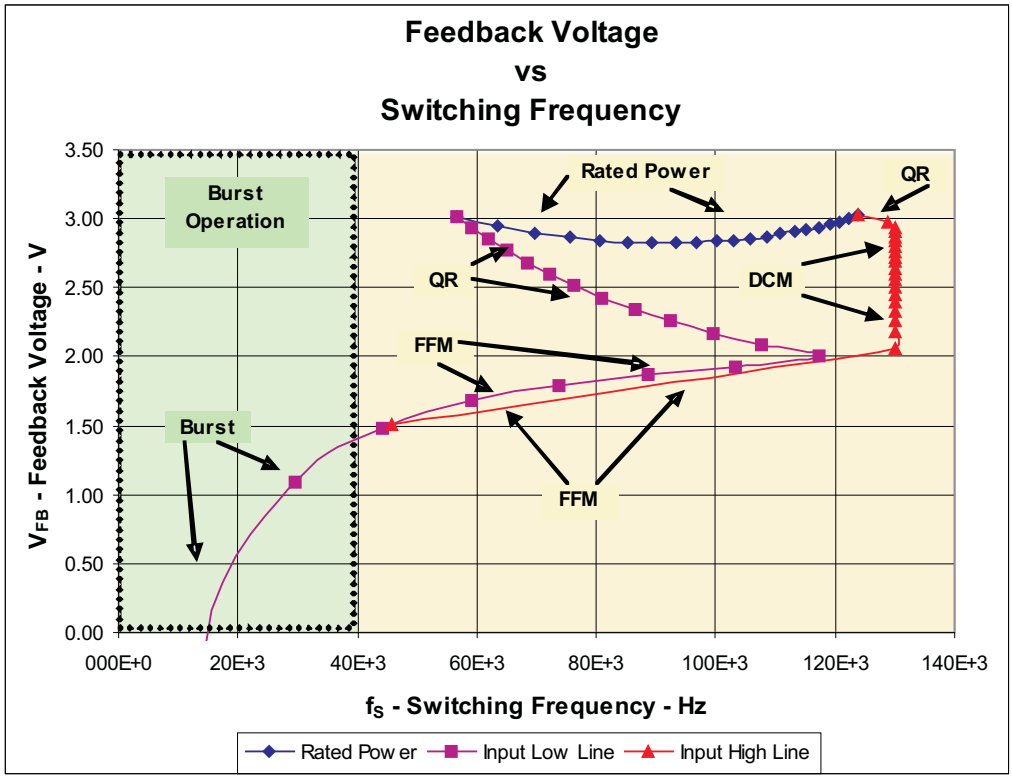

Figure 2. Boundaries with Respect to the Feedback Voltage

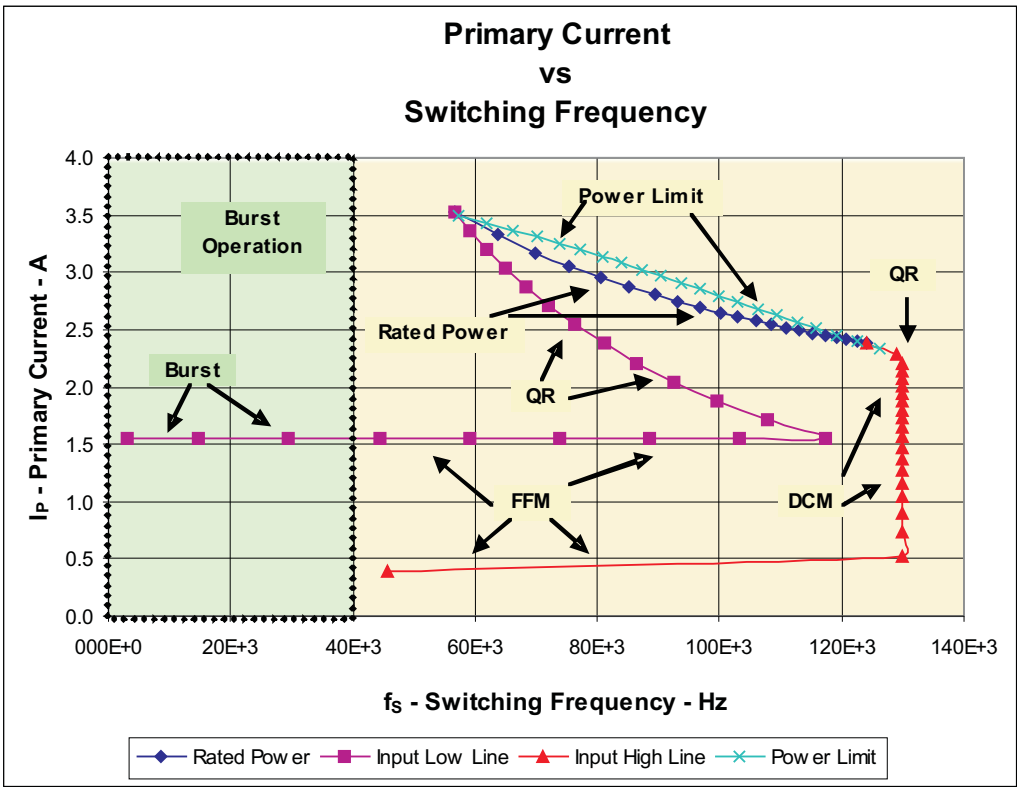

Figure 3. Boundaries with Respect to the Primary Current

2 Transformer Design Considerations

Once the Design Calculator spreadsheet has determined the recommended primary inductance, the acceptable leakage inductance, and the turns ratios for the secondary and bias windings, the transformer can be designed. Be sure to insert the actual turns used in the final design into the appropriate cells in the QR Simulator spreadsheet. It is absolutely crucial that the bias windings be well coupled to the primary. These windings not only supply the operating bias to the UCC28600 and, possibly the PFC controller, but also determine quasi-resonant status and play a key roll in accurate fault detection. Working in conjunction with the OVP resistors and the power limit and current sense resistors, the information provided by the bias windings sets up the internal reference current for limiting the power on a cycle-by-cycle basis. As a result, the bias windings must provide an accurate proportional portrayal of the primary current.

To minimize leakage inductance and still meet isolation requirements, design the windings using triple insulated wires and minimal tape layers. Filling the winding layers with bifilar windings and placing the bias windings as close as possible to the primary windings is necessary for a successful transformer design. Spreading the bias windings over the entire width of the bobbin and adding a small capacitor (under 100 pF) to primary ground at the diode end of the winding will divert noise out of the transformer. Also, cores with a round center post will help reduce leakage. Figure 4 shows a recommended winding pattern for the transformer.

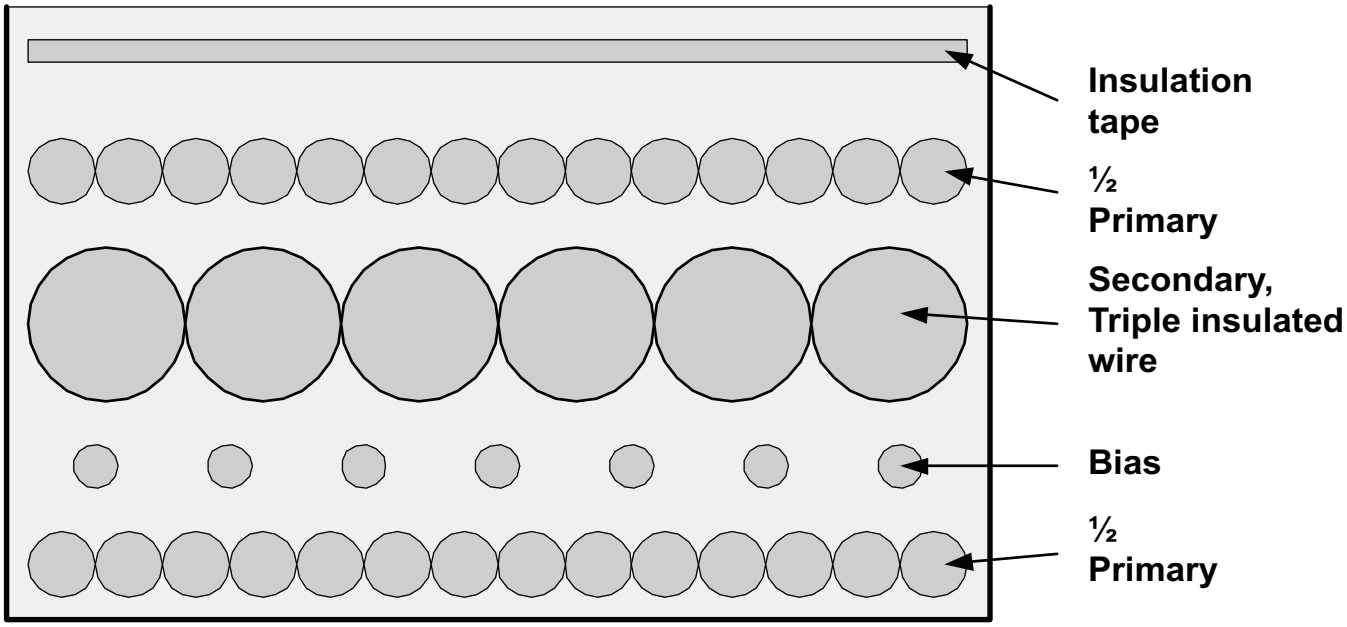

Figure 4. Example of a Recommended Transformer Design.

Note: Use multiple strand wire to distribute each of the coils across the layer.

For a non-PFC design using universal ac line input or a boost-follower PFC design, the core and number of turns is selected based upon the minimum input voltage. For designs using a traditional boost PFC front end, the core must be selected based upon the steady state high line conditions but must also take into consideration the low line ac voltage. Because the UCC28600 will always start up with the PFC stage disabled via the STATUS pin, the flyback transformer must be designed to avoid saturating when turning on into any acceptable load at low line conditions.

Because the transformer is a major contributor to the audible noise that may be present on the converter, the entire transformer assembly should be varnished and glued. Also adding filler in the discrete gaps will reduce the mechanical chatter between the bobbin, core, and coil. Be sure to match the temperature coefficients of any material used as closely as possible otherwise when the transformer warms up during normal operation, the audible noise intensifies.

Using a copper shield, or *belly band*, around the entire transformer will provide a circumferential radiation shield for the eddy currents in the transformer. This shield is simply a grounded loop of copper foil around the entire assembly; use of this technique requires careful consideration to isolation requirements and creepage and clearance issues. By winding the secondary so that the ground end is the outermost layer, this *belly band* may not be needed.

When gapping the flyback transformer, only gap the center leg because gapped outer legs will radiate excessive EMI from the fringing fields. Placing the drain end of the primary winding as close to the core as possible will help to shield the dv/dt noise emanating from it.

3 VDD Considerations

The initial start-up bias comes from the rectified input line, V_{BULK}, through the start up resistor, R_{SU} shown in Figure 5. Because of the extremely low start up current, 25 µA maximum as shown in the electrical characteristics table in the data sheet, this resistor can be a very high value, in excess of 2 MΩ; multiple resistors in series should be used for R_{START} due to the high voltage across them. This high value, in conjunction with C_{START} dictates initial start time. Note that the C_{START}/ D2 combination is in addition to the C_{BIAS}/D1 circuitry. This added stage is required to isolate the STATUS circuitry from the start up resistors and guarantee there is no conduction through STATUS when VDD is below the UVLO. When VDD is below the UVLO turn-on threshold there is the possibility of internal floating logic gates which could potentially divert the start up current from VDD if the additional circuitry is not present. R_{BIAS} is used to smooth out transitions on the bias line.

C_{BIAS} must be high enough to hold up VDD during the burst packet period and also during interrupted start up when no load is on the output to discharge the output capacitors. This pre-bias condition occurs when the converter is started under no load and then the input supply is briefly interrupted, resulting in the output capacitors maintaining the output voltage or slowly discharging. The C_{BIAS} value is determined by:

$$C_{BIAS} = \left(\frac{I_{STANDBY}}{VDD_{CLAMP} - V_{DD(uvlo)}} \right) R_Z C_{OUT} \, ln\left(\frac{V_{OUT} - V_Z}{0.95 V_{OUT} - V_Z} \right)$$

Where $I_{STANDBY}$ is given in the electrical characteristics table of the UCC28600 data sheet, typically 350 µA, $V_{DD(clamp)}$ is typically 26 V, also from the UCC28600 data sheet, $V_{DD(uvlo)}$ is typically 13 V, C_{OUT} is the total output bulk capacitance of the converter, V_{OUT} is the output voltage of the converter, R_Z is equal to the bias resistor of the opto-coupler diode, and V_Z is equal the zener voltage of the bias for the opto-coupler. Typically, a bias capacitor value of 22 µF is used.

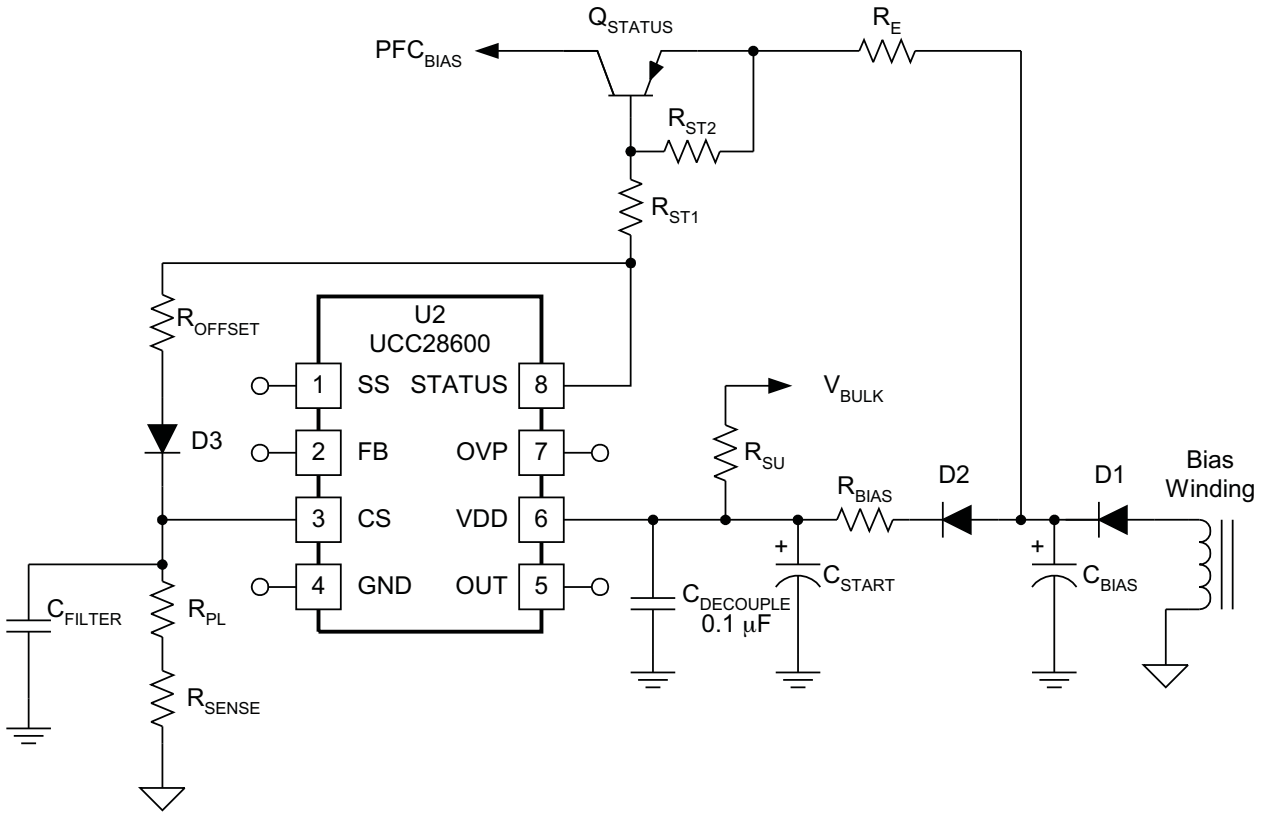

Figure 5. Biasing the UCC28600 and Providing PFC Bias Through Q_{STATUS}

4 Audio Noise

Even though the minimum switching frequency of the UCC28600 is 40 kHz, which is beyond the audible range, the burst packets are at frequencies much less, and well-within the audible range. Injecting an offset voltage into the CS pin during green mode effectively reduces the current that is switching in the flyback transformer while the converter is operating in this audible range because this offset effectively shifts the burst operating mode to a lower operating range. The transition from burst to FFM occurs sooner and less current will be allowed to excite the transformer within the audible range. The STATUS pin allows for an easy and effective way of injecting this offset only during the burst operating mode. Careful selection of the R_{ST1} and R_{ST2} resistors is required so as to allow an offset voltage into CS through R_{OFFSET} and D3 but not cause Q3 to turn on during green mode. The needed offset voltage can be determined by setting the working converter, with the R_{OFFSET} reference designator open, at its noisiest operating point and adding in a voltage from a separate bench supply into D3 until the audio noise is minimum; a 100-mV offset reasonably reduced the audible noise on the tested module. Calculation of the component values for applications using Q_{STATUS} to provide bias for a PFC front end, is as follows:

$$I_{OFFSET} = \frac{V_{CS(offset)}}{R_{PL} + R_{CS}}$$

Where $V_{CS(offset)}$ is the determined offset voltage needed to be added to CS for audio noise reduction, R_{PL} is the power limit resistor, and R_{CS} is the current sense resistor.

$$R_{ST2} = \frac{V_{BE(off)}}{I_{LEAK} + I_{OFFSET}}$$

$V_{BE(off)}$ is the maximum base-emitter voltage allowed across Q_{STATUS} and still be completely off, 0.2 V is typically used, I_{LEAK} is the leakage current into the STATUS pin and is 2 μA maximum, I_{OFFSET} is calculated above.

R_{ST1} is calculated during the Q_{STATUS} on state (in saturation), where STATUS is low impedance, and D3 is reverse biased. Setting $V_{BE(sat)}$ to 0.85 V, $R_{DS(on)}$ is the maximum STATUS $R_{DS(on)}$, reported in the data sheet to be 3.8 kΩ, V_{IN} is the minimum bias winding voltage, I_C is the collector current which will be equal to the bias current for the PFC controller, β_{SAT} = 10, I_B is the base current, equal to I_C/β_{SAT}, R_E is the emitter resistor, equal to 49 Ω, $I_{RST2(on)}$ is equal to the current through R_{ST2} when Q_{STATUS} is in the on-state:

$$I_{RST2(on)} = \frac{V_{BE(sat)}}{R_{ST2}}$$

$$R_{ST1} = \frac{V_{IN} - R_E\left(I_C + I_B + I_{RST2(on)}\right) - V_{BE(sat)}}{I_B + I_{RST2(on)}} - R_{DS(on)}$$

R_{OFFSET} is solved using the off state of Q_{STATUS}:

$$R_{OFFSET} = \frac{V_{IN} - V_D - \left(I_{OFFSET} + I_{LEAK}\right)\left(R_E + R_{ST2} + R_{ST1}\right)}{I_{OFFSET}} - R_{PL} - R_{CS}$$

Where V_D is the forward drop across D3.

Audible noise in the converter can also be reduced by using a film capacitor in the R^2CD snubber circuit instead of a ceramic capacitor. Ceramic material is inherently permanently polarized and therefore has a piezoelectric response in the presence of any applied voltage or mechanical stress and will produce a sound. As a better alternative to the R^2CD snubber, using a Zener clamp circuit, as shown in Figure 6, generally increases the efficiency and becomes quieter, although an RC snubber may still be needed if there is excessive ringing in the converter.

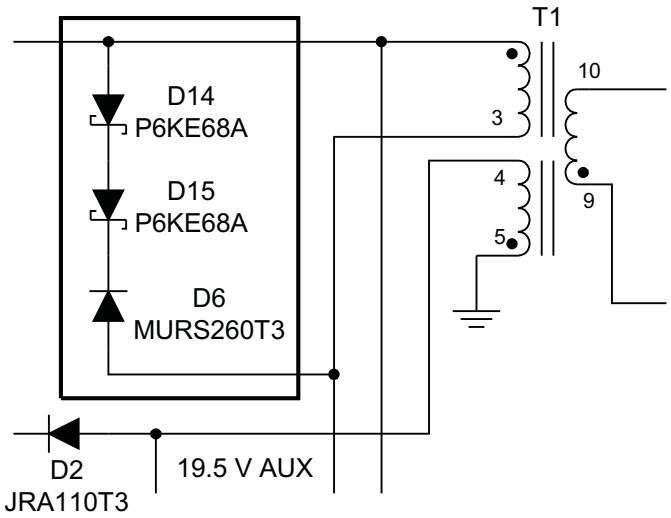

Figure 6. Zener Clamp Snubber

Refer to Transformer Design Considerations (Chapter 2) for more suggestions on reducing the audible noise on the converter.

5 Other Various Layout Considerations

Here is a variety of suggestions for the layout of the converter. These suggestions are in no particular order of importance, most are well-known and are generally good practices that can be applied to any converter design, others were learned the hard way and passed on to help a fellow designer. All should be considered prior to layout.

- It is expected that this device is primarily used in applications with single layer copper PCBs which, unfortunately, limits the use of ground planes. As in any converter, the board layout plays a critical role in performance. Minimize the high current loop to reduce parasitic capacitances and inductances. At the same time, do not inadvertently make traces with a high dv/dt too wide as this creates a very good E-field antenna.
- Separating the device's signal ground from the high current power ground is also required in order to isolate the noise away from the device's substrate. The separate grounds should, ideally, be tied together at the bulk capacitor on the primary side.
- Returning the sense resistor to the input capacitor, instead of to the ground plane under the device is required for a successful design.
- The decoupling capacitor on VDD, $C_{DECOUPLE}$ in Figure 5, must be placed as close as possible to the VDD and GND pins of the device.
- Also, the FB components should be tightly arranged with short connecting traces and as far away from noise as possible.
- Use a 0.025 inch or greater trace for the gate drive, with traces as short as possible, avoid right angles, route on one layer if possible.
- Use a small value gate drive resistor to in series with the gate drive to control the turn on transition time and reduce the dv/dt ringing on this node.
- A 10-kΩ resistor is placed between the gate of the MOSFET and ground to discharge the gate capacitance and protect against inadvertent dv/dt triggered turn-on.
- Adding a small capacitor, C_{FILTER} shown in Figure 5, to the CS pin effectively creates an RC low pass filter in conjunction with the power limit resistor and will improve noise immunity at the current sense pin.

6 Measuring No-Load Power

Because the input currents and power quantities are very small when the converter is operating in green mode, certain considerations must be made when trying to measure the no-load input power. Presently, the EnergyStar criteria for external power adapters states that converters with a rated output power of less than 10 W must have a maximum measured input power of 0.5 W or less under no-load conditions and converters with a rated output power of 10 W to 250 W must have a maximum measured input power of 0.75 W or less under no-load, or standby conditions. Accurately measuring the input current, typically less than 10 mA, at universal line voltages at such low power levels is often beyond the dynamic range capability of most power meters. The UCC28600 will be operating in green mode, where the converter draws power in 40-kHz burst packets that are spaced tens of milliseconds apart. These intermittent bursts of current and power drawn from the line will result in inconsistent measurements from the power meter.

Figure 7 shows the equipment set up for no-load power measurements. Low power measurements were taken with a Voltech PM100 using a 10-Ω external shunt and a scale factor of 10000 mV/A. Long averaging mode, set to 10 seconds, is used to display continuous measurements taken at a high sample rate and averaged over an extended time period. In this way, several hundred burst packet cycles are measured for an accurate representation of input no-load power.

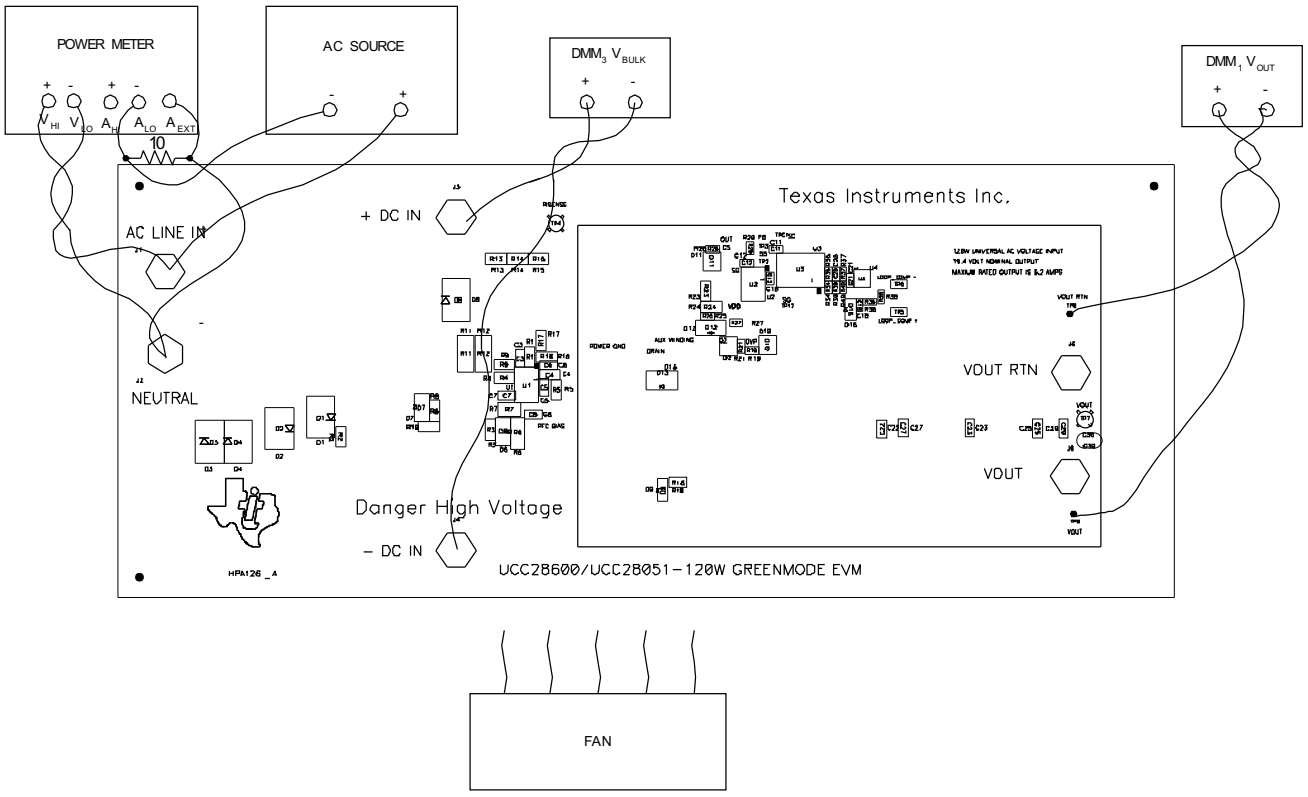

Figure 7. Equipment Set Up for Accurate No-Load Power Measurements

7 Loop Compensation

The feedback network uses an opto-coupler and shunt regulator for closed loop control. The collector of the opto-coupler is tied directly to the feedback (FB) pin of the UCC28600. The FB pin has an internal 20-kΩ pull-up resistor to the internal 5-V reference of the device. Maximum duty cycle is achieved when FB is high and zero duty cycle occurs when FB is low. The voltage on FB plays a key role in determining what mode the converter is in. Placing a capacitor on FB provides a delay time for over load protection, as shown in Figure 8. Using a 390-pF capacitor gave adequate delay without adversely effecting performance. Values much larger than this should be avoided.

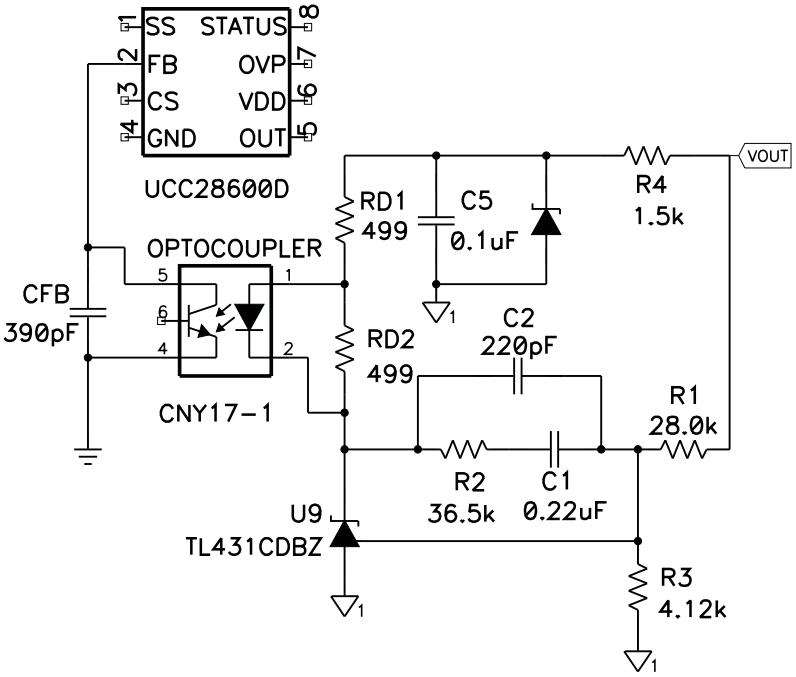

Figure 8. Typical Loop Compensation for the UCC28600

As shown in Figure 8, the UCC28600 uses a Type II compensation scheme that would be applicable to most discontinuous mode flyback converters. The TL431 shunt regulator is biased off of the output voltage. Resistor values for R4, RD1, and RD2 can be massaged in such a way as to run at minimal power levels. This is helpful when designing a circuit that must meet stringent no-load input power requirements; even during open circuit operation, the TL431 and opto-coupler must be biased and will consume power.

Due to the various modes of operation of the UCC28600, the switching frequency of the green-mode controller will vary, yet the compensator is static. The actual crossover frequency of the converter varies by more than three-to-one for a universal ac line input. The crossover frequency of the control loop determines the period of the pulses in the burst packets during light load operation. A higher crossover frequency results in fewer pulses in a burst packet, and the burst packets will have a shorter period. The period of the burst packets impacts the selection of the primary bias capacitor of the UCC28600 as this capacitor must have a holdup time long enough to not trigger the UVLO off threshold of the device.

The theoretical maximum crossover frequency is limited to one-fifth of the minimum switching frequency of the converter, which is 40 kHz in the UCC28600. Because the crossover frequency will vary three-to-one during its full range of operation, designing the loop crossover frequency to be between 2 kHz and 3 kHz at nominal input voltage and 50% load with a phase margin of 70% to 80% should satisfactorily stabilize the loop for the entire range of operation. One basic approach to select compensation components is to place a relatively large ceramic capacitor (0.1 μF for example) across the error amplifier and measure the Bode plot at nominal input voltage, 50% load and then mathematically subtract out the effect of the capacitor in order to determine the transfer characteristic of the power stage at that particular operating point. Then it is possible to calculate the appropriate components for the pole and zero placement in order to achieve the desired frequency response. Figure 9 shows the final Bode plot for a 120-W offline converter with a resultant crossover frequency of 2.5 kHz and a phase margin of 70 degrees.

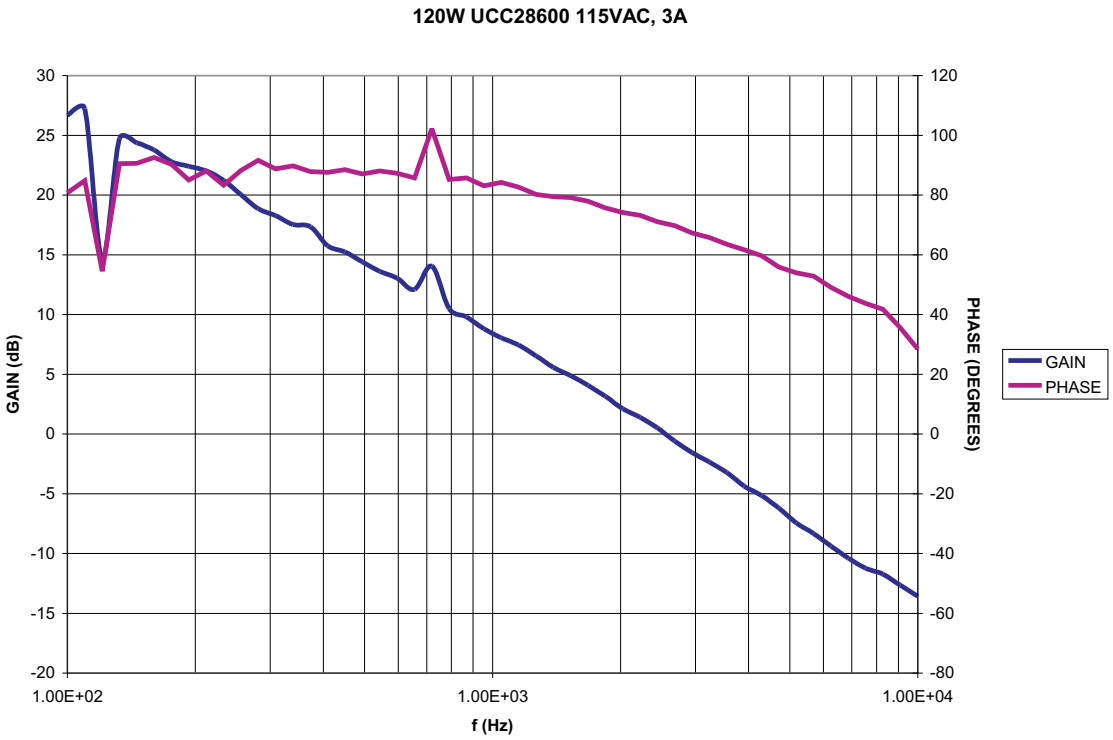

Figure 9. Bode Plot for a 120-W Offline Converter

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