# TECHNICAL NOTE

## POWER SOLUTIONS FOR DDR2 NOTEBOOK PCs

*In cooperation with* TEXAS INSTRUMENTS

## Overview

This technical note provides a general guideline for designing the DDR2 memory power circuitry. It includes the DDR2 voltage requirements and encompasses a sample reference design focused on the Texas Instruments Incorporated (TI) TPS51116, a complete DDR2 memory power solution which includes a synchronous buck controller, 3A linear droput regulator (LDO), and buffered references.

## DDR2 Advantages for Notebooks

DDR2 memory is an excellent solution for notebook computers. The greatest advantage it has over older technologies is its reduced power consumption which results in cooler operating temperatures and extended battery life. (See Figure 1, below.) Reduced power consumption combines many design features, including lower operating voltages, reduced page sizes, and 4n-prefetch support.

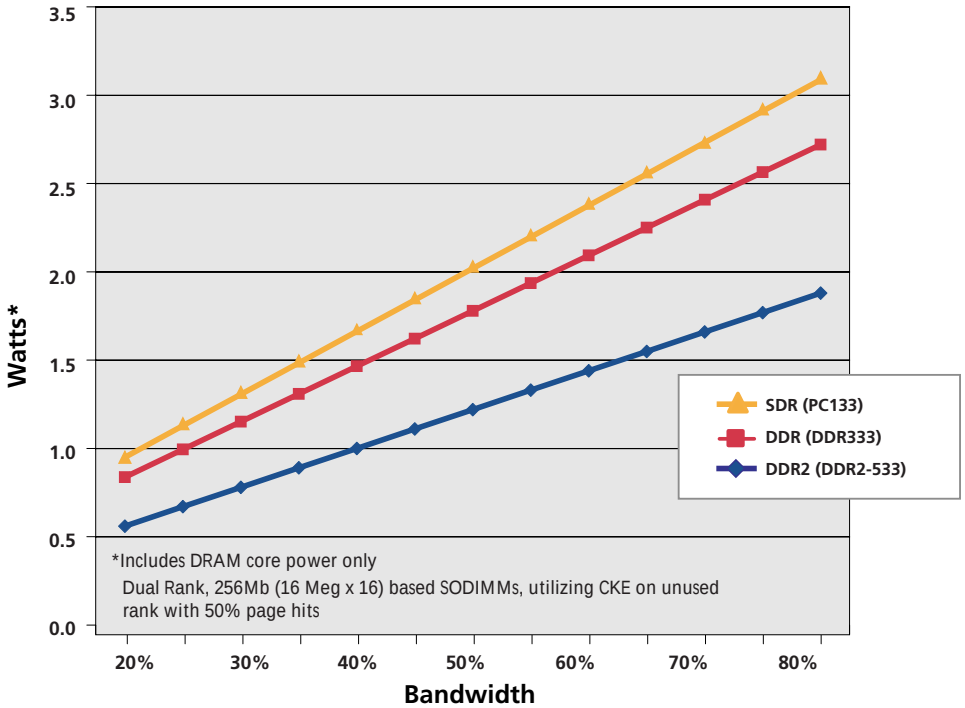
DDR2 memory utilizes a low operating voltage of only $V_{DD}$ = $V_{DD}Q$ = 1.8V and supports a SSTL_18 I/O interface. The page sizes for DDR2 have also been reduced to help minimize the activation current. Finally, it supports a 4n-prefetch which allows the device core to run at a slower frequency while driving an ultra-fast data rate (DDR2 currently supports 667 MT/s/b).

Other advantages of DDR2 memory for notebooks include higher-density in the same space. Aside from the voltage key placement and pinout change, the DDR2 SODIMM uses the same 200-pin socket as DDR.

At the device level, DDR2 components will be manufactured at individual memory densities up to 2Gb (at the component level this reflects a 128Mb x 16 or 256Mb x 8 device), which means that it supports an 4GB channel with just two slots.

Also new with DDR2 memory is on-die-termination (ODT) which has a significant impact on signal quality and power dissipation. ODT allows the controller to more effectively manage the termination to the high-speed signals where and when it is needed.

**Figure 1: Power Performance Curves on SDR, DDR, and DDR2**



## DDR2 Notebook Assumptions

JEDEC has defined four standardized small outline, dual in-line memory modules (SODIMMs) that include single- and dual-rank DIMMs which utilize either x16 or x8 devices. These are all 64-bit wide unbuffered SODIMMs with predefined electrical and mechanical specifications.

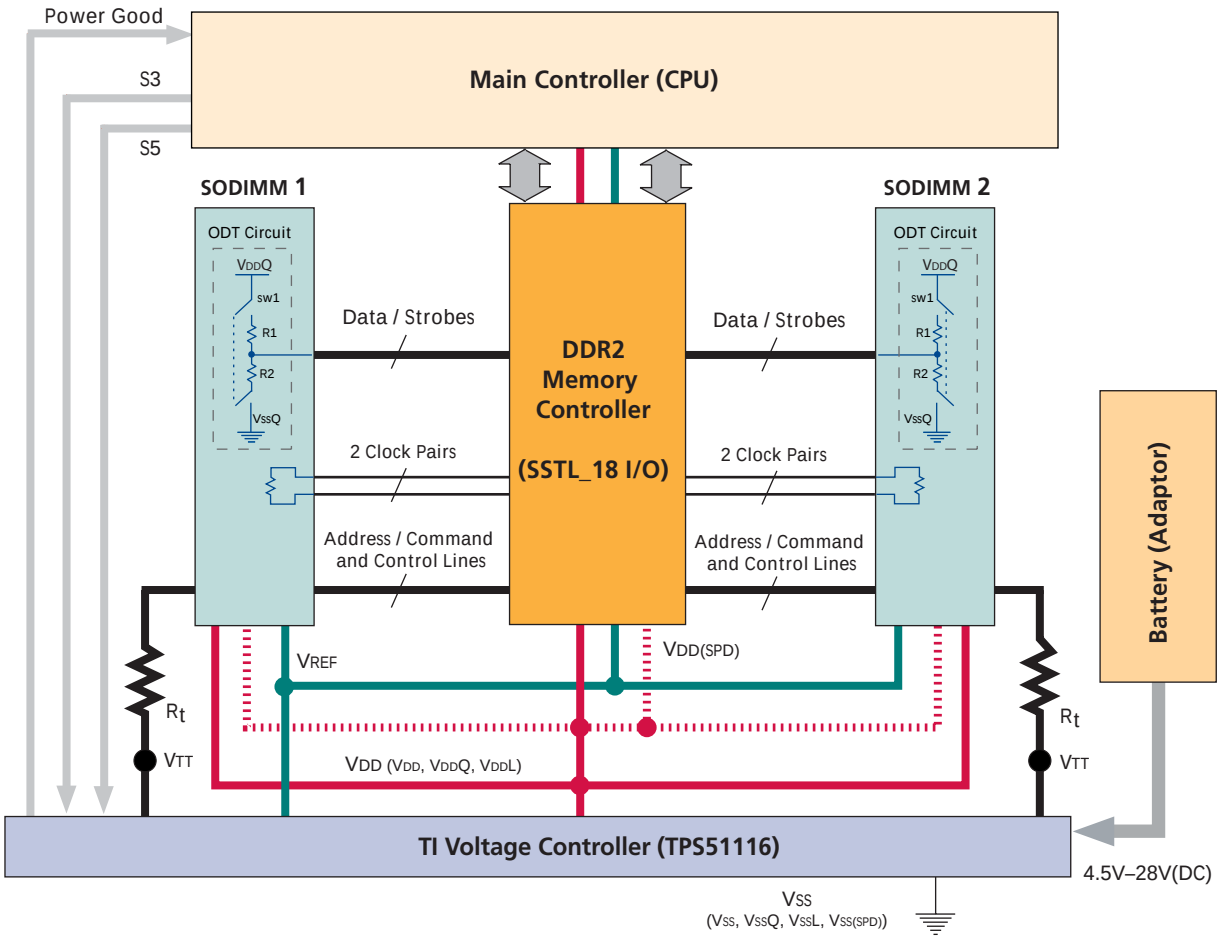
This technical note assumes the notebook-system designer will utilize a dual memory channel with two slots, one per channel (see Figure 2, below). It is expected that for a dual-channel, two-slot system both the address and command lines will be terminated at VTT through a resistor. All of the high-speed data strobes and data signals will utilize localized ODT. On the module the differential clock pairs (CK/CK#) are differentially terminated.

This combination makes for a low-cost, low-power application that maximizes battery life while maintaining a small size and high-performance system.

## DDR2 Voltage Requirements

One challenge of designing a DDR2 system is to meet the strict power requirements and predefined power-up and initialization sequences as defined by JEDEC (JESD79-2 DDR2 SDRAM Specification). As such, it is critical that the initial power ramps be controlled to meet specifications. In addition, both the termination voltage (VTT) and reference voltage (VREF) must maintain their respected relationships to VDD at all times. The following pages will provide detailed voltage requirements for DDR2 notebook systems.

**Figure 2: Functional Block Diagram of a Dual-Channel, Two-Slot DDR2 Notebook**



## Supply

### VDD (VDD, VDDL, VDDQ)

The DDR2 device requires a single power source for primary supply voltages. This ensures that all voltage levels track each other, especially during the power ramp. At the module level, VDD (device core), VDDL (device DLL), and VDDQ (device I/O) share a single power plane with the interconnecting pins labeled as VDD. Likewise, VSS, VSSL, and VSSQ share a common ground plane labeled as VSS.

The memory supply voltage is specified as VDD = VDDQ = 1.8V with a DC tolerance of ±100mV. DC is defined as any signal less than or equal to 20 MHz. At the initial power up, all supply power should be stable and meet specification within 10ms or less.

The amount of current each module will consume depends on the density and speed of the module, number of ranks, and most important, the usage conditions. For example, to build a high-density dual-rank module using (x8) DRAMs, sixteen individual devices are required. A system utilizing two of these modules and running a heavy-use condition may consume up to 7W–8W. However, the same system, using one lower-density, dual-rank module using (x16) DRAMs, will only have eight discrete components each and under moderate use conditions, might only consume a total of 1.5W–2W. As such, Micron has a dedicated technical note and a custom DDR2 power calculator which provides additional information on how to estimate actual module power usage. Access the calculator tool and the technical note on Micron's Web site at **www.micron.com/systemcalc**.

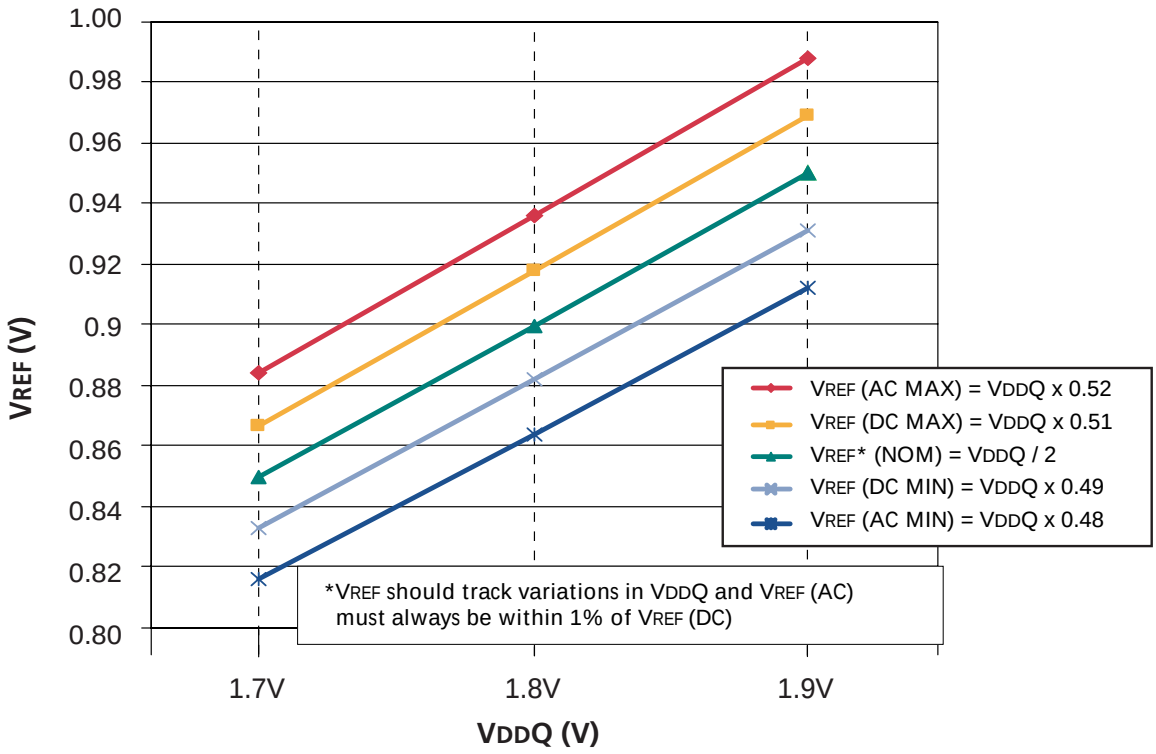
### VREF

Another key supply voltage is the input reference voltage (VREF). All DDR2 input receivers are calibrated to operate within the specified VREF input levels. For proper device operation, it is critical that the VREF input is free from excess noise or voltage variations. Any degrading of the VREF input voltage will directly affect the setup and hold times of the DDR2 device.

VREF is expected to equal VDDQ/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise (non-common mode) on VREF may not exceed ±1% of the DC value. Peak-to-peak AC noise on VREF must not exceed ±2 percent of VREF (DC). AC noise is defined as any noise over 20 MHz in frequency. There is virtually no current draw on the DDR2 VREF pin; only leakage current is present (less than 5µA per DRAM component).

Figure 3, below, shows the industry-standard voltage specifications and tracking requirements for VREF.

**Figure 3: Required VREF Voltage Relationships**



### VTT

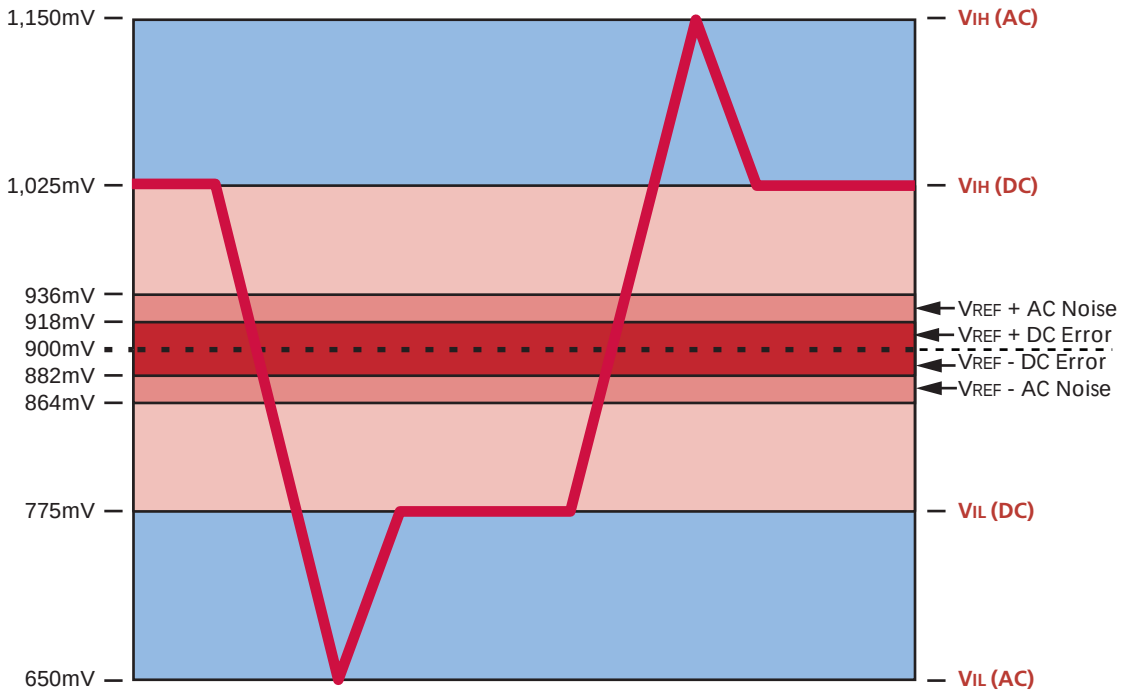
DDR2 memory is optimized for stub series terminated logic at 1.8V (SSTL_18) operation. The address, command, and control lines require system-level termination to a midpoint voltage. This midpoint voltage is called VTT (or the I/O termination voltage). By having the termination sit at midpoint, it ensures symmetry for switching times. It is important that VTT tracks any variation in the DC levels of VREF. By specification, at all times, VTT must equal VREF ±40mV. The termination voltage (VTT) is supplied directly to the motherboard and not the module. See Figure 4, below, for logic levels of a properly terminated SSTL_18 signal.

### ODT (On-Die Termination)

As previously indicated, the high-speed, bidirectional signals (data and strobes) are uniquely terminated with on-die-termination (ODT). ODT is new for DDR2 and allows for the most optimal signal quality possible (see Figure 5 on page 5). This is done by dynamically controlling the exact termination value where and when it is needed. For example, the ideal placement for termination is at the end of the active signal trace. So, when WRITING to SODIMM1, the memory controller will dynamically disable the ODT function on SODIMM2, memory controller (both buses), and activate the ODT circuitry on SODIMM1 (at the end of the active transmission line). Likewise, during a READ from either SODIMM, the memory controller will dynamically disable the ODT circuitry at both SODIMM locations and enable ODT circuitry on the active bus at the memory controller. This facilitates a much-simpler board design using fewer components and less cost.

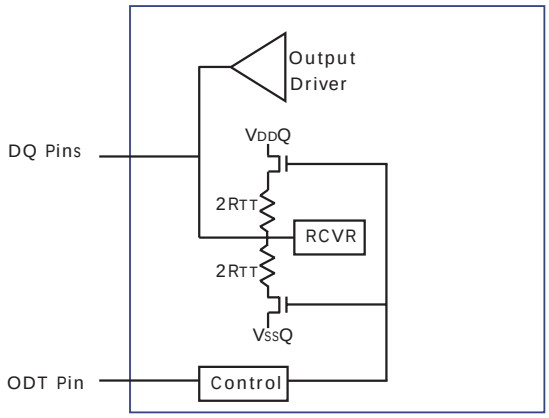
ODT allows better thermal and power management control. For example, during DRAM inactive times, most memory controllers will completely disable the termination to conserve power.

**Figure 4: SSTL_18 Single-Ended Input Logic Levels**




Note: Numbers in diagram reflect nominal values (VDD = VDDQ = 1.8V).

**Figure 5: Functional Block Diagram of ODT**




### VDD(SPD)

Although not utilized for the DRAM, there is one other power requirement for the SODIMM. This is the power for the serial present detect (SPD) EEPROM, which holds the module operating parameters. This voltage (VDDSPD) has a wide-range tolerance from +1.7V to +3.6V. In its worst case, the current draw of this pin should be no more than 3mA–4mA.

## Power Management for Notebooks with Micron DDR2 and TI's TPS51116

Designers who use Micron's DDR2 memory modules can now incorporate TI's new TPS51116. The TPS51116 is an integrated power management solution which combines a DC/DC current mode switching controller with a 3A sink/source linear dropout regulator (LDO). This highly-integrated device significantly reduces the number of external components typically required to support all the power management for DDR2 memory systems, making the TPS51116 easy to use while offering a smaller total-solution size and lower total-solution cost without sacrificing performance.

## TPS51116: A Solution for Complete DDR2 Power Management

Figure 6 shows a typical application schematic for the TPS51116, illustrating how the TPS51116 integrates the complete DDR2 power management solution with:

- Synchronous current mode DC/DC controller to power VDD
- Buffered reference to provide VREF (VREF tracks one-half VDD)
- 3A sink/source LDO to power VTT, (VTT tracks VREF)
- S3/S5 sleep state controls

This high-level integration simplifies the design of the power management segment of DDR2 memory. This places the burden on the TPS51116 to meet the industry-standard specifications and the proper management of S3 and S5 states.

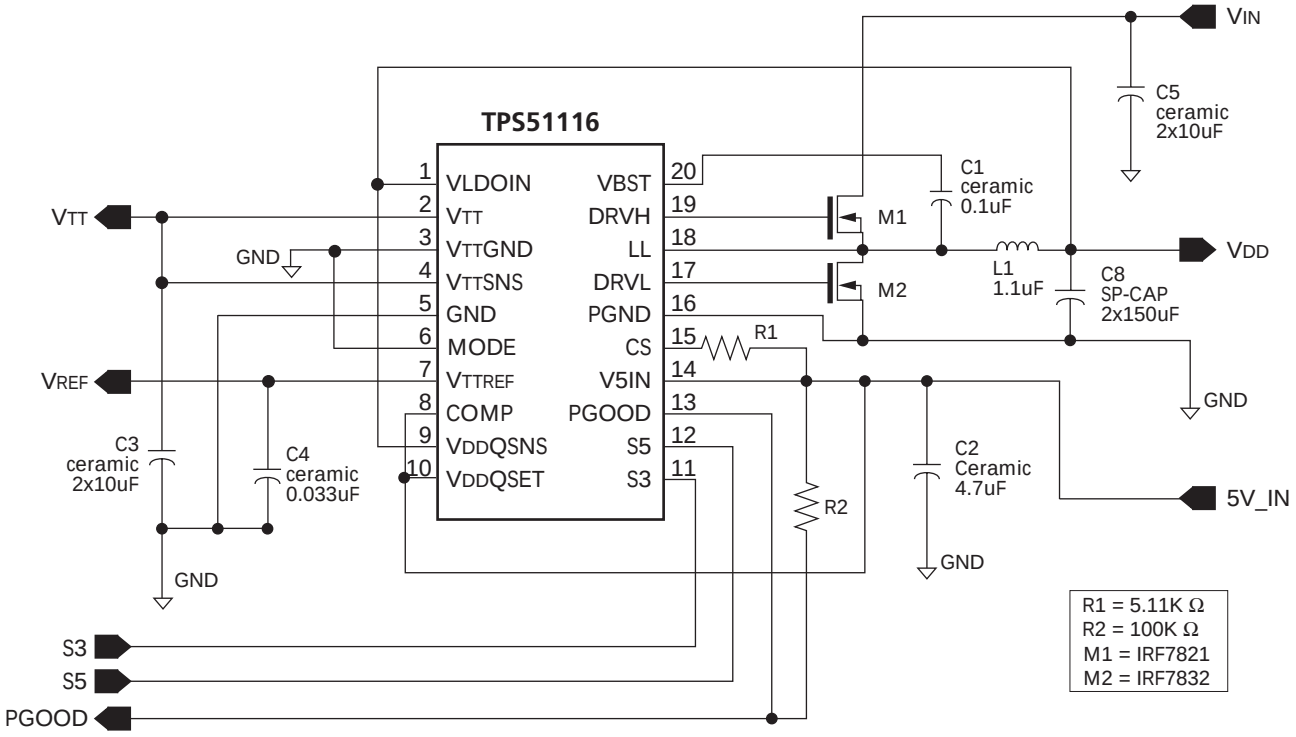
The synchronous current mode DC/DC controller is used to power VDD/VDDQ. Implementing the power supply requires two external NFETs, in addition to an inductor and input/output capacitors. This output is used to power DDR2 memory's VDD/VDDQ and is able to achieve high efficiency during wide load variation—expected to range from 10mA to 10A.

The output of TPS51116's switcher is internally divided down by one half and is used to generate VREF. The VREF output tracks changes in VDD/VDDQ with a high level of accuracy, achieved by the precisely-matched internal resistor divider. VREF is buffered, and this helps to increase its immunity to noise and changes in load. This is critical in maintaining the stringent VREF to VDDQ tracking requirements of the DDR2 device.

The final output voltage rails required for DDR2 is for VTT. The power for this rail comes from the LDO segment of the TPS51116. The LDO supports 3A peak current and has 1.5A continuous current capabilities.

This LDO can sink/source current and meet the industry-standard specifications with only 2x10uF ceramic output capacitors. DDR2 allows the use of an LDO to power termination (VTT) because of the reduction of required current, due to the implementation of ODT.

**Figure 6: Typical Application Circuit for TPS51116**




## Line Regulation, Load Regulation, and Transient Response

As stated previously, the industry-standard specifications must be met to power DDR2 memory. Below are the voltage tolerances that need to be supported throughout the changes in input voltage (line regulation), output current (load regulation), and transient response, as defined:

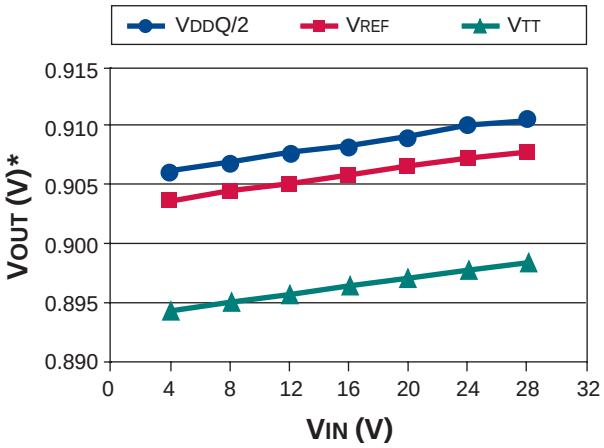
- VDDQ = 1.8V ±100mV
- VREF = 0.49 VDDQ/0.51 VDDQ
- VTT = VREF ±40mV

Line regulation ensures the tolerances are maintained when the input voltage changes. Figure 7 shows as the input voltage changes from 4V to 28V, VDDQ only changes a few millivolts (spec is ±100mV). VREF tracks VDDQ/2 and there is only about a 10mV difference between VTT and VREF (spec is ±40mV).

Load regulation and transient response is ensuring the tolerances are maintained when the output current changes. Load regulation is a static test condition and transient response is a dynamic test condition.

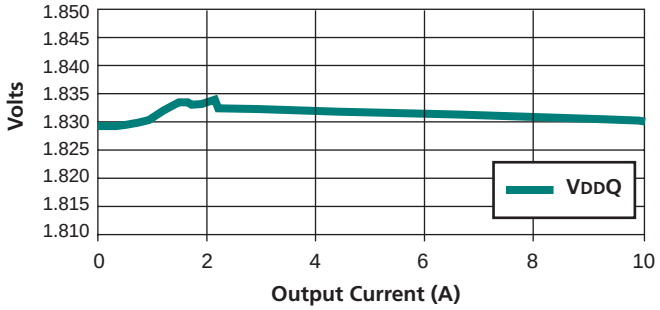
Figure 8 on page 7 shows VDDQ with a static load change from 0A to 10A on VDDQ, with its output voltage is less than 35mV from 1.8V (specification is ±100mV). In Figure 9 on page 7, the load changes from -1.5A to 1.5A on VTT, and VDDQ is about 25mV from 1.8V (specification is ±100mV), with VTT–VREF near ±20mV (specification is VREF ±40mV).

**Figure 7: Line Regulation All Three Outputs**

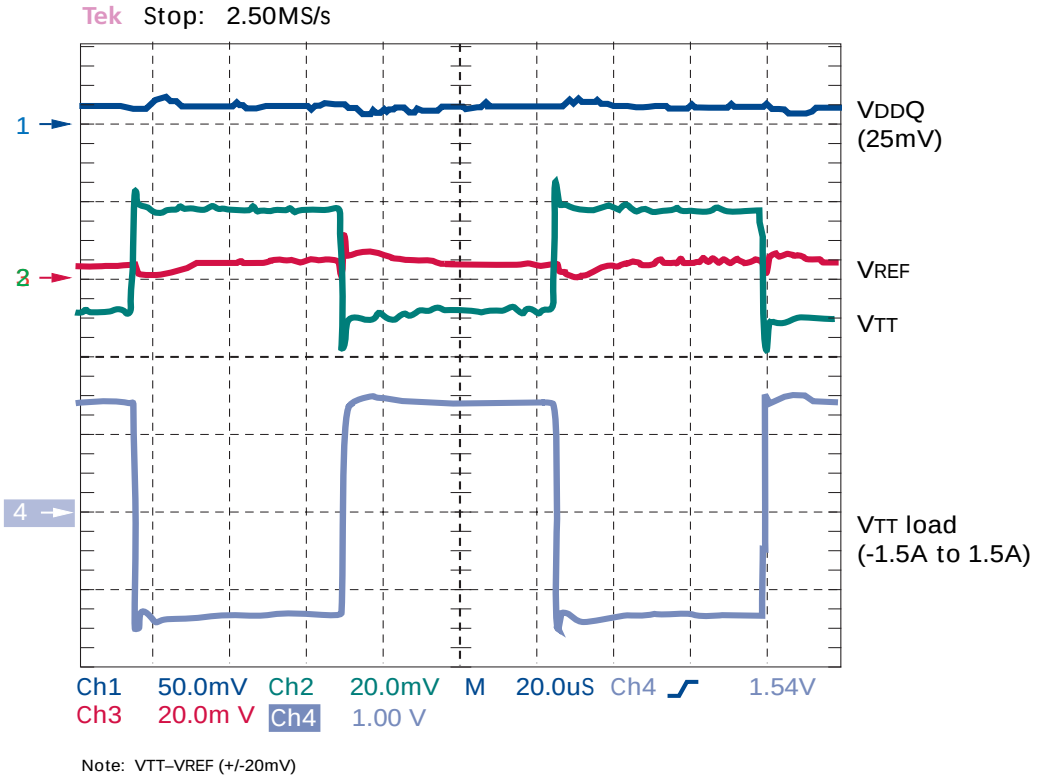



* Test was performed with a 7A load on VDDQ/2 and a 0.3A load VTT

## Figure 8: Load Regulation
## VDDQ Only (VIN = 12V)




## Figure 9: Transient Response
## (VIN = 12V)




Note: VTT–VREF (+/-20mV)

## TPS51116 Manages the Critical Relationship Between VTT/VREF and VDDQ

TI's TPS51116 has a very important role when it comes to managing the sleep state functions, which exists in the notebook. Where DDR2 memory is concerned, it is critical during both start-up and shutdown that VDDQ is always higher than VTT/VREF. If the condition were to occur where VTT/VREF is greater than VDDQ + 0.3V, then the DDR2 memory could run the risk of latching up. Using the TPS51116 to power the DDR2 memory ensures that this condition will not occur.

This is achieved by taking advantage of the integrated sleep state functions within the TPS51116. The S3 and S5 pins that exist on the TPS51116 are simply connected to the S3 and S4/S5 control signals which exist in the notebook computer (Figure 2 on page 2). With the S3 and S5 pins, all the sleep state functions can be managed. Below is a summary of the sleep state modes:

- S0 = Full On
- S3 = Suspend-to-RAM (STR)
- S4/S5 = Suspend-to-DISK (STD)/Soft-Off

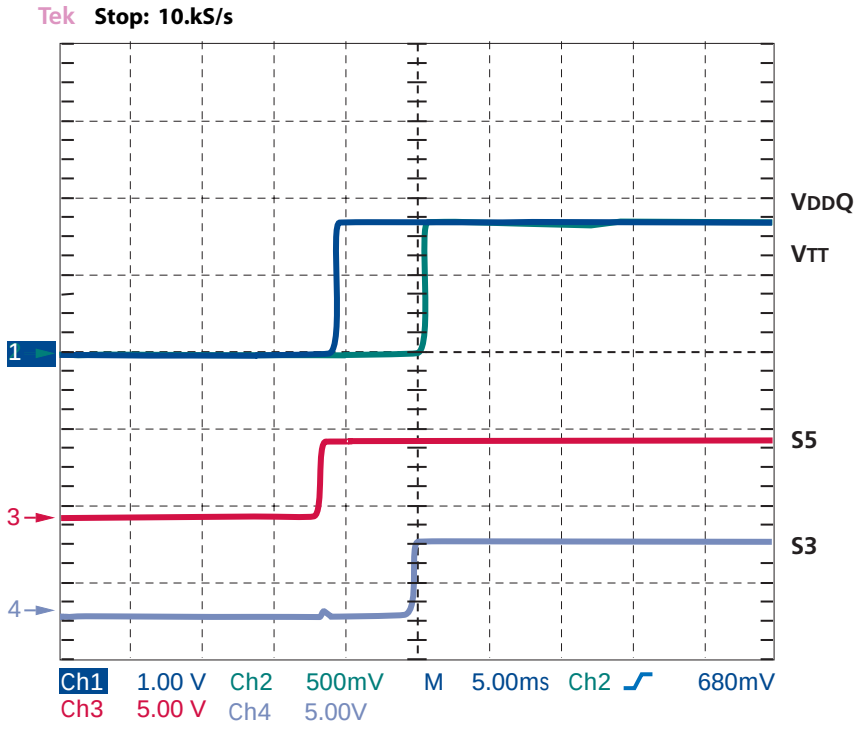
A summary of how the TPS51116 handles the sleep state modes is provided in Table 1.

When transitioning from an S4/S5 state (STD) to S0 (Full On), S5 will go HIGH first, then S3 will go HIGH. Figure 10 shows when S5 goes HIGH, VDDQ turns on, and when S3 goes HIGH, VTT will turn on. During start-up, VTT can not turn on until a VDDQ voltage exists and as soon as VDDQ voltage turns on, the VTT voltage will track VDDQ. Therefore, during start-up, VDDQ will always be greater than VTT.

**Table 1: S3 and S5 TPS51116 Input and Output Parameters**

| STATE | STATUS | INPUTS | | OUTPUTS | | |
|---|---|---|---|---|---|---|
| | | S3 | S5 | VDDQ | VREF | VTT |
| S0 | FULL ON | HIGH | HIGH | On | On | On |
| S3 | SUSPEND-TO-RAM (STR) | LOW | HIGH | On | On | Off (High-Z) |
| S4/S5 | SUSPEND-TO-DISK (STD)/SOFT-OFF | LOW | LOW | Off (Discharge) | Off (Discharge) | Off (Discharge) |

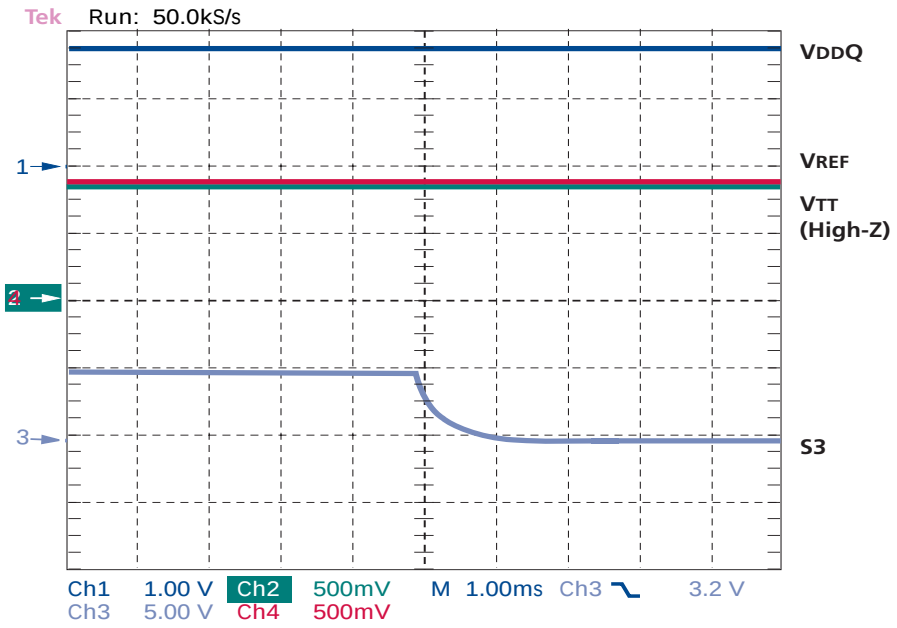
**Figure 10: Full-On Power Ramp**



During an S3 state, the S3 control signal will go LOW and the system will enter a Suspend-to-RAM state (STR). STR can only occur after the DRAM has been properly placed into self refresh mode. This requires a predefined series of command sequences (turn off ODT, precharge all banks, synchronously take CKE LOW with the AUTO REFRESH command). Please see any Micron DDR2 data sheet for all requirements.

The STR or self refresh mode is the lowest DRAM power state. If the proper command sequences are followed and all supply voltages are kept within their specified limits, then the DDR2 DRAM will preserve the data contents indefinitely. During this state, $V_{DD}$/$V_{DDQ}$ and $V_{REF}$ remain on and $V_{TT}$ enters a high impedance state (High-Z). The $V_{TT}$ output no longer sinks or sources current and is floating. This is shown in Figure 11, below.

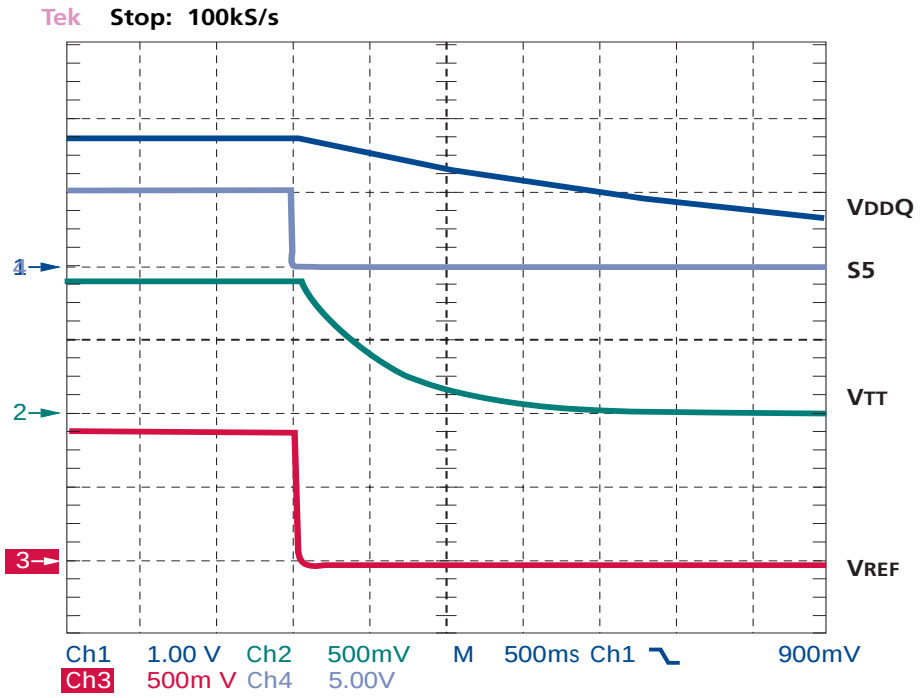
**Figure 11: Enter Suspend-to-RAM**




Note: During Suspend-to-RAM, all supply voltages must be maintained within specified data sheet values, including $V_{REF}$. $V_{TT}$ is not required during STR.

For the TPS51116, to enter a Suspend-to-DISK (STD), the S5 signal must go LOW. During the STD (S4/S5 state) there is no power supplied to the DRAM and all DRAM data is lost. It is critical that upon the exit of STD the DDR2 memory is powered up correctly with a full initialization sequence. This includes the ramp-up of supply voltages and maintaining the required voltage relationships as discussed in the previous sections of this technical note. After all supply voltages are steady, there must be 200µs of stable clocks before CKE goes HIGH and the DRAM initializations sequence is started. See any Micron DDR2 data sheet for expanded DRAM initialization requirements. During the STD, all TPS51116 outputs discharge to GND, including VDD/VDDQ, VTT, and VREF. The TPS51116 has been designed to ensure that VTT and VREF discharge more quickly than VDDQ to guarantee VDDQ will always be greater than VTT/VREF. This is shown below in Figure 12.

**Figure 12: Suspend-to-DISK**




Note: After the DRAM has been properly shut down, all supply voltages may be removed and DRAM contents will be lost.

## Load Efficiency

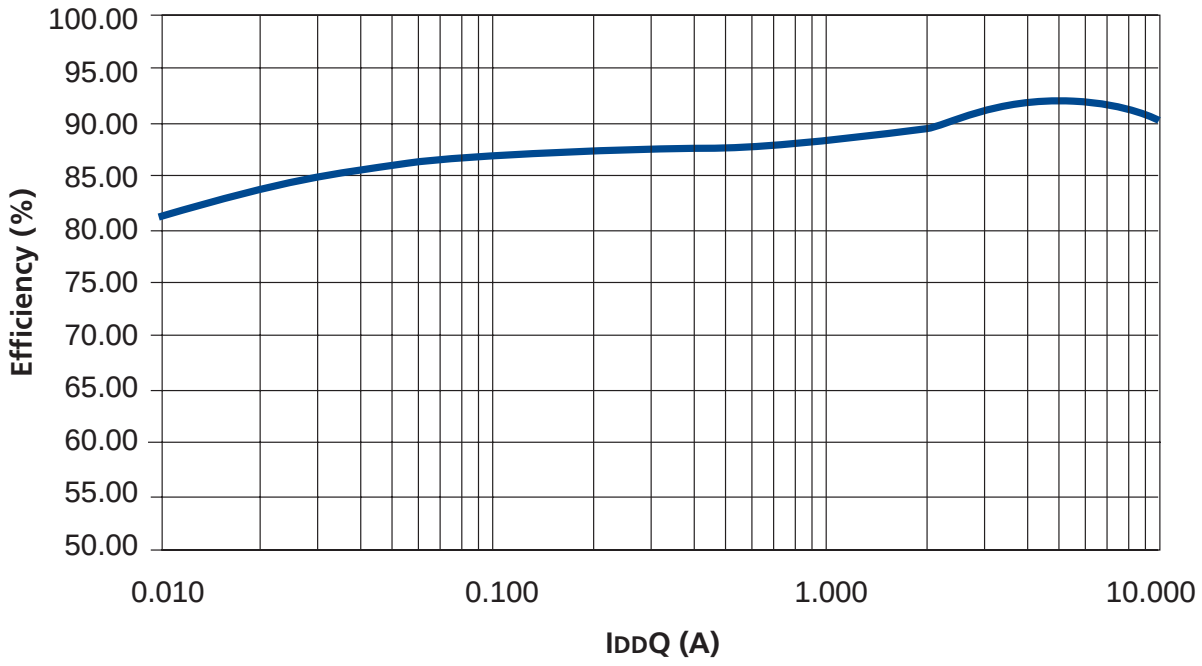
The TPS51116 has a high level of integration. The integration makes using the TPS51116 very easy and offers a smaller total solution size and lower total solution cost without sacrificing performance. One of the most important performance features is the efficiency of the switcher, which is used to power VDD. High efficiency at full loads—such as 10A—is important in reducing the total power dissipation and in extending battery life within the notebook computer.

A reduction in total power dissipation translates to a reduction in cost and size. The higher the efficiency, the longer the battery will last when the notebook is on or in an active state. The TPS51116 efficiency at 10A is 90 percent (input voltage at 12V), which is considered very high. This can be seen in Figure 13.

High efficiency at light loads—such as 10mA—is typically found during a standby condition and is critical in extending battery life when the notebook is in a standby mode. The higher the efficiency, the longer the battery will last while in standby. The TPS51116 has exceptional light-load efficiency that achieves greater than 80 percent (input voltage at 12V). This, too, can be seen in Figure 13.

The TPS51116 can achieve this high level of efficiency at both 10A and 10mA because of its ability to adapt to the changes in load. At heavy loads—such as 10A—the high efficiency can be achieved because of the TPS51116 strong gate drive capability and the gate drive's adaptive dead-time control scheme. At light loads—such as 10mA—the TPS51116 enters skip mode, which is a mode that significantly reduces the switching frequency.

**Figure 13: Light Load and Full Load VDD/VDDQ Efficiency**



## Summary

DDR2 requirements, solution, size, and efficiency are most important when designing for power in a notebook computer. The TPS51116 is an ideal solution for powering Micron's DDR2 memory modules since it is optimized for low cost, is in a small total solution size, and has high performance.

The TPS51116 high-level integration requires only seven external resistors and capacitors, not including the power train for the switcher. Other solutions will use 18 or more external components, even if the switcher is integrated with the LDO. Typically, these notebooks will require separate power management ICs for $V_{DDQ}$ and $V_{TT}/V_{REF}$.

Texas Instruments' power products can be found at www.ti.com.

For notebook applications, DDR2 memory's high performance is unsurpassed. DDR2 supports ultra-fast data transfer rates with extremely-low operating power, dynamic ODT termination, and a small footprint.

With ODT, there is substantially less termination and signal routing on the motherboard. To ensure functionality, strict guidelines must be followed. As such, integrating a power solution for a reliable DDR2 notebook design can be challenging. The information within this technical note identifies for the designer the critical DDR2 voltages and establishes a method to implement power to the DDR2 memory channel.

For the latest data sheets, please refer to Micron's Web site at **www.micron.com/datasheets**.

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