



Control Driven Synchronous Rectifiers In Phase Shifted Full Bridge Converters

Application Note

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ABSTRACT

Driving a current doubler synchronous rectification output stage can be a very complex task, especially for a phase shifted full bridge topology. However, using the A and B outputs of the UCC3895 along with the UCC37324 dual 4-A MOSFET driver, direct PWM control of a synchronous rectifier current doubler output stage achieves. This technique provides the proper gating and timing signals necessary to accurately synchronize output switching to primary side bridge switching.

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1 Phase Shifted Full Bridge Switching Basics

Understanding the synchronous rectifier switching requirements requires some background in phase shifted timing fundamentals. In Figure 1, the full bridge comprises four primary side MOSFET devices labeled QA, QB, QC and QD. Power is transferred to the transformer secondary whenever any two diagonal switches, QA and QD or QC and QB, are on simultaneously. Conversely, whenever the two upper or lower switches, QA and QC or QB and QD are on simultaneously, this is known as the freewheel state. During the freewheel state it is important to note that the transformer primary is shorted, resulting in zero voltage across both the primary and secondary windings. Also, though not shown in the timing diagram of Figure 1, there is a finite delay between the turn off and turn on of QA and QB and QC and QD, when the resonant period occurs.

Neglecting delay times, four distinct switching states make up one full switch cycle of the phase shifted full bridge.

t₀→t₁: QA and QD are on, causing a positive voltage to appear across the transformer secondary dotted end. This corresponds to Q2 being on and Q1 being off, providing two separate current paths through L1 and L2. The transformer secondary current is equal to the current through L1, which is half the total output current. The second half of the output current is delivered via L2 freewheeling through Q2. Q2 is carrying the full load current during this state.

t₁→t₂: QA and QC are on, causing the voltage across the transformer, V_T to be zero. On the secondary side Q1 and Q2 are also both on. Notice also that the current in L2 has the same slope as the previous t₀→t₁ state, while the current in L1 has changed to a negative slope due to the voltage across L1 also becoming negative. Both L1 and L2 are now freewheeling. It is also important to note that since there is zero voltage across the transformer, the magnetizing current, I_M , does not change during this state.

t₂→t₃: QC and QB are on, causing a negative voltage to appear across the transformer secondary dotted end. This corresponds to Q1 being on and Q2 being off. The transformer secondary current is equal to the current through L2, which is half the total output current. The second half of the output current is delivered via L1 freewheeling through Q1. Q1 is carrying the full load current during this state.

t₃→t₄ = t₀: QB and QD are on, causing the voltage across the transformer, V_T to be zero. On the secondary side Q1 and Q2 are also both on. Notice also that the current in L1 has the same slope as the previous t₂→t₃ state, while the current in L2 has changed to a negative slope due to the voltage across L2 also becoming negative. Both L1 and L2 are now freewheeling. Similar to state t₁→t₂, since the transformer voltage, V_T is again zero, the magnetizing current, I_M , does not change during this state.

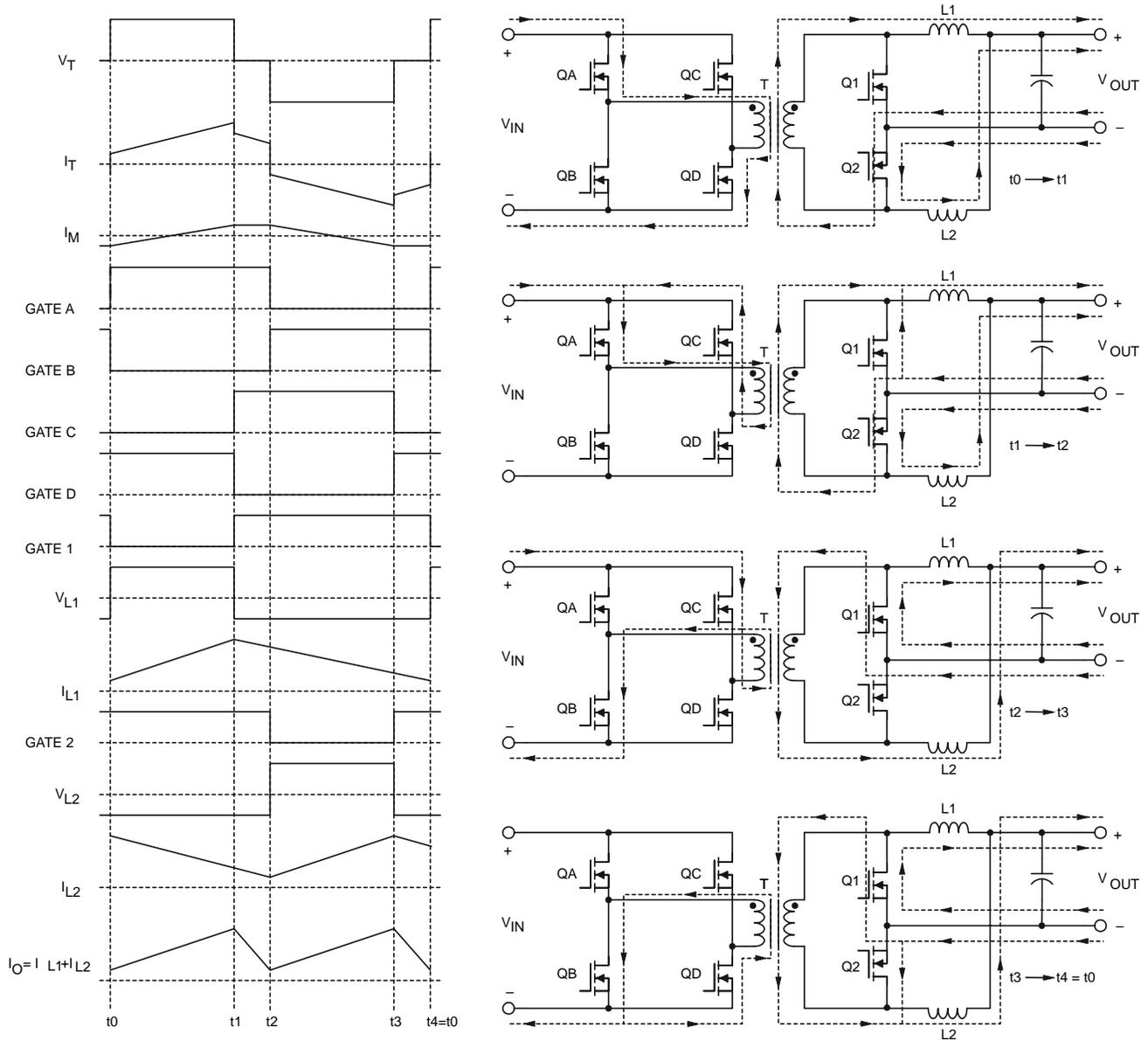


Figure 1. Phase Shifted Full Bridge with Current Doubler Timing Diagram

2 Synchronous Rectifier Switching Requirements

Traditionally, synchronous rectifiers are either self-driven, directly from the transformer secondary voltage, or control-driven, where the desired gate drive signals are derived from the pulse width modulator (PWM) controller. Since part of the phase shifted full bridge switching cycle contains a freewheel period, as noted in states $t1 \rightarrow t2$ and $t3 \rightarrow t4$ of Figure 1, there is no transformer voltage available for the synchronous rectifier gate drives during this period. Therefore, self-driven synchronous rectification is not an option with this topology. This brings attention to control-driven synchronous rectification.

By observing each of the four switching states in Figure 1, the following truth table and corresponding logic circuit can be established, defining the relationship between the PWM control signals and the synchronous rectifiers.

STATE	PRIMARY PWM INPUTS				TRANS INPUTS		SR INPUTS	
	GATE A	GATE B	GATE C	GATE D	OUT 1	OUT 2	GATE 1	GATE2
$t0 \rightarrow t1$	1	0	0	1	0	1	0	1
$t1 \rightarrow t2$	1	0	1	0	1	1	1	1
$t2 \rightarrow t3$	0	1	1	0	1	0	1	0
$t3 \rightarrow t4$	0	1	0	1	1	1	1	1

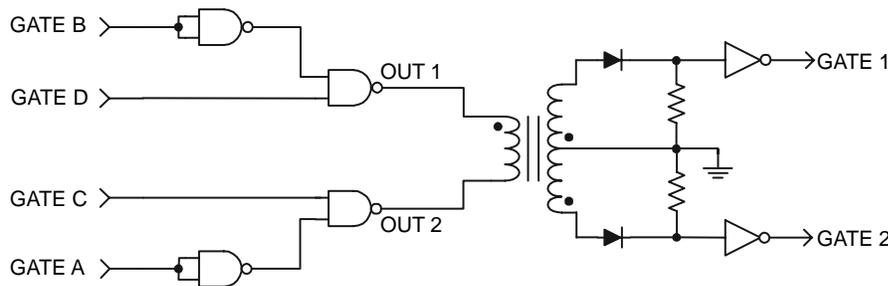


Figure 2. Synchronous Rectifier Truth Table and Drive Logic

The circuit in Figure 2 is an example of primary side PWM control where the NAND gates handle all of the PWM demodulation before passing the synchronous rectifier drive signals through a signal transformer, and onto a secondary side referenced driver circuit. The problem with this approach is the excess amount of signal delay taken on by the additional logic gates. Because the turn-off of the appropriate synchronous rectifier must precede the start of the next primary side switching command, some delay is acceptable. However, too much delay can result in either of the synchronous rectifiers staying on during the start of the next switching state where the corresponding command would otherwise be to turn-off the switch.

Realizing the problems associated with externally developing the synchronous rectifier drive signals, some newer controllers include this logic internally. While this may seem like a convenient feature, a compromise is realized by the additional requirement of two device pins and silicon area, along with higher PWM cost.

3 An Easier Method

There is a simple way to drive the synchronous rectifiers of a phase shifted full bridge without incurring any of these problems. Referring back to Figure 1, notice that the current flowing in the secondary during the $t_1 \rightarrow t_2$ state is almost identical to the secondary current flow shown in the $t_0 \rightarrow t_1$ state. If Q1 were not turned on during the $t_1 \rightarrow t_2$ state, then the corresponding gate drive signal GATE 1 would be identical to GATE B.

Similarly, the current flowing in the secondary during the $t_3 \rightarrow t_4$ state is almost identical to the secondary current flow shown in the $t_2 \rightarrow t_3$ state. If Q2 were not turned on during the $t_3 \rightarrow t_4$ state, then the corresponding gate drive signal GATE 2 would be identical to GATE A. The timing diagram in Figure 3 highlights the implications of using the primary referenced PWM signals, GATE A and GATE B to directly drive the synchronous rectifiers.

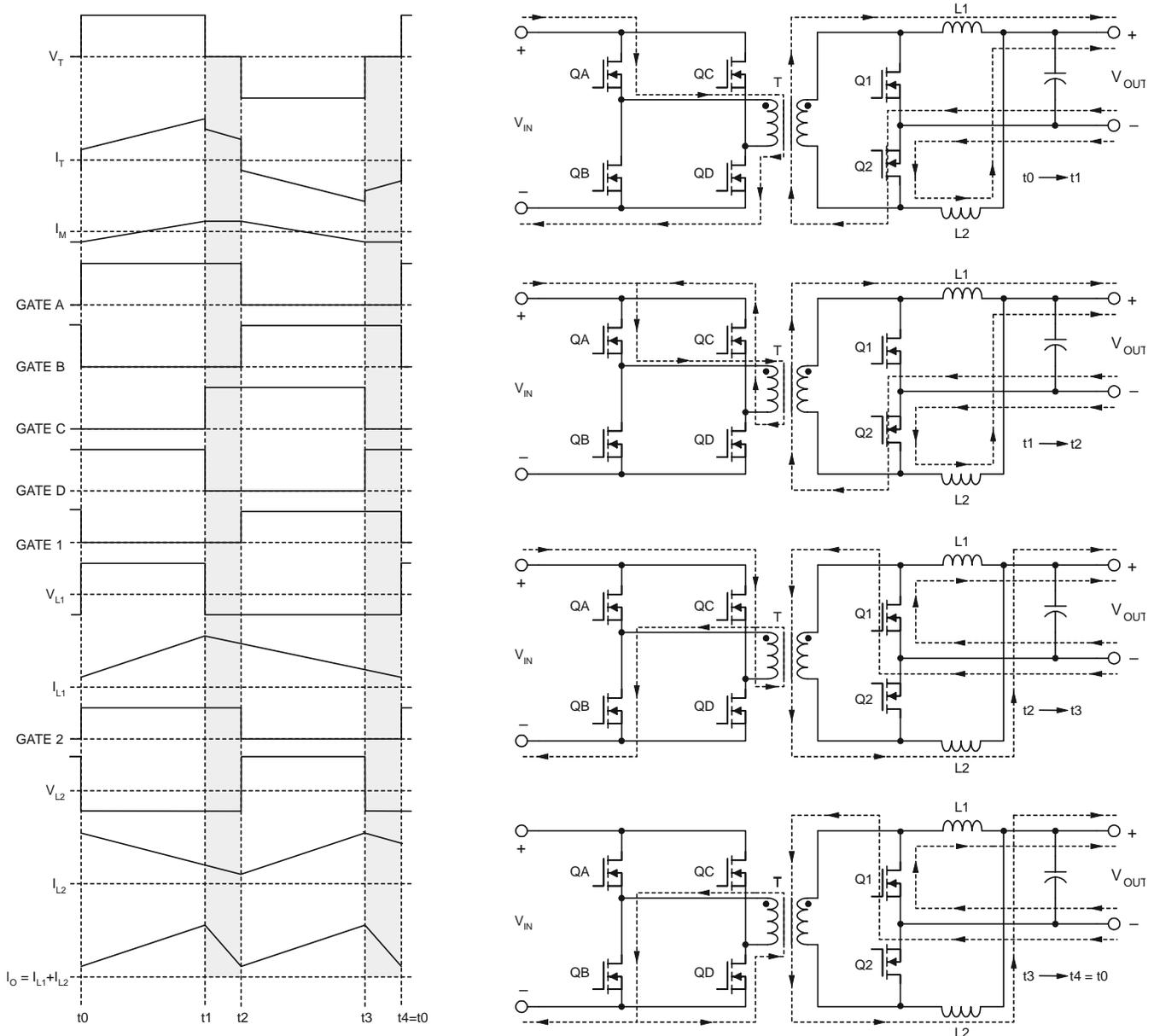


Figure 3. Phase Shifted Full Bridge With AB Driven Synchronous Rectifiers

Comparing the timing diagram of Figure 3 to that of Figure 1, the only difference occurs during the freewheel period, highlighted in Figure 3. During the freewheel period in Figure 1, both output rectifiers are conducting. Conversely, during the same period in Figure 3, only one of the synchronous rectifiers is conducting. Because the current flowing during the freewheel state remains in the same rectifier as the previous state, the switching action, as far as the output load current is concerned, will remain unchanged as shown in Figures 1 and 3.

What about body diode conduction between the interval of Q2 turning off and Q1 turning on or vice versa? Typically there is a dead time associated between the turn off of one synchronous rectifier and the turn on of the alternate rectifier, as might be expected between the $t1 \rightarrow t2$ and $t3 \rightarrow t4$ intervals. During this dead time the circulating current would normally be forced to flow through the synchronous rectifier body diode. However, unique to the phase shifted full bridge topology is the freewheel period where the transformer primary is clamped. Clamping the transformer primary results in zero volts across the primary and consequently zero volts across the secondary. With zero voltage across the transformer and no change in the magnetizing current, body diode conduction in the synchronous rectifiers is virtually eliminated during this period.

Driving the synchronous rectifiers directly with the GATE A and GATE B PWM signals removes the logic circuitry previously shown in Figure 2. The propagation delays mentioned are also eliminated. Using this technique, the synchronous rectifier truth table and corresponding gate drive circuit are now reduced to that of Figure 4.

STATE	PRIMARY PWM INPUTS				SR INPUTS	
	GATE A	GATE B	GATE C	GATE D	GATE 1	GATE 2
$t0 \rightarrow t1$	1	0	0	1	0	1
$t1 \rightarrow t2$	1	0	1	0	0	1
$t2 \rightarrow t3$	0	1	1	0	1	0
$t3 \rightarrow t4$	0	1	0	1	1	0

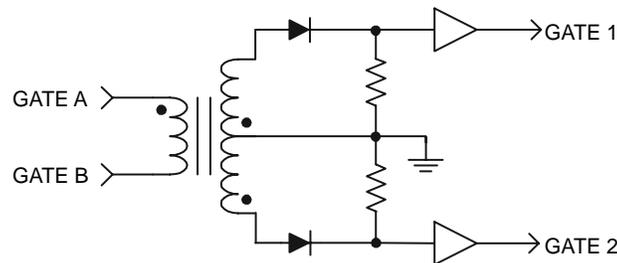


Figure 4. Simplified Synchronous Rectifier Drive Using AB PWM Signals

4 Application Diagram

A simplified application diagram, using the AB signals from a phase shifted full bridge PWM controller to drive the synchronous rectifiers of a current doubler output stage, is shown in Figure 5. By not including the logic circuitry shown in Figure 2, the UCC3895 is able to free up two additional device pins. The additional pins are utilized by offering more advanced features such as adaptive delay set (ADS), which is used to extend the converter's ZVS load range while maintaining the maximum possible duty cycle range. The UCC3895 also offers separate power and signal ground pins assuring reliable noise-free operation within the device.

Also shown are the UCC37324 MOSFET drivers. These dual 4-A drivers are recommended for high frequency designs where high speed, high peak current, and minimal rise and fall times are necessary. For additional hands-on information, Texas Instruments offers the UCC3895EVM-001 evaluation module.

The UCC3895EVM-001 uses the AB outputs of the UCC3895 for direct control driven synchronous rectification of a current doubler output stage, helping the user gain a better understanding of this novel switching technique.

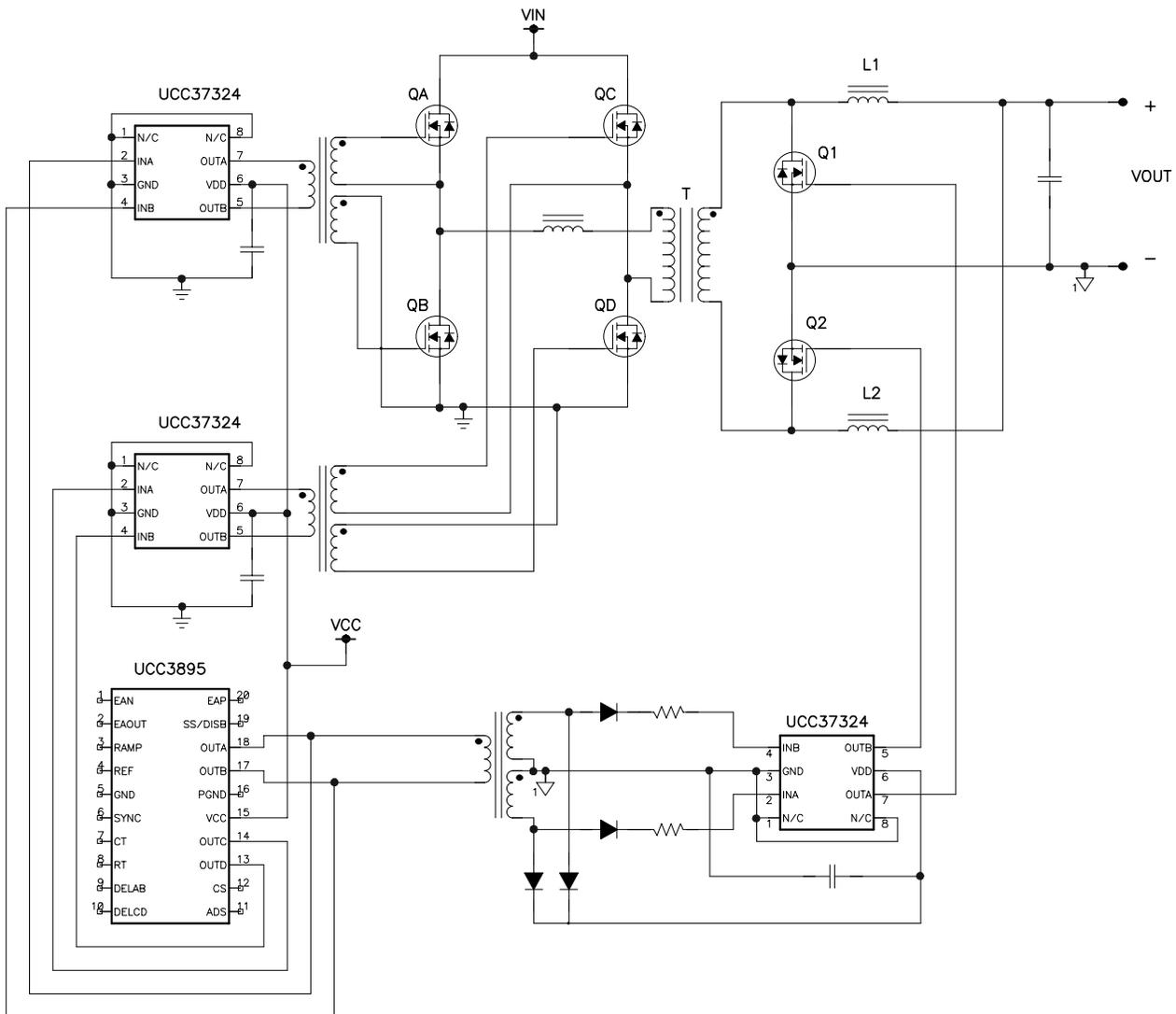


Figure 5. Simplified Application Diagram of Synchronous Rectifier Drive Using AB PWM Signals

5 Conclusion

Using the A and B outputs of any phase shift PWM controller, this approach has the added benefit of reducing components, minimizing propagation delays and greatly simplifying the design task of driving a current doubler output stage.

6 References

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