UCC3895 OUTC/OUTD Asymmetric Duty Cycle Operation

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ABSTRACT

A small number of current-mode applications using non–synchronous output stages have experienced asymmetric pulse widths on the OUTC and OUTD outputs of the UCC3895. Applications using synchronous rectification and/or voltage mode control typically do not experience this anomaly. For the cost of a single resistor, a simple fix allows reliable and stable operation of the UCC3895.

Contents

1 Problem Description

In certain applications, asymmetric duty cycle operation can be observed between the OUTC and OUTD outputs of the UCC3895. The asymmetry generally occurs when the UCC3895 is configured for current-mode operation at very light load or start-up conditions. When the output of the UCC3895 error amplifier is approximately 0.875 V, the PWM comparator output can vary in response to a shallow ramp signal sensed at the ramp pin. The current-sense signal plus any slope compensation are summed at the ramp pin of the UCC3895 and can become very shallow during minimum output load current.

Since there is very little slope definition during light-load operation, the ramp valley can hover near 0 V for a longer period. This results in approximately 0.8 V seen at the inverting input of the PWM comparator. Likewise, since the output of the error amplifier is fed directly to the non-inverting input of the PWM comparator, an error amplifier output of approximately 0.8 V places near equal voltages at both PWM comparator inputs, resulting in non-hysteretic output switching of the PWM comparator. This erratic switching behavior is then passed onto the drive logic for OUTC and OUTD and ultimately can manifest itself as asymmetrical output pulses between OUTC and OUTD. Additionally, since OUTA and OUTB are driven directly from the internal UCC3895 clock, this leg is not subject to asymmetric pulse errors resulting from a shallow ramp signal, as shown in Figure 1. When operating in this mode, typical output waveforms look similar to those shown in Figure 1.

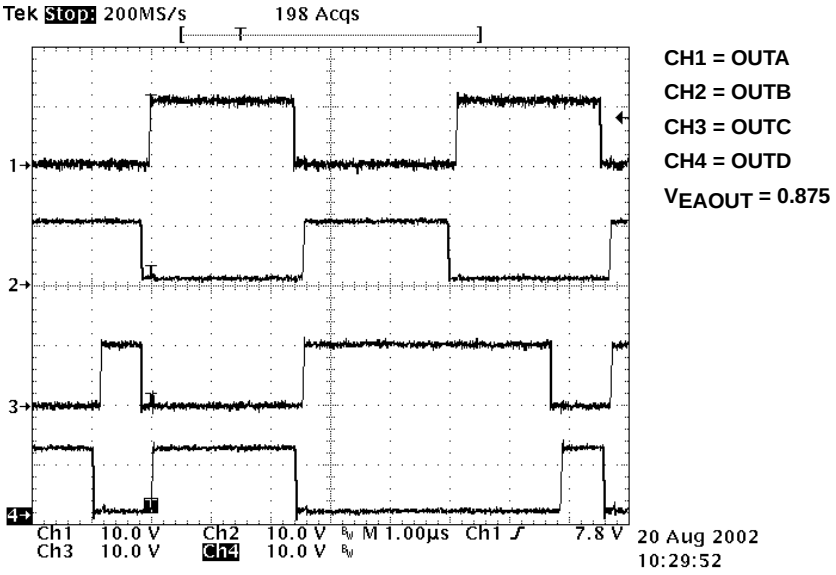

Figure 1. UCC3895 Output Waveforms

2 Solution

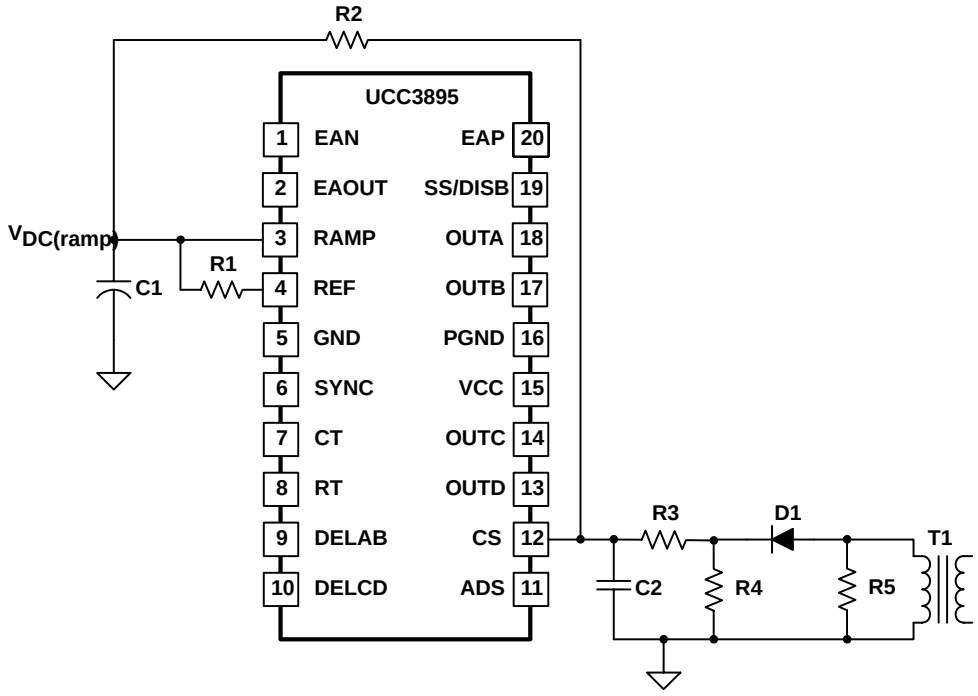

Figure 2. Peak Current Mode Control (slope compensation not shown)

T1 is a current sense transformer operating with D1 and R4 to produce a voltage representation of the current to be sensed. R3 and C2 form a leading edge filter network at pin 12 of the UCC3895. Most UCC3895 current mode applications, including the UCC3895EVM–001 available from Texas Instruments, include these components or similar circuitry.

The UCC3895 contains an internal pull-down MOSFET pulling the RAMP input (pin 3) down to GND. (See block diagram on page 7 of the UCC3895 data sheet, TI Literature No. SLUS157) The gate signal of this MOSFET is derived from the SYNC signal (pin 6) of the UCC3895. By adding a dc offset voltage, $V_{DC(ramp)}$, to the ramp signal at pin 3, a dc voltage is consequently seen at the drain of the internal MOSFET. During the period of time where the ramp valley was shallow at approximately 0 V, there is now some dc voltage for the internal FET to pull down to ground. The action of pulling down the ramp combined with the charging and discharging of C1 produce a more defined ramp signal during start-up and also at minimum output load operation.

1 V of dc offset should be sufficient and can be added by choosing R1 according to equation (1).

$$R1 = \left(\frac{V_{REF}}{V_{DC(ramp)}} - 1 \right) \times (R2 + R3 + R4) \quad (1)$$

This equation is valid for using a current sense transformer configured as shown in Figure 2. For variations on the type of current sensing circuit used, equation (1) would have to be modified accordingly.

3 Test Results

For the circuit shown in Figure 2, a 2.2-kΩ resistor was added for R1 with C1 equal to 100 pF. As shown in Figure 3, the ramp signal is disturbed during the asymmetric pulse operation of OUTC and OUTD. With the addition of R1, Figure 4 shows the ramp signal with approximately 1 V of dc offset added. The ramp signal is shown being pulled down by the UCC3895 internal MOSFET with each synchronous pulse, and then charging back up through C1. Though not clearly visible, the original ramp signal still exists atop the dc offset voltage. OUTC and OUTD are also shown in stable operation and very small duty cycles of approximately 5% are attainable.

CH1 = OUTC
CH2 = OUTD
CH3 = RAMP
V_{EAOUT} = 0.875 V

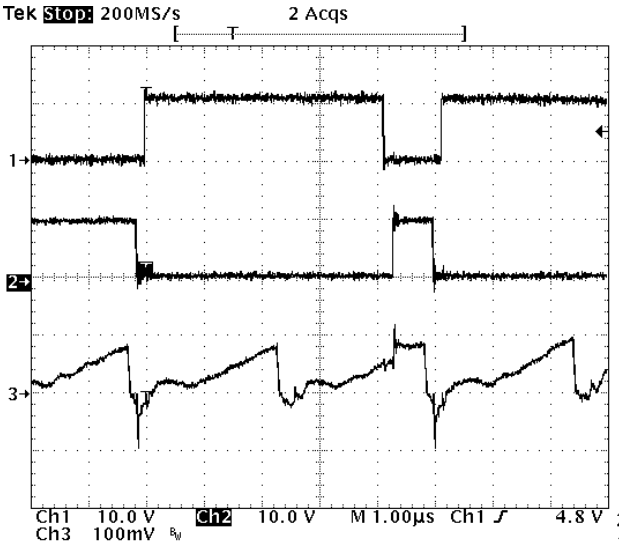

Figure 3. No DC Offset Added to Ramp

CH1 = OUTC
CH2 = OUTD
CH3 = RAMP
CH4 = SYNC

R1 = 2.2 kΩ
R2 = 510 Ω
R3 = 0 Ω
R4 = 20 Ω
V_{EAOUT} = 0.875 V

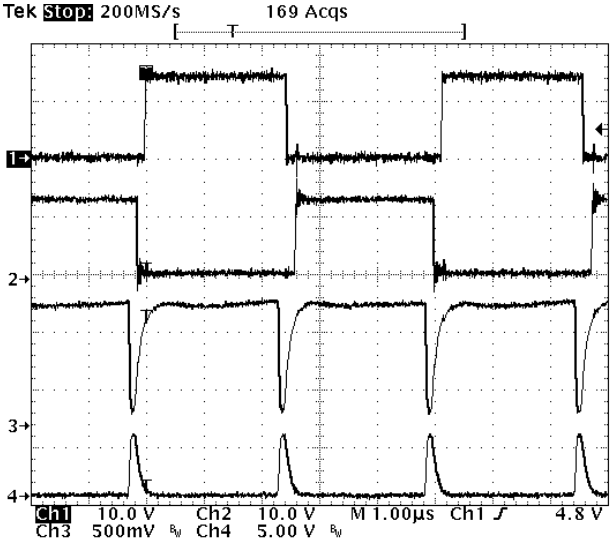

Figure 4. 1-V DC Offset Added to Ramp

4 Summary

The UCC3895 configured in voltage mode does not experience OUTC and OUTD asymmetric output pulses. Also, when using synchronous rectifiers in current mode operation this problem does not typically exist due to the additional reflected secondary current added to the primary side current sense. A small number of current mode applications running at very small duty cycles have experienced asymmetric OUTC and OUTD output pulses. However, for the cost of one resistor, a simple fix allows reliable and stable operation of the UCC3895.

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