



ABSTRACT

The DEM-FDA-SOIC-EVM is an unpopulated evaluation module (EVM) for fully differential amplifiers (FDA) in the D (SOIC) package. This EVM is designed in accordance with high-speed performance specifications and Texas Instruments' FDAs with output common mode (Vocm) control and power down (PD) functionality. The EVM is designed to enable quick and efficient lab testing of TI High Speed FDAs using 50-Ω SMA connectors for use with lab equipment. All the necessary connectors to perform lab measurements, including power and signal connections, are considered for this schematic. The EVM is configured for single-ended input and single-ended output when populated according to the schematic; the EVM can accommodate fully differential behavior with proper configuration. The output transformer enables single-ended output for easy interfacing with test equipment, and there are external SMA connectors for output common mode and power down control. Additional options on the amplifier input traces prior to termination resistors and extensions of transformer pads after the amplifier outputs allow for optional AC coupling.

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1 Features

- Split or single supply operation
- Configurable gain and feedback network with optional compensation capacitors
- Supports single-ended or differential inputs
- Designed for easy connection to standard 50- Ω input and output impedance lab equipment
- Inputs, outputs, and control signals all include SMA connectors for high speed operation

2 EVM Specifications

Section 2.1 through Section 2.4 provides a general description of the DEM-FDA-SOIC-EVM specifications and configurations.

2.1 Power Supply Connections

While operating as split supply, apply positive supply voltage to VCC+, negative supply to VCC-, and ground reference from supply to GND. The board can also be configured for single supply operation by connecting the positive supply voltage to VCC+ and ground to GND and VCC-.

2.2 Input and Output Connections

The DEM-FDA-SOIC-EVM is equipped with SMA input and output connectors for simple interface to signal generators and analysis equipment. To obtain the best results, it is recommended to use 50- Ω characteristic impedance cables between the EVM and lab equipment.

The example schematic in Figure 3-1 shows the EVM configured for a single-ended input with a differential output that is also converted to a single-ended signal through the transformer (T1). This example configuration makes it easy to interface the board with single ended input and output test equipment. In this example case, the input impedance is balanced to accept a connection from a 50- Ω characteristic connection. The resistor R14 is set to 26.1- Ω to provide a balanced impedance that would match the parallel combination formed by the test equipment 50- Ω impedance and resistor R4.

The board can also be configured for differential inputs and differential outputs. Differential inputs can be applied by populating both input SMA connectors (J3 and J5). When using differential inputs, it is important to balance the impedances created by resistors R4 and R14 so that each input is balanced to the same impedance. Otherwise an impedance imbalance will cause output errors. For differential outputs, a shorting resistor should be placed between terminals 1 and 6 and also between terminals 3 and 4 of the transformer (T1) footprint. Both output SMAs should be populated and resistors R8 and R13 removed. It may be necessary to adjust the output loading network formed by R7, R9, and R11 if a differential output impedance match other than 50- Ω is required.

Additional features of the board include optional AC coupling at the inputs and outputs of the amplifier circuit. The input side traces include series 0603 resistor pads prior to the input termination resistors, denoted as R16 and R17, to provide optional AC coupling. The pads of transformer T1 have been extended inward to enable AC coupling at the output of the device. If the board is to be used with DC coupling, the transformer pad extensions can be left unconnected and R16 and R17 should be populated with 0- Ω resistors.

2.3 Output Common Mode Control (Vocm)

FDAs have a feature to externally drive output common mode (Vocm). This feature can be utilized by populating equivalent value resistors for R1 and R2 to VCC+ and VCC-. This sets the output common mode to mid-supply, a common configuration. Additionally, the option to drive Vocm with the SMA connector exists. For this use case, do not populate R1 or R2. If there is need to terminate the Vocm signal source into 50- Ω , C3 can be replaced by a 50- Ω resistor.

2.4 Power Down Function

Many TI op-amps have a shutdown or power down (PD) feature; this allows for the amplifier to appear as a high impedance load and enables low current draw. This feature is often active low and can be left *floating* or be driven to a value. In the case of the THS4130 shown in the schematic, driving the PD pin to VCC- will place the amplifier in *power down*. For convenience and ease of use, the EVM contains a header and jumper to control PD functionality without externally driving the PD pin. If an external signal is needed to drive PD, removing the jumper will enable input through the SMA connector. For specific amplifier power-down polarity, please refer to the respective device data sheet.

3 Example Schematic and Layout Using THS4130

Figure 3-1 shows the DEM-FDA-SOIC-EVM schematic in an example configuration using the THS4130 fully differential amplifier. Figure 4-1 through Figure 4-4 show the PCB layer prints for the top traces, ground plane, power plane, and bottom traces respectively.

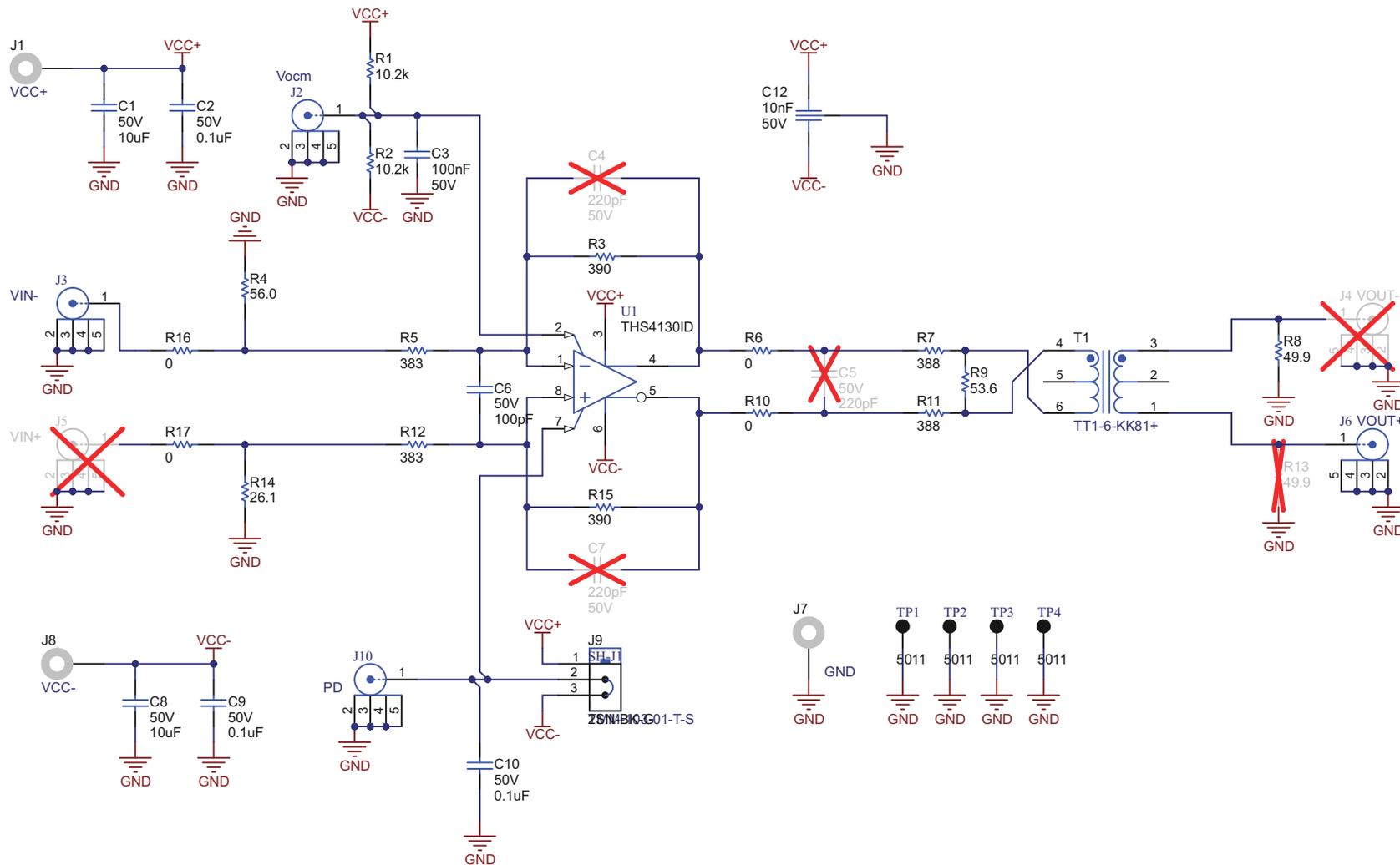


Figure 3-1. Schematic with Example Configuration Using the THS4130

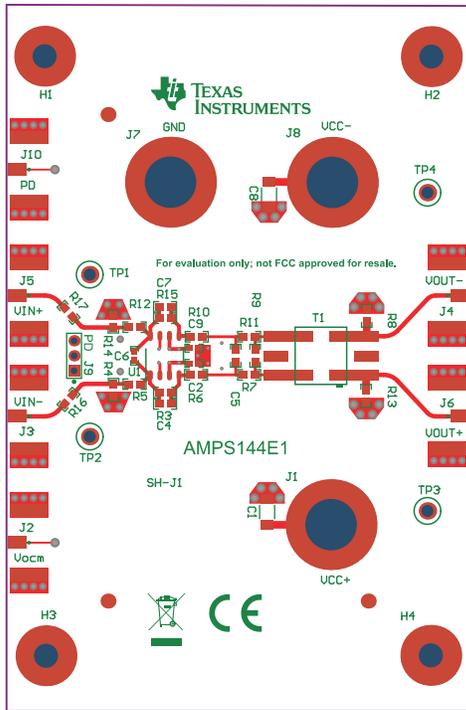


Figure 4-1. PCB Top Layers

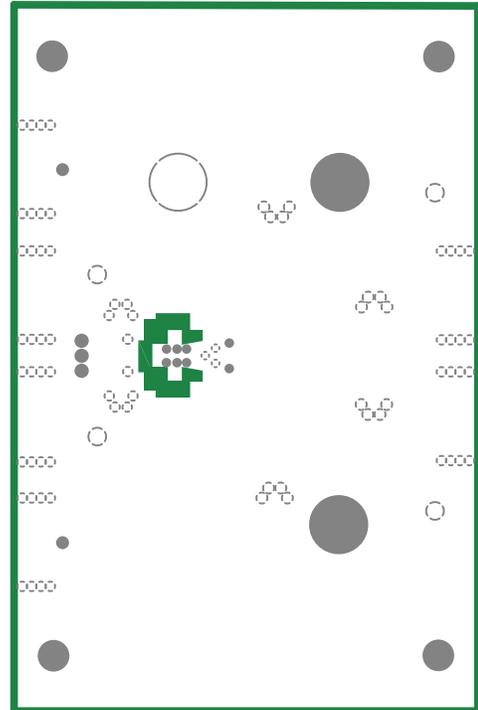


Figure 4-2. PCB Second Layer (Ground)

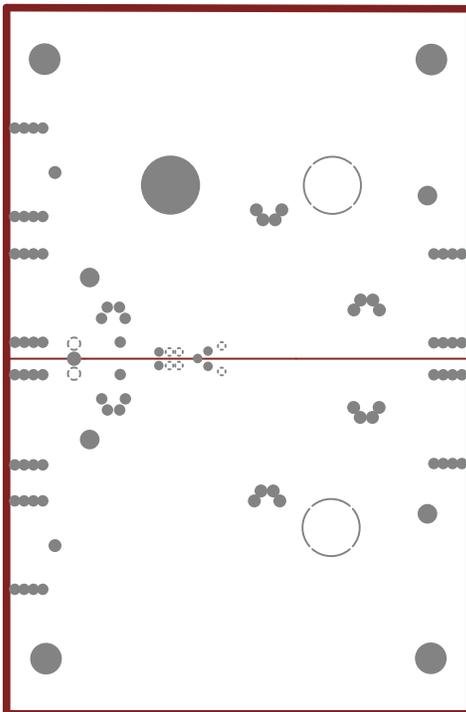


Figure 4-3. PCB Third Layer (Power)

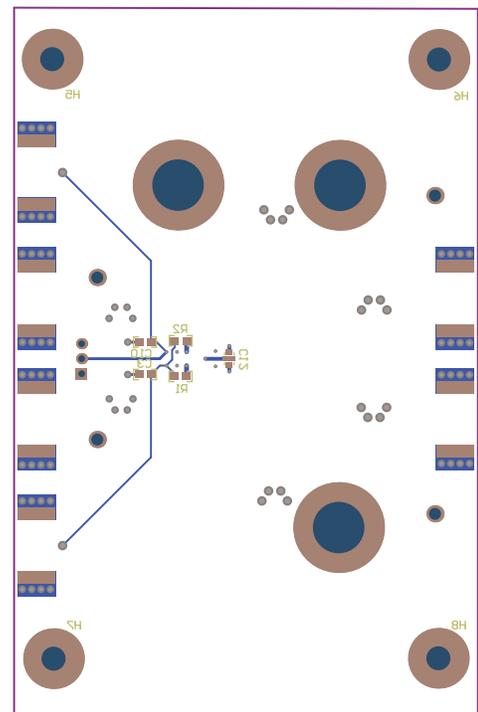


Figure 4-4. PCB Bottom Layers

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