

# Designing Bipolar High Voltage SEPIC Supply for Ultrasound Smart Probe



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## ABSTRACT

Medical imaging, specifically ultrasound, is undergoing a significant transformation. A smart probe ultrasound scanner is a handheld device that visualizes internal organs of the human body and their size using advanced technology. The high degree of integration in front-and back-end units within a handheld device brings the designers face-to-face with challenges like power dissipation, thermal performance, size constraints and noise immunity. This application note provides a solution to efficiently power ultrasound transmitters. This design generates bipolar programmable high voltage (HV) up to  $\pm 80$  V from a very low voltage source. It can deliver continuous average power of 2-W on each rail. A Single-Ended Primary-inductor Converter (SEPIC) topology with uncoupled inductors is preferred over transformer based flyback converter in order to accomplish the critical height requirement ( $< 5$  mm). It features symmetric rails ( $< 1\%$ ) and load regulation of  $< 2\%$ . It can be synchronized to an external clock to help filter out beat frequencies. This application report also provides a solution to generate programmable output voltage of up to  $\pm 100$  V by the introduction of an intermediate boost stage.

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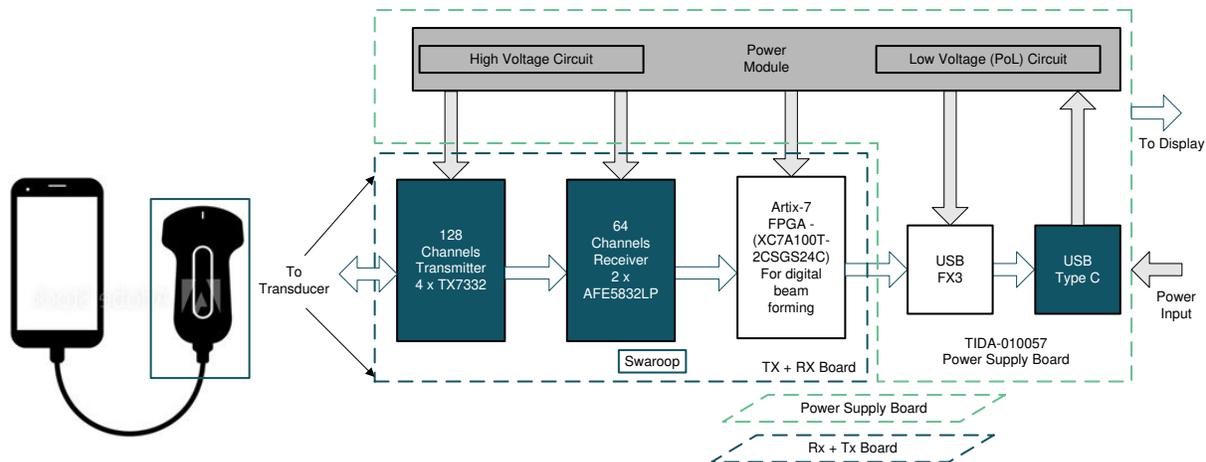
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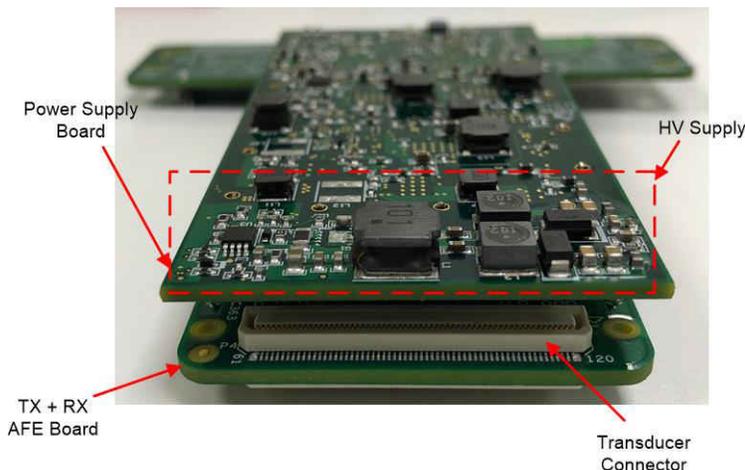
**1 Introduction**

Ultrasound imaging is widely used technique for diagnostic purpose. In addition to high-performance cart-based ultrasound systems, it is now possible to use a handheld device (smart probe) to accomplish high-quality ultrasound imaging. These smart probes leverage the power and resources of a mobile/tablet to process and display ultrasound images. A typical use case for these systems is to bring modern medical imaging technology to remote places, making the diagnostics faster. This small equipment is typically powered by battery (1S/2S), or from USB source. The data can be transferred over USB or Wi-Fi®.

Figure 1-1 (left) shows a generic picture of such smart probe ultrasound scanner depicting a probe connected to a mobile device. Figure 1-1 (right) shows the system level block diagram of the smart probe, which includes transmit (TX) and receive (RX) analog front end (AFEs) for transmitting and receiving ultrasonic pulses and a FPGA to perform beam-forming. The whole setup is powered through the power supply board, consisting of DC-DC converters to generate point of load voltages, HV circuit for TX and USB controller for data and power management. This whole assembly of the analog front-end and power supply module is shown in Figure 1-2, where the different sections are highlighted in red.



**Figure 1-1. (left) Generic Smart Probe; (right) System Block Diagram of Smart Probe Ultrasound Scanner**



**Figure 1-2. Power Supply and TX+RX AFE Boards**

This application report focuses on the generation of compact, transformer less high-voltage supply for powering an ultrasound transmitter. This design generates programmable bipolar supply up to  $\pm 80V$ , from a very low input voltage (typically 5 V) in a single stage. Key constraints of size and height are met by using transformer-less SEPIC architecture. High efficiency of SEPIC architecture ensures low thermal footprint. This design also achieves  $<2\%$  load regulation, fast transient response, and very low noise. The solution can be synchronized to an external clock in order to enable filtering of beat frequencies.

Table 1-1 below summarizes the design specifications of the high voltage circuit in the smart probe ultrasound scanner.

**Table 1-1. Design Specifications of High Voltage Power Supply in Smart Probe Ultrasound Scanner**

Characteristics	Specifications
Input voltage range	<ul style="list-style-type: none"> <li>Option-1: From USB power (4.25V to 5.5V DC)</li> <li>Option-2: From 1S/2S Li-Ion battery (3.6 V to 8.4 DC)</li> </ul>
Output voltage	Bipolar (from 10 V to 80 V @ 25 mA and -10 V to -80 V @ 25 mA), symmetrical loads
Peak Efficiency	75%
Switching frequency	250 kHz
Size (length x width)	15 mm x 45 mm (single layer)
Height	$< 5$ mm
Output voltage regulation	$<2\%$
Voltage symmetry with equal load on both rails	$<1\%$
Output ripple	0.1% of the output voltage
Synchronization to external clock frequency	Yes

## 1.1 Key Design Challenges

The quality of the final ultrasound image is directly dependent on the quality of the *power supply*, since the noise from the supply can distort the image. The key design challenges are as follows:

- Dual rail HV ( $\pm 80$  V @ 25 mA) generation from USB supply with single stage implementation and transformer-less approach to achieve height  $<5$  mm with HV Rail symmetry  $<1$  % and load regulation within 2%
- Efficient layout and placement to achieve high signal to noise ratio (SNR) with noise floor below -90dB and data integrity, by minimizing conducted and radiated emissions
- Overall system efficiency  $> 80\%$  and thermal performance (temperature rise  $<15^\circ$  C above ambient)

## 1.2 Potential Topologies for Generating High Voltage Supply

Considering the voltage requirements (up to 80 V, and 100 V in some cases), low power levels (approximately 2 W per rail) and small size of the solution, the most optimum power supply topologies are Boost/Cuk, Flyback and SEPIC. Since negative rail is required Flyback and SEPIC are better choices, due to ease of implementation. A brief description and comparison of both topologies is provided below.

**SEPIC:** SEPIC is a flexible topology that can function as step-up and step-down voltage regulator, it features minimal active components, a simple controller, and clamped switching waveforms to minimize switching noise

**Flyback:** Flyback converter is the most commonly used SMPS circuit for low output power applications where the output voltage must be isolated from the input main supply. The flyback topology is essentially the buck-boost topology that is isolated by using a transformer as the storage inductor.

In [Table 1-2](#), a comparison between Flyback and SEPIC converter is shown:

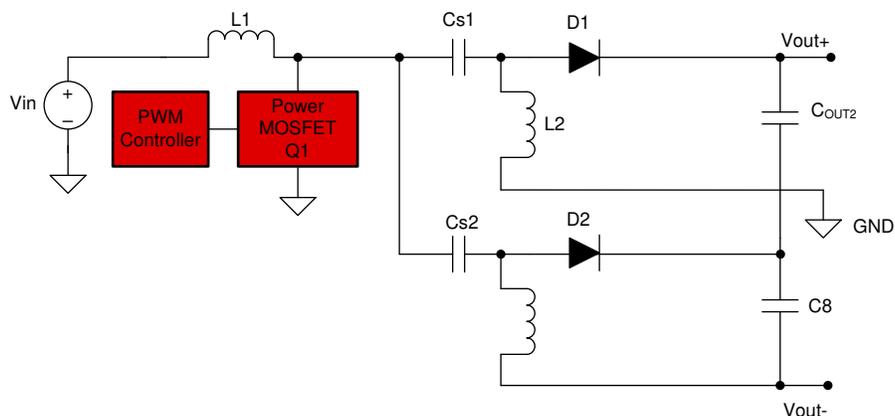
**Table 1-2. Pros and Cons of Flyback and SEPIC Topology**

	Pros	Cons
Flyback	<ul style="list-style-type: none"> <li>High step-up ratio</li> <li>Lower diode stress</li> <li>Lower magnetic components count</li> </ul>	<ul style="list-style-type: none"> <li>Low efficiency at light loads</li> <li>Custom transformer (height increases)</li> <li>Snubber required</li> <li>Higher surge current</li> <li>Higher FET stress</li> </ul>
SEPIC	<ul style="list-style-type: none"> <li>Off-the-shelf inductors (height decreases)</li> <li>High efficiency at light loads</li> <li>Reduced switching losses (no leakage inductance of transformer)</li> <li>Lower FET stress</li> </ul>	<ul style="list-style-type: none"> <li>Smaller step-up ratio</li> <li>Higher diode stress</li> <li>Higher magnetic components count</li> </ul>

Considering the challenges discussed in [Section 1.1](#), Flyback topology is also suitable to generate bipolar high voltage supply. Nevertheless, the height of the Flyback transformer cannot accomplish an upper limit in the order of 5 mm (unless costly custom planar transformer is used in the design). This is the reason for selecting the SEPIC topology with off-the-shelf uncoupled inductors in this design.

## 2 Design of high voltage circuit using SEPIC topology

[Figure 2-1](#) shows the generic schematic of the SEPIC topology. It uses three inductors:  $L_1$ ,  $L_2$  and  $L_3$ . The three inductors can be wound on the same core since the same voltages are applied to them throughout the switching cycle and using a coupled inductor takes up less space on the PCB. However, they have to be custom made and may not be small in height, hence this solution uses uncoupled inductors. The capacitor  $C_{S1}$  and  $C_{S2}$  isolate the input from the output and provides protection against a shorted load.

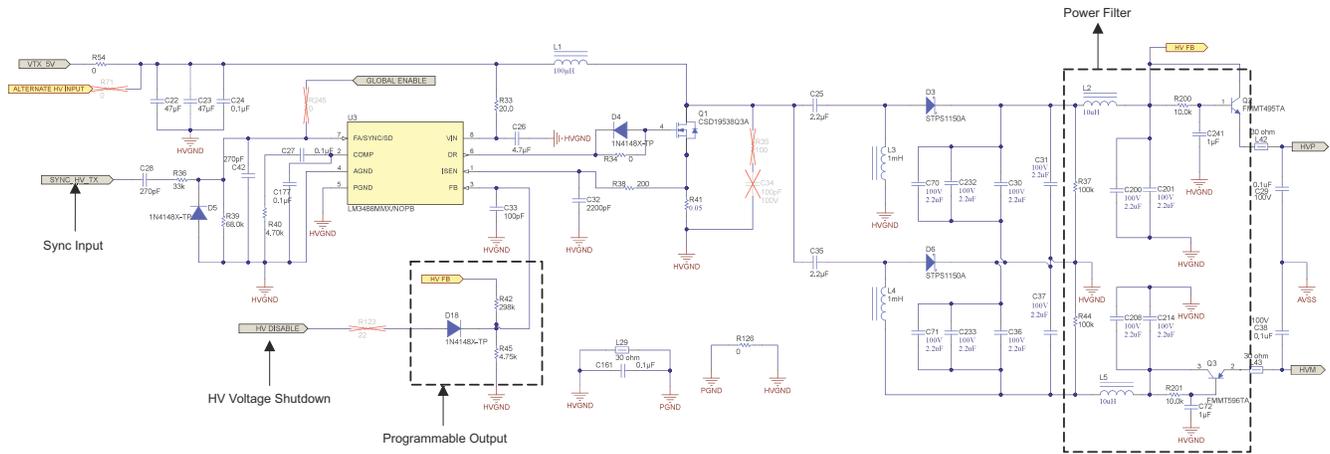


**Figure 2-1. SEPIC Topology Scheme**

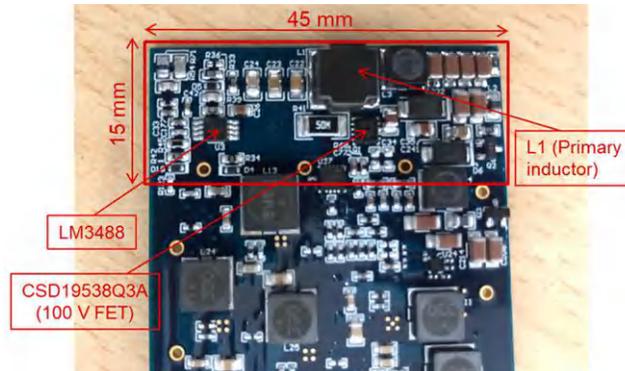
For detailed information on SEPIC, see the [Designing A SEPIC Converter](#) and the [LM3488/-Q1 Automotive High-Efficiency Controller for Boost, SEPIC and Fly-Back DC-DC Converters](#). These documents refer to a coupled inductor approach, however the current solution adopts uncoupled inductors.

### 2.1 TI HV Supply Architecture Using SEPIC Topology

This design implements a single stage architecture using only a single converter and a switch followed by two complementary output sections to generate the respective positive and negative HV rails. Custom made coupled inductors can benefit reduced energy losses due to leakage inductance, however, using uncoupled inductors helps meet the height requirements and better components choice [1]. The feedback is taken from positive output rail. [Figure 2-2](#) shows the complete schematic of the design and [Figure 2-3](#) shows the physical picture of the board highlighting the HV section.



**Figure 2-2. Schematic of the High Voltage Circuit Design for Smart Probe**



**Figure 2-3. Power Supply Board Highlighting the HV Section**

Table 2-1 explains the component selection, and equations for the SEPIC power converter using LM3488 device.

**Table 2-1. Design Equations and Selected Components**

Parameter	Equations	Selected Components
Duty cycle	$D = \frac{V_{OUT} + V_D}{V_{IN} + V_{OUT} + V_D} = 94.15\%$ <span style="float: right;">(1)</span>	LM3488, which can reach a Duty cycle of 100%.
L1 (for minimum 40% current ripple)	$L1 > \frac{V_{IN,MAX}^2 \times D}{R \times F_{SW} \times P_{OUT}} \rightarrow 70.1 \mu H$ <span style="float: right;">(2)</span> <p>where, R is %ripple of input of current (0.4)</p>	100 $\mu$ H (23% of current ripple), Isat = 1.2A, DCR = 0.377 $\Omega$
L2, L3 (for minimum 40% current ripple) -> L3,L4 in Figure 2-2	$L2 > \frac{(1-D) \times V_{OUT}^2}{R \times F_{SW} \times P_{OUT}} \rightarrow 1020.8 \mu H$ <span style="float: right;">(3)</span> <p>where, R is % ripple of input of current (0.4)</p>	1000 $\mu$ H (41 % of current ripple) Isat=80 mA, DCR=5.4 $\Omega$
MOSFET Q1 in Figure 2-2	$V_{SW(PEAK)} = V_{IN} + V_{OUT} + V_D = 86.28 = 86.28V$ $T_{OFF} < 210 \text{ ns @ } 250 \text{ kHz and } D = 94.14\%$ $V_{GS(TH)} < V_{IN}$	CSD19538Q3A VDS,MAX = 100 V; RDS, ON = 58 m $\Omega$ VGS,TH = 3.2V; T <sub>OFF</sub> = 9 ns
CS2, CS3 -> C25, C35 in Figure 2-2	$\Delta V_{CS} = \frac{I_{OUT} \times D_{MAX}}{C_S \times F_{SW}} = 0.042 \text{ V}$ <span style="float: right;">(4)</span>	2.2 $\mu$ F ; VDC=50V
D2, D3 -> D3, D6	VIN+VOUT=85V - Schottky diode to minimize losses	STPS1150 ; V <sub>FORWARD</sub> = 0.78 V ; VRRM=150 V
COUT2, COUT3 -> C70, C232, C30, C31, C71, C233, C36 in Figure 2-2	$ESR \leq \frac{V_{ripple} \times 0.5}{I_{L1(PEAK)} + I_{L2(PEAK)}} \leq 42 \text{ m}\Omega$ <span style="float: right;">(5)</span> $C_{OUT} \geq \frac{I_{OUT} \times D_{MAX}}{V_{ripple} \times 0.5 \times F_{SW}} \geq 2.355 \mu F$ <span style="float: right;">(6)</span> <p>Vripple= 1% *Vout</p>	4 x 2.2 $\mu$ F - VDC = 100 V
CIN -> C22, C23, C24 in Figure 2-2	$CIN(RMS) = \frac{\Delta I L1}{\sqrt{12}} = 0.18 \text{ A}$ <span style="float: right;">(7)</span>	2x 47 $\mu$ F - 0.1 $\mu$ F - VDC = 10 V
Compensation (RC, CC1 and CC2) R40, C27, C177 in Figure 2-2	$f_{RHPZ} = \frac{((1 - D_{MAX})^2 \times V_{OUT})}{(2 \times \pi \times D_{MAX} \times L2 \times 0.5 \times I_{OUT})} = 1.31 \text{ kHz}$ $f_R = \frac{1}{(2 \times \pi \times \sqrt{L2 \times CS})} = 3.35 \text{ kHz}$ <span style="float: right;">(8)</span> $f_c = \frac{f_R}{6} = 219 \text{ Hz}$ <span style="float: right;">(9)</span> $RC = \frac{(2 \times \pi \times f_c \times C_{out} \times V_{out}^2 \times (1 + D_{MAX}))}{(GCS \times GMA \times V_{REF} \times V_{INMIN} \times D_{MAX})} = 1.9 \text{ k}\Omega$ <p>Where, GCS = <math>\frac{1}{R_{SN}}</math>, where R<sub>SN</sub> = 20 A / V, and GMA = 800 <math>\mu</math>mho</p> <span style="float: right;">(10)</span> $CC1 = \frac{4}{(2 \times \pi \times f_c \times R_c)} = 1.5 \mu F$ <span style="float: right;">(11)</span> $CC2 = \frac{(C_{out} \times ESR)}{RC} = 47.4 \text{ pF}$ <span style="float: right;">(12)</span>	Rc = 4.70 k $\Omega$ - Cc1 = 0.1 $\mu$ F - Cc2 = 0.1 $\mu$ F

The output of the SEPIC circuit is cascaded with a  $\pi$  filter followed by an emitter follower configuration (power filter) in order to minimize the AC ripple. The filter is built in order to provide an attenuation of 24.44 dB (see Equation 13) of the AC ripple as shown in Figure 3-3 through Figure 3-6 in Section 3.2.

$$\text{Gain} = \frac{1}{\sqrt{1 + \left(\frac{f}{f_0}\right)^2}} \tag{13}$$

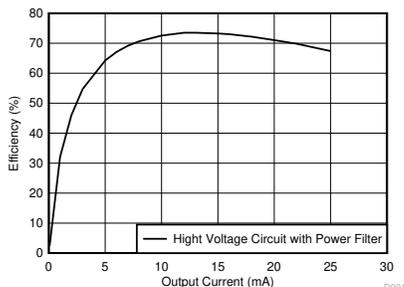
where  $f_0$  is the cut-off frequency of the RC filter and  $f$  is switching frequency of the input.

### 3 Test Results

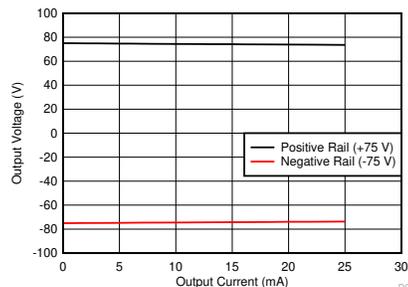
The circuit shown in Figure 2-2 is characterized for performance with 5V input supply and test results are presented in the subsequent sub-sections.

#### 3.1 Efficiency and Load Regulation

Figure 3-1 and Figure 3-2 shows the efficiency and load regulation of the power supply with symmetrical loads on the positive and the negative rail. The load is varied from 0 to 25 mA on each rail. The peak efficiency observed is ~75 % and worst case load regulation is 1.99 %. The positive and negative outputs are symmetrical within 1% with respect to each other.



**Figure 3-1. Efficiency Curve of SEPIC HV Power Supply**



**Figure 3-2. Load Symmetry of SEPIC Showing Accuracy of Less Than 1% and Load Regulation Less Than 2%**

### 3.2 Output Ripple Measurement

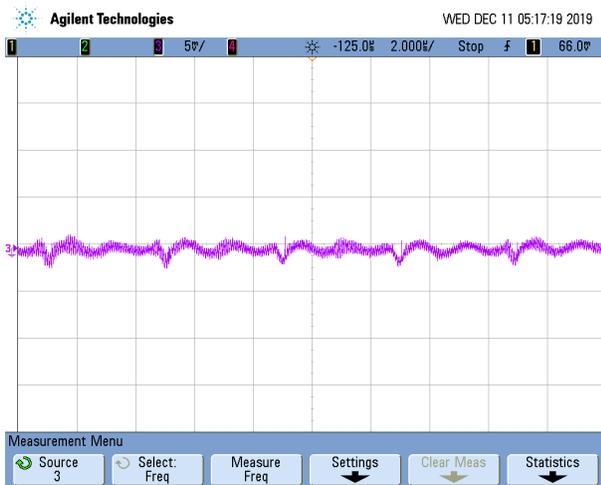
Figure 3-3 and Figure 3-5 shows the output ripple of the high voltage circuit of both negative and positive rail at full load, respectively. The ripple is measured at the output capacitor before the  $\pi$  filter, the peak to peak ripple is close to 25 mV. Figure 3-4 and Figure 3-6 shows the ripple measured after the Power Filter, which is significantly attenuated.



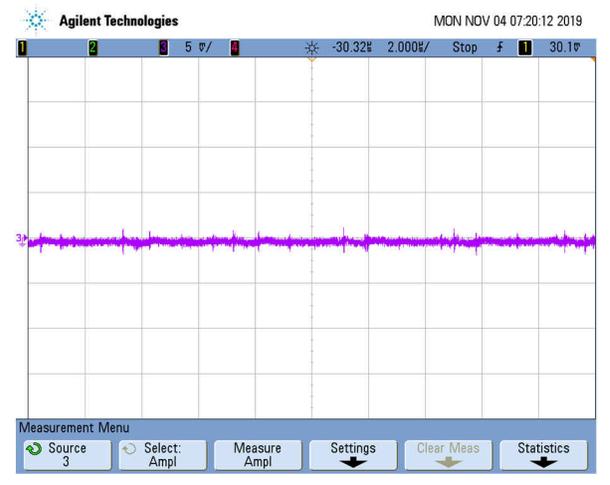
**Figure 3-3. Output Ripple of Negative Rail Before Power Filter**



**Figure 3-4. Output Ripple of Negative Rail After Power Filter**



**Figure 3-5. Output Ripple of Positive Rail Before Power Filter**



**Figure 3-6. Output Ripple of Positive Rail After Power Filter**

### 3.3 Load Transient Test

Figure 3-7 shows the load transient response of the power supply. The load of 25 mA per rail is applied onto both positive and negative rail with a duty cycle 20% at pulse repetition frequency of 5 kHz, as shown in purple waveform. A drop of less than 50 mV is observed on both the rails. Moreover, the load transient response test is repeated in case the load of the power supply is 1 A per rail with a duty cycle of 1%, at pulse repetition frequency of 5 kHz. The result in Figure 3-8, shows a drop of less than 1 V per rail.



Figure 3-7. Load Transient Response of Positive and Negative Output Rail With Symmetrical Loads (25 mA)

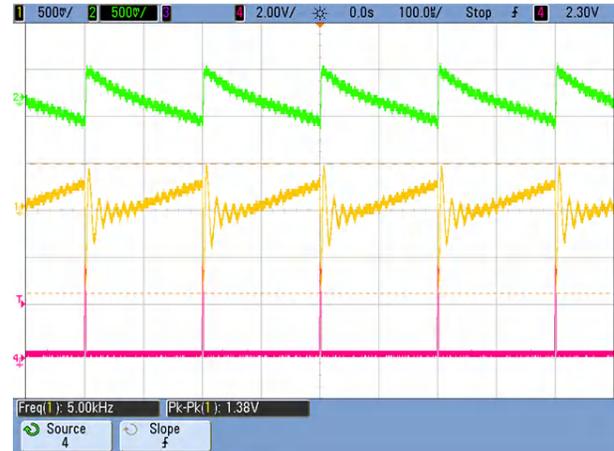


Figure 3-8. Load Transient Response of Positive and Negative Output Rail With Symmetrical Loads (1A)

### 3.4 Noise Measurement

Figure 3-9 and Figure 3-10 show the FFT of the received data collected from TX + RX setup consisting of TX7332 as transmit device and AFE5832LP as receive device. Figure 3-9 shows the noise with ideal bench supply and Figure 3-10 shows the noise with High Voltage supply generated by this design. The SNR in case of bench power supply and SEPIC based supply are 55.297 dB & 55.264 dB, respectively. This demonstrates that the noise performance of this design is comparable with the bench power supply.

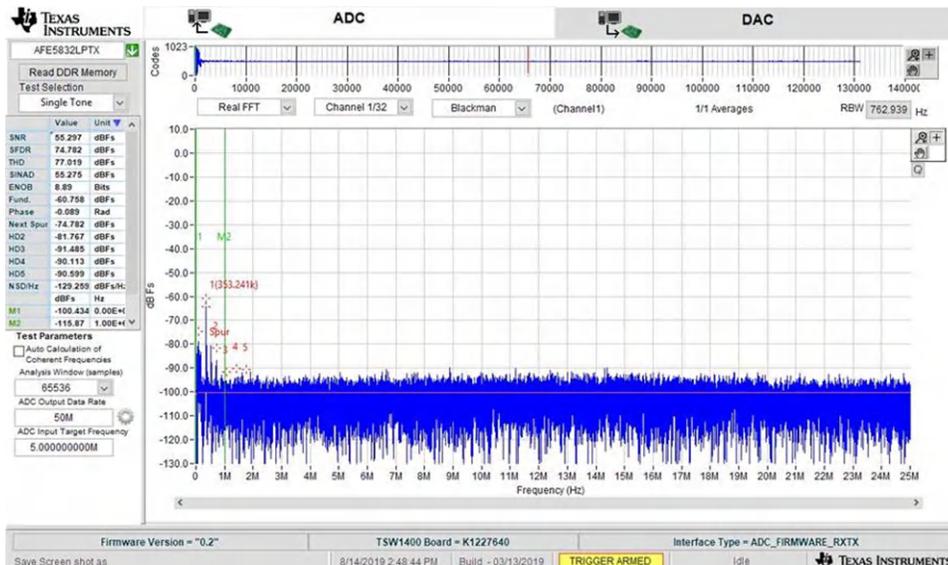


Figure 3-9. FFT of the Received Data Using Bench Power Supply, Showing SNR of 55.297 dB

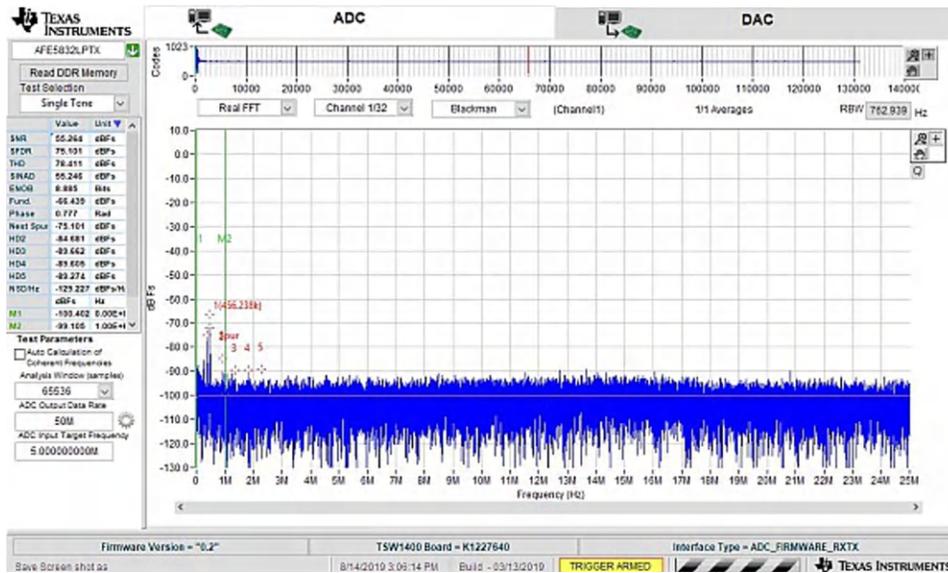


Figure 3-10. 11 FFT of the Received Data Using SEPIC Power Supply, Showing SNR of 55.264 dB

### 3.5 Thermal Performance

Figure 3-11 shows a thermal image of the high voltage circuit, with symmetrical load of 25 mA on each rail with 20 % duty cycle at 5 kHz shown in Figure 3-7. The maximum temperature is 34.7°C, reached after 30 minutes of powering on at ambient temperature of 20°C.

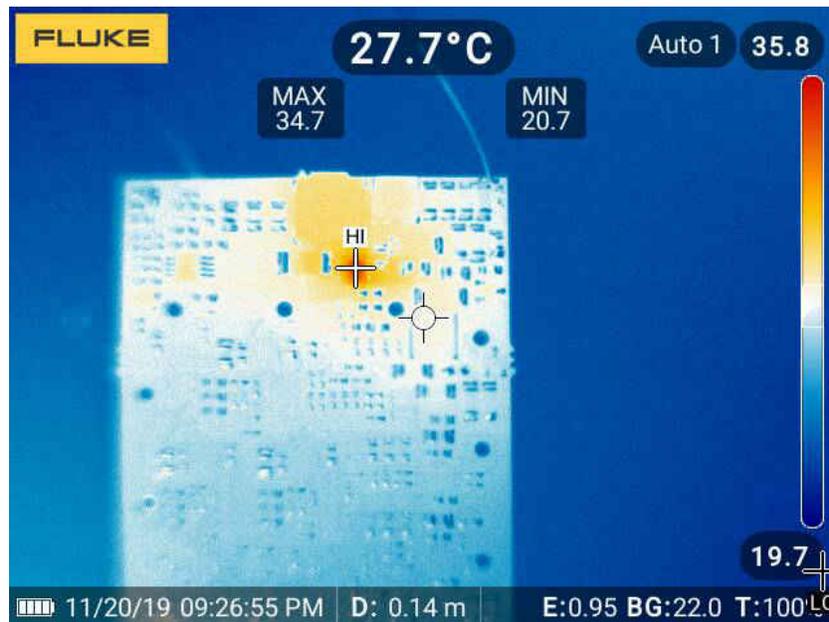


Figure 3-11. Thermal Performance of High Voltage Section

## 4 Possible Variants of the Design

This section shows possible variations of this design.

### 4.1 Option 1: Programmable Output Voltage

Based on the various ultrasound operating modes, the output of the high voltage circuit should be programmable. This can be implemented as shown in Figure 2-2 by replacing the diode D18 with one resistor R3, joining the feedback resistors (shown in Figure 4-1). Output voltage can be varied through the control voltage (VDAC). Resistors can be set using equations (2), (3), (4) where R1 and R2 are the feedback resistors.

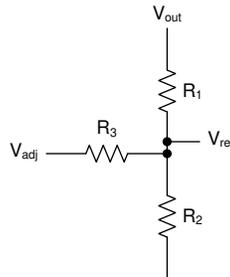


Figure 4-1. Implementation of Programmable Output

$$I_{R1,min} = \frac{V_{out,min} - V_{ref}}{R1} \quad (14)$$

$$R_3 = \frac{V_{adj,max} \times R_1}{V_{out,max} - V_{ref} - R_1 \times I_{R1,min}} \quad (15)$$

$$R_2 = \frac{V_{ref} \times R_1 \times R_3}{R_3 \times V_{out,max} - R_1 \times V_{ref} - R_3 \times V_{ref}} \quad (16)$$

Figure 4-2 shows linear relationship between the programmed output voltage and the control voltage.

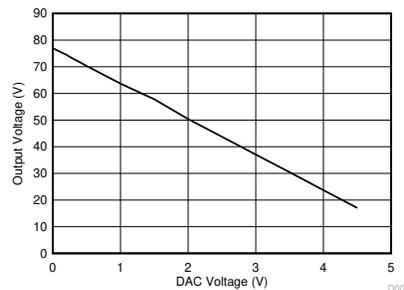
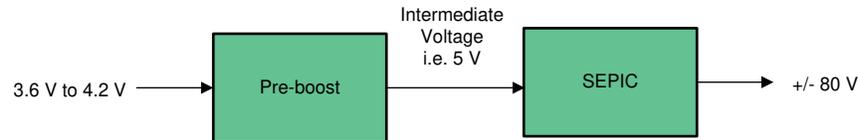


Figure 4-2. Linearity of Output Voltage vs Control Voltage (VDAC)

The designer should take care of the saturation current rating of the secondary inductors to take care of increased output current at reduced output voltage. In SEPIC converter the current is provided mainly from secondary inductors during off time. In this design, the secondary inductors are rated for 80 mA.

## 4.2 Option 2: Support Input From 1S Li-Ion Battery

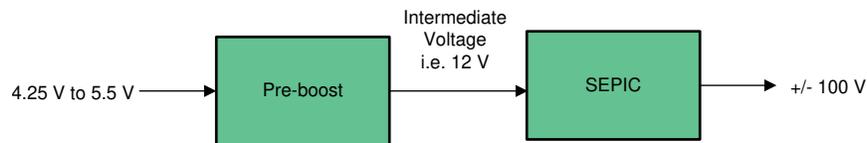
1S Li-Ion battery has a typical operating voltage range of 3.0 V to 4.2 V. To generate an output voltage of  $\pm 80$  V, the existing SEPIC needs a PWM controller that can achieve high duty cycle  $> 95\%$ . At these very high duty cycle there are practical limitations such as: parasitics which affect the turn-on and turn-off time of the MOSFET, lower available time for energy transfer from primary to secondary side which limit the achievable maximum output voltage. Hence an intermediate boost stage is required to be added, as shown in Figure 4-3.



**Figure 4-3. Case of 1S Battery**

## 4.3 Option 3: Output Voltage Up to $\pm 100$ V

In some cases ultrasound probes may require  $\pm 100$  V. The same limitations mentioned in option 2 are applicable. To achieve this, an intermediate boost stage is needed to boost the input to a minimum of 12 V to have a duty cycle of approximately 90%, as shown in Figure 4-4.



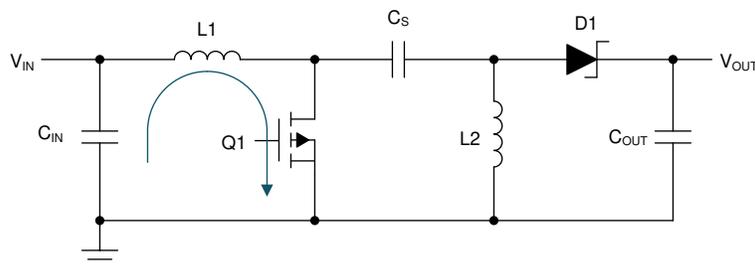
**Figure 4-4. Case of  $\pm 100$  V**

### Note

the components ratings should be taken care in both these cases. For instance, the MOSFET in second case has to withstand about 113 V, and the coupling capacitor has to be rated for 20 V.

## 5 Layout Guidelines

Layout in SEPIC is very critical. While designing, the most important rule is to reduce the noise in the high current switching loop, which is shown in Figure 5-1. The current flows from the input supply to the primary inductor and through the MOSFET. To minimize induced EMF due to switching currents, it is desirable to keep parasitic inductance of this loop as low as possible. Components (primary inductors, input electrolytic capacitors, and FET) must be placed as close as possible to each other. In this layout, a single ground plane was used, and all the signals return onto this low impedance plane, as shown in Figure 5-2. In case the HV circuit is placed in proximity to the transducer, shielding might be necessary to minimize effects of radiated interference from HV section.



**Figure 5-1. Hot Loop in SEPIC Configuration**

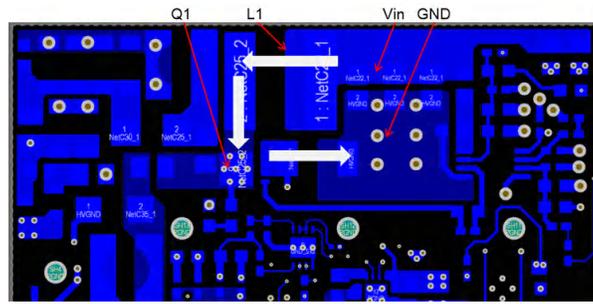


Figure 5-2. Layout Section of HV

## 6 Clock Synchronization

The schematic shown in Figure 2-2 can be synchronized to an external clock signal only if the duty cycle of the latter is larger than the duty cycle of the controller itself (larger than 93%). This design can be synchronized to an external clock with 50% Duty cycle by implementing the solution shown in Figure 6-1. Two diodes forming an OR-ing system are introduced. One diode is placed from the gate drive pin to the sync pin. The other one comes from the input clock signal. The resistor R36 and R39 are series SYNC resistor and discharge resistor, respectively. If DR\_pin is more positive than SYNC\_HV\_TX, then D1 will be reverse-biased and the SYNC-PIN will be driven high from D2. If DR\_pin is less positive than SYNC\_HV\_TX, then D2 will be reverse-biased and SYNC\_PIN will be driven High from D1. Test results are shown in Figure 6-2 and Figure 6-3.

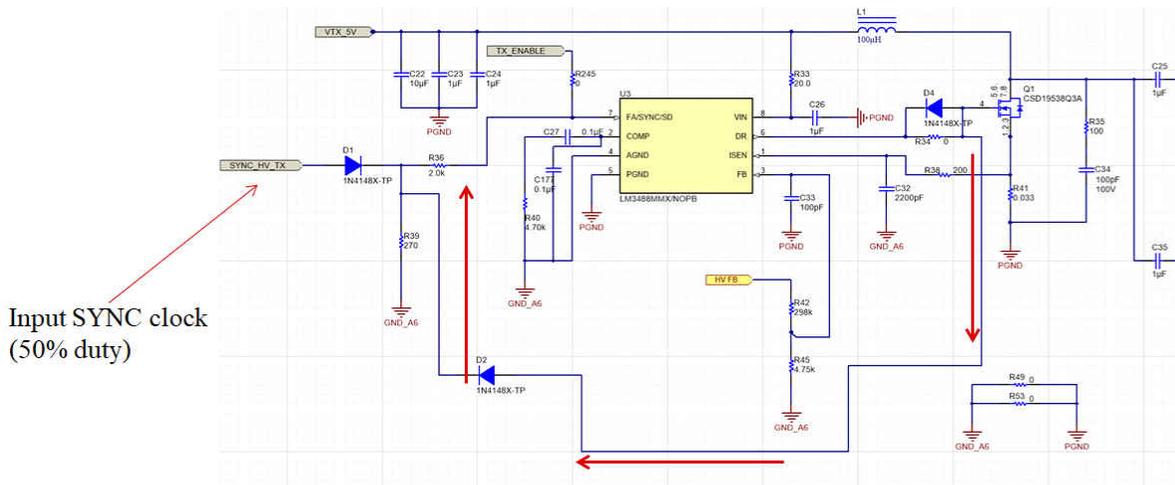


Figure 6-1. Section of the Schematic of HV Supply Updated After Implementation of SYNC Functionality



Figure 6-2. Synchronization at No Load With 50% Duty Cycle Clock

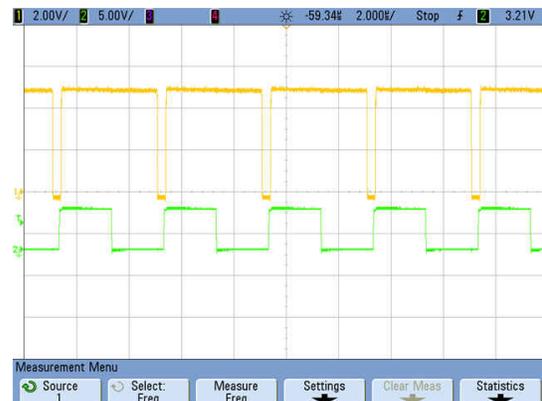


Figure 6-3. Synchronization at Full Load With 50% Duty Cycle Clock

## 7 Summary

The rapid evolution of ultrasound smart probes is changing the medical landscape and is helping provide better healthcare in remote places. The advent of these handheld devices is coming with the big challenges of compact size, high noise immunity, efficiency and thermal performance. This design, by the selection of SEPIC topology over the traditional transformer-based flyback topology, helps in solving some key- challenges for generating high voltage from low input voltage, in the desired size and height, while maintaining a high efficiency, low noise, good load regulation and symmetry. Based on the voltage requirement of the ultrasound transducer and operating modes, the output of high voltage circuit supports programmability.

## 8 References

1. Texas Instruments: [Benefits of a coupled-inductor SEPIC converter](#)
2. Texas Instruments: [LM3488/-Q1 Automotive High-Efficiency Controller for Boost, SEPIC and Fly-Back DC-DC Converters Data Sheet](#)
3. Texas Instruments: [Designing A SEPIC Converter](#)

## 9 Revision History

<b>Changes from Revision * (January 2020) to Revision A (May 2023)</b>	<b>Page</b>
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	<b>1</b>

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