TRF796x Software Design Hints

1 Software Design Hints

Table 1 shows which items apply to each device.

Table 1. Device Application

Item		TRF7960	TRF7961
#1	ISO15693 only - Direct command (0x14) 'Transmit next slot'	✓	✓
#2	Missing IRQ	✓	✓
#3	Lost IRQ	✓	✓
#4	Wrong data due to "overshoots"	✓	
#5	ISO14443A decoder	✓	
#6	Tags that do not follow the 14443A-level 4 framing	✓	
#7	SPI specialties / typical pitfalls	✓	✓

#1   *ISO15693 only - Direct command (0x14) 'Transmit next slot'*

Description   Sending of 'Transmit next slot' direct command (0x14) can happen only once (ISO 15693).

Hint   Before sending the 'Transmit next slot' direct command, the 'Reset' direct command must be sent.

Used only in ISO 15693 'Inventory' command (with 16 time slots). ISO 15693 'Write Single Block' command and 'Lock Block' command are affected also if the 'Option' bit is set.

#2   *Missing IRQ*

Description   The device does not send (by pin 13) any interrupt requests on certain conditions. The chip can enter a state in which the sending of additional interrupts during receive (RX) or transmit (TX) is stopped. This happens when the Stop Condition is exactly aligned with the byte boundary on the TX data.

Hint   The loading and reading of the FIFO should be coded so that the Stop Condition does not fall directly on the TX byte boundary.

#3   *Lost IRQ*

Description   Lost IRQ if the end of RX IRQ arrives at the same time that the IRQ register is being read (also see #6).

Hint   Add additional checks to retrieve the RX data if the IRQ is suppressed by a coinciding read operation.

#4	***Wrong data due to "overshoots"***

Description The 14443A 106-kbps decoder gives wrong data in certain condition. When the analogue front-end filter overshoots, the digitizer might produce a rising edge on the subcarrier data. If this occurs within a small time window, the decoder produces false data. This happens extremely rarely and is dependent on the antenna and filter characteristics.

Hint Switch to PM channel or adjust gain to avoid overshoots in the analogue filter.

#5	***ISO14443A decoder***

Description ISO14443A subcarrier decoder makes a wrong decoding – "reading holes".

Hint Repeating the reading using different gain setting of PM cannel results in correct data read; this might require additional time.

#6	***Tags that do not follow the 14443A-level 4 framing***

Description When a transmit frame starts with the code 0x93, 0x95, or 0x97, the reply is not correctly framed. This happens because the TRF796x devices have an automatic ANTICOLLISION broken byte framer that is activated with the 0x93, 0x95, or 0x97 code.

Hint Use TRF7960 "Direct Mode".

#7	***Errata TRF796x – SPI specialties / typical pitfalls***

For further information concerning the SPI, see *Using the SPI interface with the TRF7960* (SLOA140).

#7a	***SPI with SS pin only – no high impedance***

Description Serial interface with SS pin only. The interface does not go to high impedance when SS is high. It is not possible to multiplex the serial port interface lines.

Hint An external three-state buffer must be used if the chip is connected to a serial bus and the interface lines need to be multiplexed.

#7b	***SPI with SS pin only – direct commands***

Description Serial interface with SS pin only. The direct commands are not executed if they are the last operation in the SPI communication.

In the SPI interface with SS pin, the Stop condition clock pulse is missing (compared to the parallel interface and SPI without SS pin). Some operations rely on this clock, and they do not work as expected.

Hint If a direct command is the last operation in the SPI communication (the SS pins goes high after) an additional clock pulse must be sent.

#7c   SPI with SS pin only – IRQ status bit

Description   Serial interface with SS pin only. IRQ status bits are not cleared after the 'IRQ status' register (0x0C) is read.

Hint   A dummy read must be made after reading the 'IRQ status' register. This can be done in noncontinuous or continuous mode. In continuous mode, 8 clock pulses are needed. In noncontinuous mode, 16 clock pulses are needed (8 pulses for address and 8 pulses for data).

#7d   SPI with SS pin only – no TX if single bit in FIFO

Description   Serial interface with SS pin only. The chip does not start with transmission if only 1 byte is loaded to the FIFO.

Hint   The microcontroller must load an additional byte to the FIFO. The chip transmits only 1 byte on the TX if the "Number of complete bytes" in the registers 0x1D and 0x1E is 1.

#7e   SPI with SS pin only – clock polarity change

Description   Data CLK clock polarity must be switched when FIFO read operation (single or continues) is executed. During SPI data transmission, the MOSI line is valid on the rising edge, and the MISO line is valid on the falling edge of the Data CLK signal.

Hint   Firmware must switch clock polarity between FIFO writes and reads.

#7f   SPI with SS pin only – IRQ status register rst

Description   The IRQ Status register (0x0C) is not automatically cleared after reading.

Hint   A dummy register read is required to clear the content of the IRS status register and drive the IRQ line to low.

#7g   SPI with SS pin only – Single byte Direct commands

Description   All single byte direct commands need an additional CLK cycle to work.

Hint   All direct command functions must have an additional Data CLK cycle before SS goes high.

#7h   SPI with SS pin only – some registers do not take default values

Description   Some of the registers do not take the default values when the appropriate protocol is chosen in the ISO Control register.

Hint   Manually program the default settings into the TRF796x during initialization.

2 TRF796x – Known Issues With Specific Tags

Table 2. Known Issues

Issue Number	Tag Type	Problem	Hint
T1	MIFARE™ Ultralight	The 4-bit ACK and NAK reply can not be decoded with the integrated decoder/framer system. The 4-bit ACK is not according the standard ISO 14443A, so the internal data framing reports an error and needs to be by-passed.	Direct mode
T2	MIFARE Classic (standard)	The parity check fails with the encrypted frames as the MIFARE standard encrypts also the parity bit.	Direct mode
T3	Tags that do not follow the 14443A-level 4 framing	When a transmit frame starts with the code 0x93, 0x95, or 0x97, the reply is not correctly framed. This happens because the TRF796x devices have an automatic ANTICOLLISION broken byte framer that is activated with the 0x93, 0x95, or 0x97 code.	Direct mode
T4	Cryptography cards like JCOP, DESFire™	Using a cryptography card (for example, JCOP or DESFire) at close proximity (<1 cm) can cause a wrong collision error detection.	The reason is the 'calculation noise' emitted by the card which can be suppressed if the gain is drastically reduced. We proposed to use addition gain reduction enabled by test register.
T5	ISO 15693 cards requiring a slot delimiter (EOF)	There are ISO15693 cards on the market that require a slot delimiter (EOF).	A dedicated MCU timer needs to be used to generate the 37.76-µs timing grid.

IMPORTANT NOTICE