User's Guide

ISO1644DWEVM Reinforced Isolated I²C With GPIOs Evaluation Module

ABSTRACT

This user's guide describes the evaluation module (EVM) for TI's ISO1642, ISO1643, and ISO1644 isolated I²C transceivers with general purpose input/output (GPIO) channels. This EVM helps designers evaluate performance of these isolated devices in their 16-pinDW packages for quick development and analysis of data transmission systems.

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Trademarks

1 Introduction

This user's guide presents a typical laboratory setup used with this EVM.

CAUTION

This Evaluation Module (EVM) is made available for isolator parameter performance evaluation only and is not intended for isolation voltage testing. Do not use this EVM for isolation voltage tests even though the I^2C devices have galvanic isolation protection. To prevent damage to the EVM, any voltage applied as a supply or digital input/output must be maintained within the 0 V to 5.5 V recommended operating range.

Exceeding the specified input voltage range and applying loads outside the specified output range may cause unexpected operation and irreversible damage to the EVM. If there is uncertainty as to the input voltage range or load specification, please contact a TI field representative or create a post on e2e.ti.com prior to connecting power.

2 Overview

The ISO164x family of devices are low-power, bidirectional isolators that are compatible with I^2C interfaces and GPIO signals. The logic input and output buffers on these devices are separated by TI's *Capacitive Isolation* technology utilizing a silicon dioxide (SiO2) barrier. Devices with a *B* suffix are 3-kV_{RMS} basic isolated transceivers while devices without a *B* suffix are 5-kV_{RMS} reinforced isolated devices. When used with isolated power supplies, these devices block high voltages, isolate different grounds, and prevent noise currents from entering isolated grounds and interfering with or damaging sensitive circuitry.

ISO1642, ISO1643, and ISO1644 devices have two bidirectional data channels for I^2C clock and data lines and are fit for multi-master or clock-stretching applications. These devices achieve isolated bidirectional communication by introducing a static voltage offset (SVO), making the side 1 low-level output greater than the side 1 low-level input, thus preventing an internal logic latch that otherwise would occur with standard digital isolators.

Use this EVM to evaluate different signal and electrical parameters of the ISO1642, ISO1643, and ISO1644 devices. Apply test signals and sequences to the device channels to evaluate performance characteristics such as propagation delay, rise and fall times, and power consumption for different device conditions. Users can evaluate these parameters in their own lab environment.

This EVM can support evaluation of ISO1642, ISO1643, and ISO1644 devices in their 16-pinDW packages by de-soldering the included IC and soldering on a replacement component. If this is done by the user, please note that although the SDA and SCL channels are in the same pin positions across these devices, the number of GPIO channels and their direction configuration is different for each, as shown in Section 3.

Note

Although the IC landing pattern on this EVM is the same as other isolator devices, other 16-pinDW devices may have different pin configurations than the ISO1642, ISO1643, or ISO1644. **Do not** install other 16-pinDW devices.

3 Pin Configurations of Isolated I²C Transceivers With GPIO

The pin configurations of ISO1642, ISO1643, and ISO1644 in DW packages are shown in Figure 3-1.

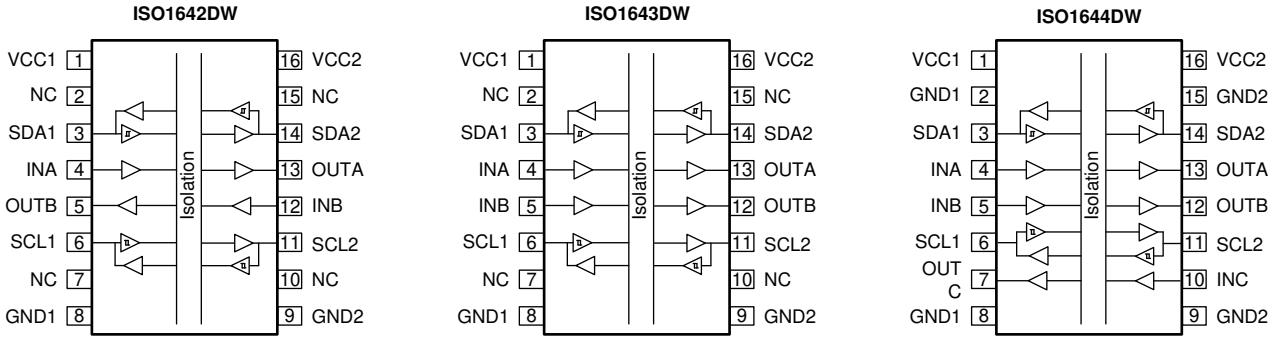

Figure 3-1. ISO1642, ISO1643, and ISO1644 Pinouts

The EVM PCB is shown in Figure 3-2 and comes with an ISO1644DW installed in place of U1. However, this EVM can also be configured for evaluation of ISO1642DW and ISO1643DW by replacing the included ISO1644DW device in place of U1.

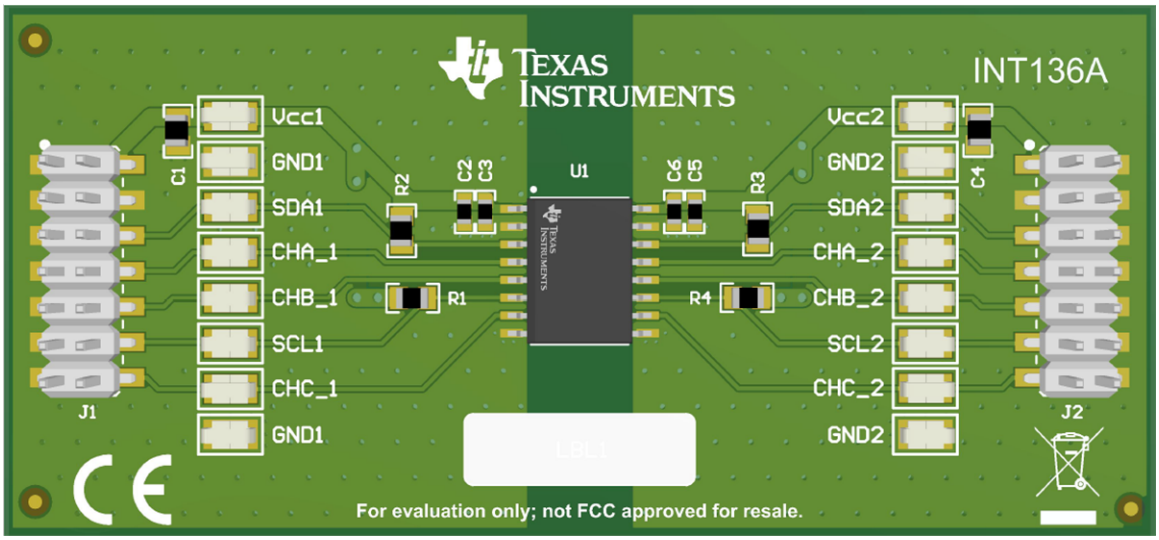

Figure 3-2. ISO1644DWEVM Top View

4 EVM Setup and Operation

CAUTION

Note that this EVM is for operating-parameter performance evaluation only and not designed for isolation voltage testing. Any voltage applied above the 5.5-V maximum recommended operating voltage of the isolators may damage the EVM.

This section describes the setup and operation of the EVM for parameter-performance evaluation. Figure 4-1 shows the basic setup of the EVM with two power supplies needed to evaluate isolator performance. Power this EVM by connecting voltages to VCC1 and VCC2 that are within the *Recommended Operating Range* in the ISO1642/ISO1643/ISO1644 device data sheet. Typical voltage levels for the VCC1 and VCC2 supplies are 3.3 V and 5 V. Separate power supplies can be used to provide each supply voltage, and they do not need to have the same value. If both sides are to be evaluated at the same supply voltage, only one power supply is required and can power both sides of the EVM.

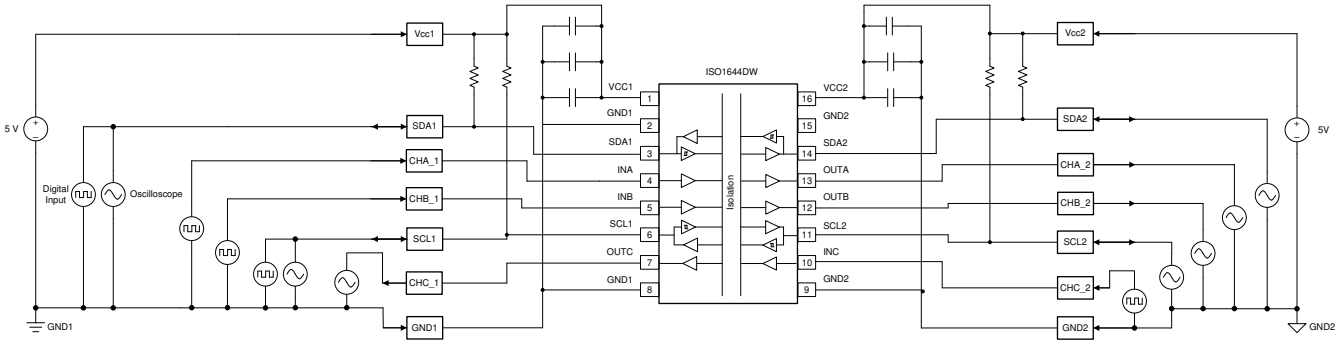

Figure 4-1. Basic ISO1644DWEVM Operation

Although the ISO1642, ISO1643, and ISO1644 devices feature bidirectional data channels, the devices perform optimally when side 1 (SDA1 and SCL1) is connected to a single controller or node of an I2C network while side 2 (SDA2 and SCL2) is connected to the I2C bus. Please note that bidirectional clocks can be used on these devices.

5 Bill of Materials

Table 5-1 lists the bill of materials (BOM) for ISO1644DWEVM.

Table 5-1. ISO1644DWEVM EVM Bill of Materials

Item	Qty.	Designator	Description	Manufacturer	Part Number
1	2	C1, C4	CAP, CERM, 10 uF, 35 V, ±10%, X5R, 0805	MuRata	GRM21BR6YA106KE43L
2	2	C3, C6	CAP, CERM, 0.1 uF, 25 V, ±5%, X7R, 0603	AVX	06033C104JAT2A
3	2	J1, J2	Header, 100mil, 7x2, SMT	Molex	15912140
4	4	R1, R2, R3, R4	RES, 3.3 k, 5%, 0.125 W, AEC-Q200 Grade 0, 0805	Vishay-Dale	CRCW08053K30JNEA
5	16	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16	Test Point, Miniature, SMT	Keystone	5019
6	4	H9, H10, H11, H12	Bumpon, Hemisphere, 0.44 X 0.20, Clear	3M	SJ-5303 (CLEAR)
7	1	U1	IC, Hot-swappable bidirectional I2C isolator with GPIO and enhanced EMC	Texas Instruments	ISO1644DWR

6 EVM Schematic and PCB

The ISO1644DW isolated I^{2}C EVM comes with an ISO1644DW installed in place of U1. This EVM can also be configured for use with an ISO1642DW or ISO1643DW. Each signal line (SDAx, SCLx) is configured with a 3.3-kΩ pullup resistor (R1 to R4) to the corresponding power supply (VCCx). These resistors may be replaced with 0805 resistors of other values per the application requirements. For insight on calculating appropriate pullup resistor values for I^{2}C buses, please refer to the *I2C Bus Pullup Resistor Calculation application report*.

Note

ISO164x devices are designed to sink different amounts of current on side 1 and side 2, be careful to choose resistors that keep I_{OL1} and I_{OL2} within the recommended operating range if replacing resistors R1 to R4.

Signal pins may be tied directly to ground using the header pins (J1 on side 1; J2 on side 2) to simulate a device pulling the I^{2}C line low. While not being actively driven low, the lines will be pulled up through the included pullup resistors. **Signal lines should not be tied directly to a supply voltage without a pullup resistor to limit input current**. These jumpers also provide input /output signal access, including for oscilloscope probes, to each pin.

Note

Ensure that SDAx and SCLx signal lines are not tied directly to VCCx. A current-limiting pullup resistor is required, and populated by default, to limit current in the cases where the device pins drive a low-voltage.

Figure 6-1 shows the schematic diagram for this EVM, and Figure 6-2 and Figure 6-3 show the printed circuit board (PCB) layout.

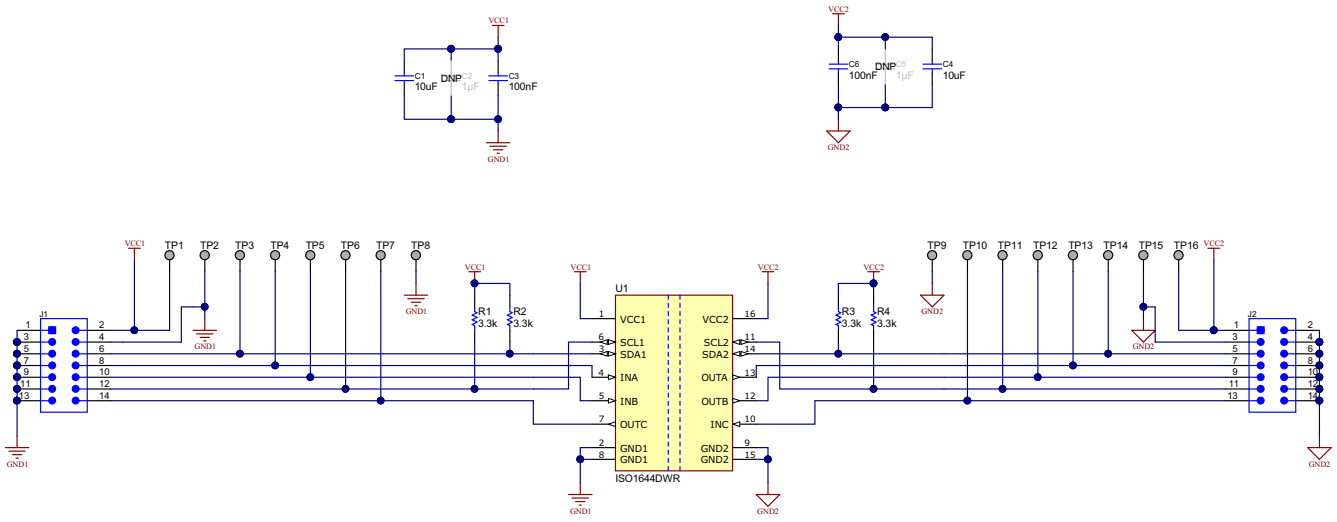

Figure 6-1. ISO1644DWEVM Schematic

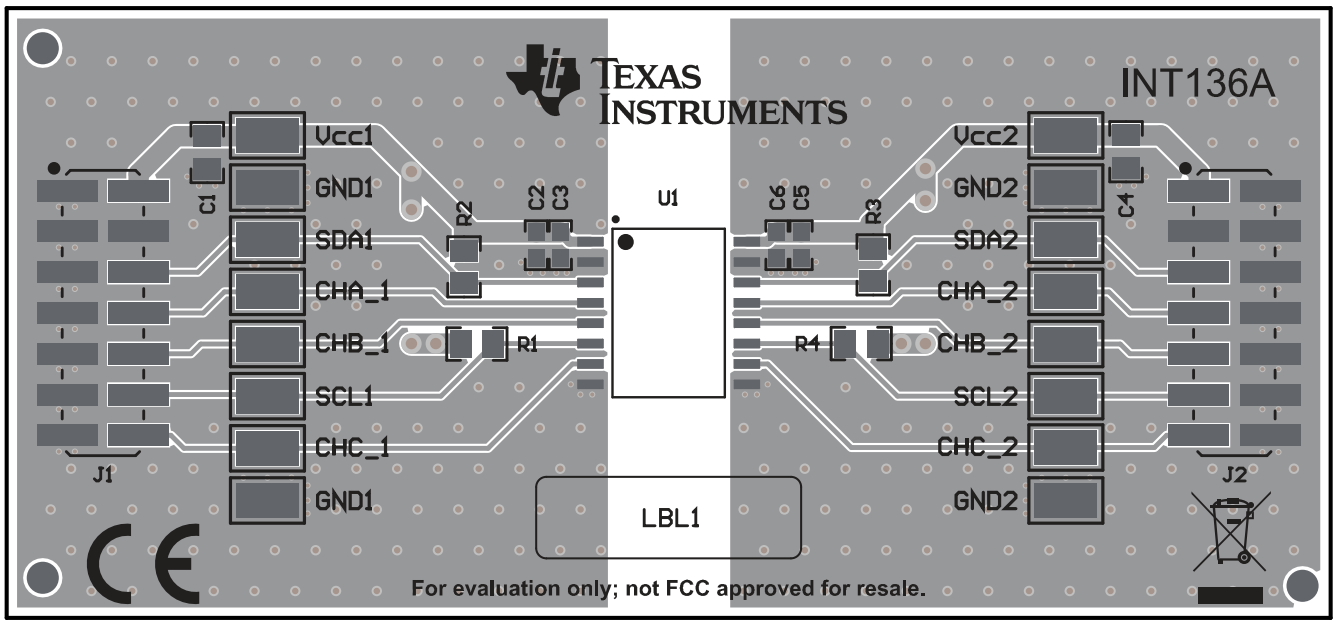

Figure 6-2. ISO1644DWEVM Top PCB Layout

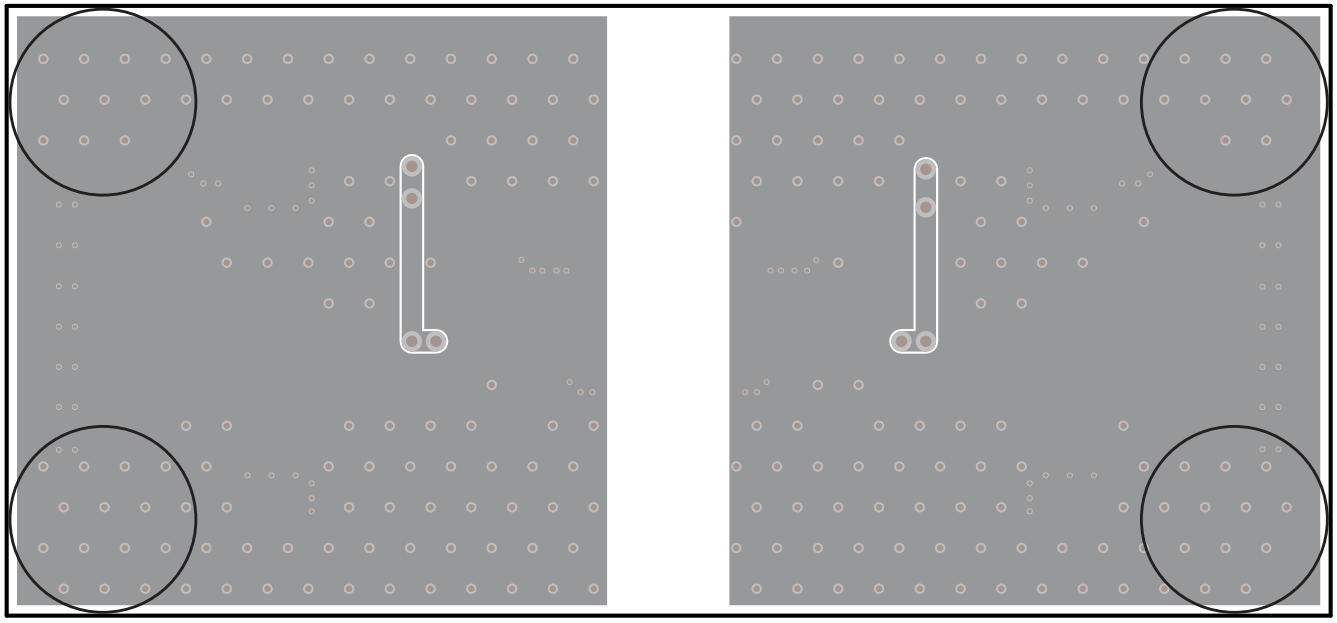

Figure 6-3. ISO1644DWEVM Bottom PCB Layout

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