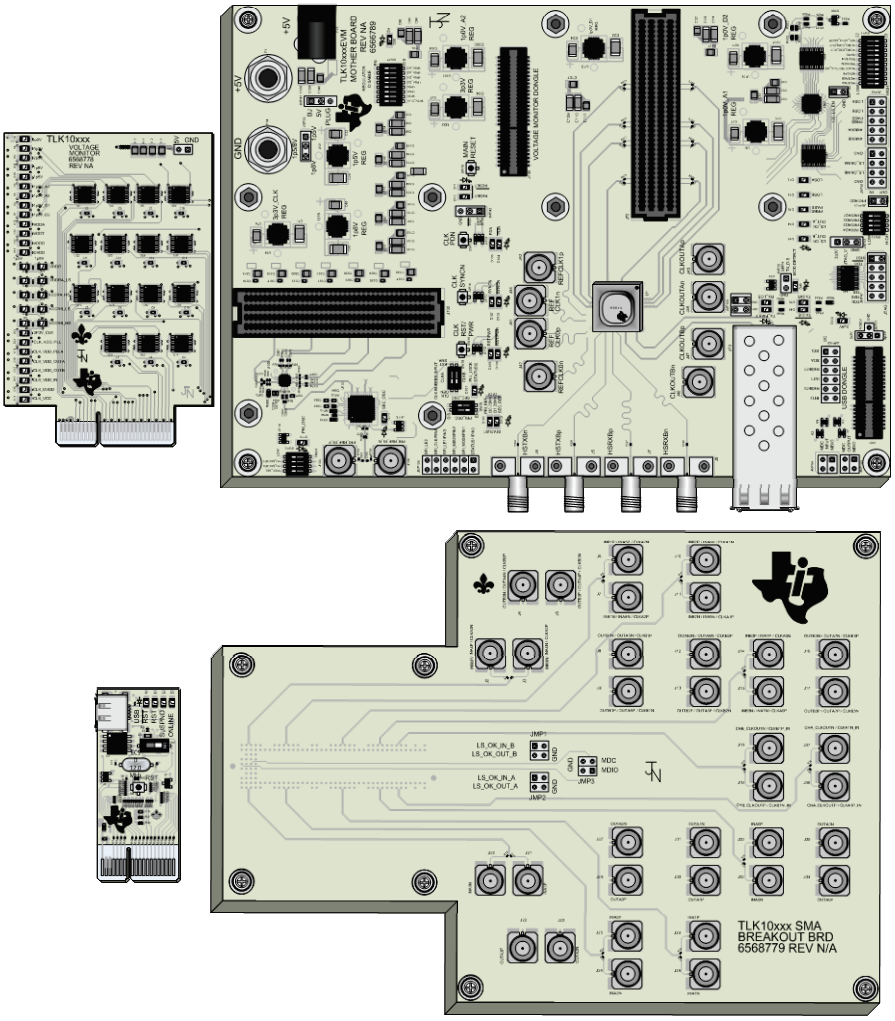
TLK10232 Dual-Channel XAUI/10GBASE-KR Transceiver with Crosspoint Evaluation Module (EVM) Graphical Users Interface User's Guide

This user's guide describes the usage and construction of the TLK10232 evaluation module (EVM). This document provides guidance on proper use by showing some device configurations and test modes. In addition, design, layout and schematic information is provided. Use the Information in this guide to help the customer choose the optimal design methods and materials in designing a complete system.



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WARNING

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user, at their own expense, will be required to take whatever measures may be required to correct this interference.

1 Introduction

TI's TLK10232 SERDES evaluation module (EVM) boards are used to evaluate the functionality and the performance of the TLK10232 Dual Channel XAUI/10GBASE-KR transceiver device in a 144-pin PBGA package.

The TLK10232 is a dual-channel, multi-rate transceiver, intended for use in high-speed bi-directional point-to-point data transmission systems. This device supports three primary modes. It can be used as a XAUI to 10GBASE-KR transceiver, as a general-purpose 8b/10b multi-rate 4:1, 2:1, or 1:1 serializer/deserializer, or can be used in 1G-KX mode.

The TLK10232 provides flexible clocking schemes to support various operations. They include the support for clocking with an externally-jitter-cleaned clock recovered from the high-speed side. The device is also capable of performing clock tolerance compensation (CTC) in 10GBASE-KR and 1GBASE-KX modes, allowing for asynchronous clocking.

Other features of the TLK10232 include an integrated latency measurement function, various PRBS, high, low, and mixed CRPAT long/short, CJPAT, and KR pseudo-random test pattern generation and verification for self test system level support. Low- and high-speed side loopback modes are provided for self-test and system diagnostic purposes. Several high- and low-speed internal loopback modes are also possible for self-test and system diagnostic purposes.

The TLK10232 has an integrated loss of signal (LOS) detection function on both high- and low-speed sides. LOS is asserted in conditions where the input differential voltage swing is less than the LOS assert threshold. The input differential voltage swing must exceed the de-assert threshold for the LOS condition to be cleared.

The low-speed side of the TLK10232 is ideal for interfacing with an FPGA or ASIC, located on the same local physical system. The high-speed side is ideal for interfacing with remote systems through an optical fiber, an electrical cable, or a backplane interface. The TLK10232 supports operation with SFP and SFP+ optical modules as well as 10GBASE-KR compatible backplane systems. Both FPGA and optical interfaces are available in this evaluation system for rapid prototyping and easy development.

Configuration of the TLK10232 on a per-channel basis is available by way of accessing a register space of control bits available through a two-wire access port called the Management Data Input/Output (MDIO) interface as defined in Clause 22 and 45 of the IEEE 802.3 Ethernet Specification. (1) The TLK10232 EVM GUI provides access to all the registers of every device used on any of the TLK10232 boards through a standard USB 1.1 interface. The boards can be configured to accept or provide MDIO signals from or to an external source by installing and uninstalling certain resistors, if necessary.

The TLK10232 EVM board can be run from one 5-V power supply and all voltages needed are regulated down through on-board LDO Regulators which can be adjusted to the appropriate minimum, nominal, and maximum values by changing a single resistor value.

Voltage monitor circuits with LEDs are included for all voltage rails for easy debugging and identification of valid power rails through the use of the voltage monitor board.

All data I/O signals are broken out to connectors for easy and rapid prototyping as well as all control signals being easily controlled through the GUI or shunts on header blocks and dip switches.

2 EVM PCB and High-Speed Design Considerations

Use the board to evaluate device parameters and to act as a guide for high-speed board layout. As the frequency of operation increases, special care must be taken to ensure that the highest signal integrity is maintained. To achieve this, the board's impedance is controlled to 50-Ω single-ended or 100-Ω differential impedance for both the low- and high-speed differential serial and clock connections. Vias are minimized and, when necessary, are designed to minimize impedance discontinuities along the transmission line. Care was taken to control trace length mismatch (board skew) to less than ±0.5 MIL.

Overall, the board layout is designed and optimized to support high-speed operation. Thus, understanding impedance control and transmission line effects are crucial when designing high-speed boards. Some of the advanced features offered by this board include:

- TLK10232 PCB (printed-circuit board) is designed for optimal high-speed signal integrity using Rogers Material for the outer signal layers and FR-4 for the inner layers. All Gigabit and clock signals are

(1) The MDIO register map is located within the TLK10232 Quad-Channel XAUI/10GBASE-KR Transceiver with Crosspoint datasheet.

routed over the Rogers Material for minimal signal loss. The FPGA and SMA breakout daughterboards use FR-4 for all layers.

- SMA and header fixtures are easily connected to test equipment.
- All input/output signals are accessible for rapid prototyping.
- On-board capacitors provide AC coupling of differential transmit and receive signals. Zero-Ohm resistors have been placed on the transmit pins so that external loopback tests can be implemented and only a single AC-coupling capacitor on the RX pins will be located in between the TX and RX signals. If the TX signals need to be evaluated on their own, the 0-Ω resistors can be replaced with 0.1-µF capacitors.
- The high-speed signals of channel A have been routed to SFP+ modules for easy evaluation in systems that implement optical fiber configurations. The high-speed signals of channel B have been routed to edge launch SMA connectors for easy evaluation in systems that use standard test equipment.
- The low-speed signals of all four channels have been routed to Samtec SEAM/SEAF board-to-board connectors allowing for smaller EVM PCB size and additional options for evaluation of these signals. An SMA breakout board is optionally supplied that will allow for access to these low-speed signals. SMA cables can be connected from the input signals to the output signals to create an external loopback situation, or to standard lab test equipment. The pinout is compatible with the TLK10002 EVM FPGA daughterboard and any variety of custom interface boards could be created for use with the TLK10232 EVM motherboard.
- The MDIO data signals have been routed to the TLK10232 and the bus continues to a 0.10-in header allowing for multiple boards to be daisy chained on a single MDIO Bus.
- This board can operate in standalone mode using an external MDIO data controller and the hardware control pin settings, or through the USB dongle interface. The use of the USB dongle is recommended and the preferred mode of operation. All control pins of the TLK10232 device have also been connected to TI's TCA6424 I^2C-to-GPIO device and when using the supplied TLK10232 EVM GUI and USB interface, these control pins should be set to a high voltage or logic "1" in hardware and controlled through the GUI interface allowing the TCA6424 to pull the signals low when needed.

3 TLK10232 EVM Kit Contents

The TLK10232 EVM kit contains the following:

- TLK10232 EVM motherboard
- TLK10232 EVM USB dongle board
- TLK10232 EVM Voltage monitor board
- TLK10232 EVM SMA breakout board (optional)
- TLK10232 EVM User's Guide (this document)
- Banana jack power adapter cables
- USB cable
- CD-ROM containing user interface software

4 Power

The TLK10232 EVM motherboard can be powered from one 5-V power supply. The 5-V power supply powers the board's general logic ICs and LDOs as well as the board's LEDs. The power from the LDOs is split into the planes through 1210 zero-Ω resistors that could be replaced with a ferrite bead or inductor of the user's choice, should the need arise to filter out any noise that may be present. A series of bulk decoupling capacitors are placed at the entry point of the split planes immediately following the 1210 zero-Ω resistors. Additional local decoupling capacitors are placed near the power pins of the devices connected to the planes in order to source instantaneous switching current and help with noise filtering. The 5-V supply input should have a current ability of approximately 2.5 A, if running in the heaviest power device configurations.

The LDO regulators used on the EVM are TI's TPS74401 and are adjustable using a resistor divider between the output and a feedback pin. Each regulator has been set to provide the appropriate voltage with a slightly higher margin at the source to account for IR drop across the board since there are no sense lines on these regulators. If more information on the use of these regulators is desired, please consult the regulator datasheets found at www.ti.com.

Several power supplies such as VDDRA_LS/HS, VDDRB_LS/HS, and VDDO can be operated off of either 1.5 V or 1.8 V, depending upon your specific setup. The EVM is designed to allow either of these voltages to be selected for use with the previously mentioned TLK10232 supply rails, but will only allow either 1.5 V or 1.8 V to be selected at a time. Selection between 1.5 V and 1.8 V is performed by moving the jumper between the center pin and the respective 1p5V and 1p8V pins of JMP35.

Refer to Section 11 for more detailed information on the regulators and power distribution circuitry.

5 Voltage Monitoring Board and Power Rail LEDs

The voltage monitoring board has window detection circuits that drive LEDs which provide a quick indication that the voltage is within specification. The voltage monitor board draws power from the 5-V plane on the motherboard and a sense line to every power rail on the board is connected to the samtec MEC1 connector. If the voltage on the sense line is within the minimum or maximum limit for that particular plane, the window detection circuit will cause the LED to turn on as an indicator that the plane is properly sourced. If the voltage is outside the minimum or maximum limits, then the LED will fail to light and the user will be informed that there is a problem with the power on that rail and that the TLK10232 device may not function properly. Several of the power planes on the TLK10232 can be supplied from either 1p5V or 1p8V and a separate LED and monitor circuit have been supplied for each case, allowing a check of the voltage configuration on the board. The voltage monitor board is not required for operation of the TLK10232 EVM motherboard and this board is supplied as a tool to be used full time or as a debug device. Hot swapping this board should not cause any damage to either the TLK10232 EVM motherboard or the voltage monitoring board.

The LEDs should be used as a basic indication of the status of power on the board being within the acceptable min and max limits given in the datasheet, and not as a precise measurement tool as some LED circuits may turn off at slightly different voltages when approaching the limits due to the manufacturing tolerances and available resistor values.

6 Control and Output Status Signals

All of the external control and status pins on the TLK10232 EVM have been consolidated to a single location on the board and broken out onto several header blocks and dip switches. LEDs have been added to the LOSA/B, LS_OK_OUT_A/B, and PRBS_PASS signals in addition to the headers for scope probes, to allow easy monitoring of the high/low value on the lines. The LED will be ON when the line is a logic high, and the LED will be OFF when the line is a logic low.

All status pins and external control pins of the TLK10232 can also be monitored or set high/low through the GUI. The preferred method of setting these control pins is through the GUI via the TCA6424 I^2C-to-GPIO IC located on the board. If shunts are placed on the header for a particular control pin, or if the dip switch setting is set low, the signal will be physically tied low and software control will not be possible. Mixed use of the hardware and software setting of various control pins is discouraged.

The I^2C-based software control of the TLK10232 control pins can be disabled by placing a shunt on JMP100 which will disable the level shifter attached to the signals by setting the enable pins low or by selecting the "Disable Software Control of Pins" radio button located on the front panel of the GUI. This will allow the onboard pullup resistors or shunts to ground on the header pins to set the high/low status of the control pins. If external control is desired and a shunt is placed on JMP100, the "Disable Software Control of Pins" radio button on the GUI front panel should be de-selected as well, to disable the software portion of the interface.

The TCA6424 device will respond to either I^2C device address 0x22 or 0x23. When two boards are used and daisy chained together, the I^2C address must be changed on the one of the two boards so that there is individual control of both boards. Flipping the switch on SW11 will change the address from 0x22 to 0x23.

See the TLK10232 datasheet (SLLSEE1) for a detailed description of the control signals.

7 MDIO

The TLK10232 supports the Management Data Input/Output (MDIO) Interface as defined in Clause 22 and Clause 45 of the IEEE 802.3 Ethernet specification. The MDIO allows register-based management and control of the serial links. Normal operation of the TLK10232 is possible without the use of this interface, however, most additional features are accessible only through the MDIO interface.

The MDIO Interface consists of a bi-directional data path (MDIO) and a clock reference (MDC). The port address is determined by control pins PRTAD[4:0] as described in the TLK10232 Datasheet.

The top 4 control pins PRTAD[4:1] determine the device port address and are set in hardware on the board. The two individual channels in TLK10232 are classified as 2 different ports. So for any PRTAD[4:1] value there will be 2 ports per TLK10232. The TLK10232 will respond if the 4 MSB's of PHY address field on MDIO protocol (PA[4:1]) matches PRTAD[4:1]. The LSB of PHY address field (PA[0]) will determine which channel/port within the TLK10232 to control.

If PA[0] = 0, TLK10232's channel A will respond.

If PA[0] = 1, TLK10232's channel B will respond.

Write transactions which address an invalid register or read only registers will be ignored. Read transactions of invalid registers will return a "0". The TLK10232 requires either 1.5-V or 1.8-V I/O levels on the MDIO/MDC signals. Therefore, a bi-directional level shifter has been provided on board that level shift the 3.3-V MDIO and MDC signals to the appropriate 1p5 and 1p8V levels. Should a different MDIO controller be used that already has 1.5-V or 1.8-V signal levels, resistors R298, R299, R451, and R491 should be removed, thus disconnecting the level shifter and resistors R293, R295, R634, and R635 can be installed which will connect the TLK10232 MDIO and MDC signal pins directly to the pins of JMP50.

The USB dongle implementing TI's TUSB3210 microcontroller is the preferred method of controlling the TLK10232 register stack and is the ONLY way to interface the GUI with the board. When the USB Dongle is connected to the EVM board through the Samtec MEC1 connector, the MDIO signals will be at 3p3V levels because the TUSB3210 is a 3p3V device with open drain architecture. The EVM board has TI's TXS0108EPWR bi-directional level shifter to convert the MDIO signals to the 1p5/8V levels required by the TLK10232. Ensure that a shunt is placed on the 3p3V and MDIO_LS pins of JMP77 on the EVM board to ensure that the appropriate 3p3V voltage is used on the Level Shifter and pull up resistors. The 2p5V voltage option is supplied for TI use only with a legacy MDIO Controller.

MDIO signals can be routed to either of the low-speed board-to-board connectors for use with the TLK10002 EVM FPGA daughterboard or other interface boards that may require MDIO communication on the same MDIO bus as the TLK10232. Currently this feature is not supported but will be available at a future time. Control over the relays used to route the MDIO bus without creating stub branches is done using the SW11 switch, or through the TCA6424 I^2C interface and GUI.

The MDIO PRTAD[4:1] is defaulted to 4b'0000. If this value is changed in hardware it must also be changed in the GUI so that proper MDIO communication is possible.

8 JTAG

The EVM also provides a separate connector to support the full five-pin JTAG interface of the TLK10232 with on-board level shifters for compatibility with most standard JTAG control interfaces to be used for manufacturing tests. The 3.3-V (header) side of the level shifter is connected to the header and the 1p5/8V side of the Level Shifter is connected to the TLK10232. If the Level shifter is not needed, providing an external voltage of the appropriate signal level between pins 2 and 3 of JMP62 should allow the signals to pass to the TLK10232 correctly.

9 Reset

The TLK10232 EVM comes configured for manual reset operations involving the pushbutton reset switch (SW10). When switch SW10 is pressed, the TLK10232 device RESET pin (RST_N) goes LOW and the entire TLK10232 device is reinitialized. A TI TPS3125J18 ultra-low voltage processor supervisory circuit is used to control the reset line. During power-on, the /RESET pin of U12 is asserted when the supply voltage becomes higher than 0.75 V. Thereafter, the supply voltage supervisor monitors the voltage and keeps /RESET output active as long as the voltage remains below the threshold voltage (VIT). An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. The delay time, td = 180ms, starts after the voltage has risen above the threshold voltage (VIT).

There is also a manual reset input to the supervisory circuit, /MR, which accepts the input from the pushbutton switch SW10. A low level at /MR causes /RESET to become active, thus resetting the TLK10232 device whenever the pushbutton RESET is pressed. By placing a jumper on JMP42, the manual reset (/MR) is tied hard to ground causing the TLK10232 to be held in a constant state of reset without the need to continually hold the reset pushbutton SW10. The supervisory circuit will release the reset line to a HIGH 180 mS (td) from the time the /MR line becomes greater than the threshold voltage (VIT).

NOTE: In order to keep the GUI settings and the device settings synchronized during the evaluation of the TLK10232, all RESET commands should be issued through the GUI via the TCA6424 I^2C-to-GPIO device connected to the signals. When the software “Main Board Reset” buttons are pressed, the GUI will adjust its memory settings of the various registers in order to match the new values the devices will reflect after the hardware RESET is performed. If the buttons are pressed on the board, the GUI will not reflect the devices true status and may result in erroneous results during testing because the device is not configured according to the GUI’s displayed results.

Depending upon the power down or the GUI termination sequence followed, the USB device may need to be RESET to allow re-enumeration to occur in future tests. When the board is powered on and the USB connection is enumerated, the USB online LED (D4) should light on the USB dongle board. If this LED fails to light, there may be a PC-related issue, the PC should be restarted and the LED should light once the PC error is fixed. If the USB connection is improperly disconnected or terminated, the USB SUSPEND Light, D3, should light and is an indication that the USB connection is not properly established. A Reset pushbutton is located on the USB dongle board and pressing this device will reset the TUSB3210 microcontroller as well as momentarily disconnect the USB device from the PC’s USB bus causing the PC to re-enumerate the device after the reset is complete.

10 Test and Setup Configurations

More detailed test setups and descriptions will be added in future revisions of this document.

The TLK10232 EVM has an SPF+ optical module cage attached directly to the channel A high-speed signals with approximately 3 inches of trace over Rogers Low-Dielectric material. Channel B’s high-speed signals are attached to edge launch SMA connectors with 0.1-µF AC-coupling capacitors on the RX lines, and 0-ohm resistors on the TX lines to facilitate an external loopback configuration with only a single set of capacitors in line. The caps or resistors should be carefully reworked as necessary to facilitate the test needs during evaluation. Placing two 0.1-µF AC-coupling capacitors can result in lower performance and greater numbers of bit errors.

All low-speed signals on the input signals have 0.1-µF AC-coupling capacitors and are routed to a Samtec SEAF board-to-board connector that will mate with either a SMA breakout board for use in parametric and lab testing, or a Spartan-6 FPGA board for system-level evaluation. The output signals are connected to 0-Ω resistors allowing them to be connected to the AC-coupled input signals. These 0-Ω resistors could be easily re-worked with 0.1-µF capacitors for AC-coupled applications.

The MDIO bus that is connected to the TLK10232 is also routed to the SEAF board-to-board connector and can be used to interface with either the FPGA or an external system board via the post level shifter MDIO signal header on the SMA breakout board.

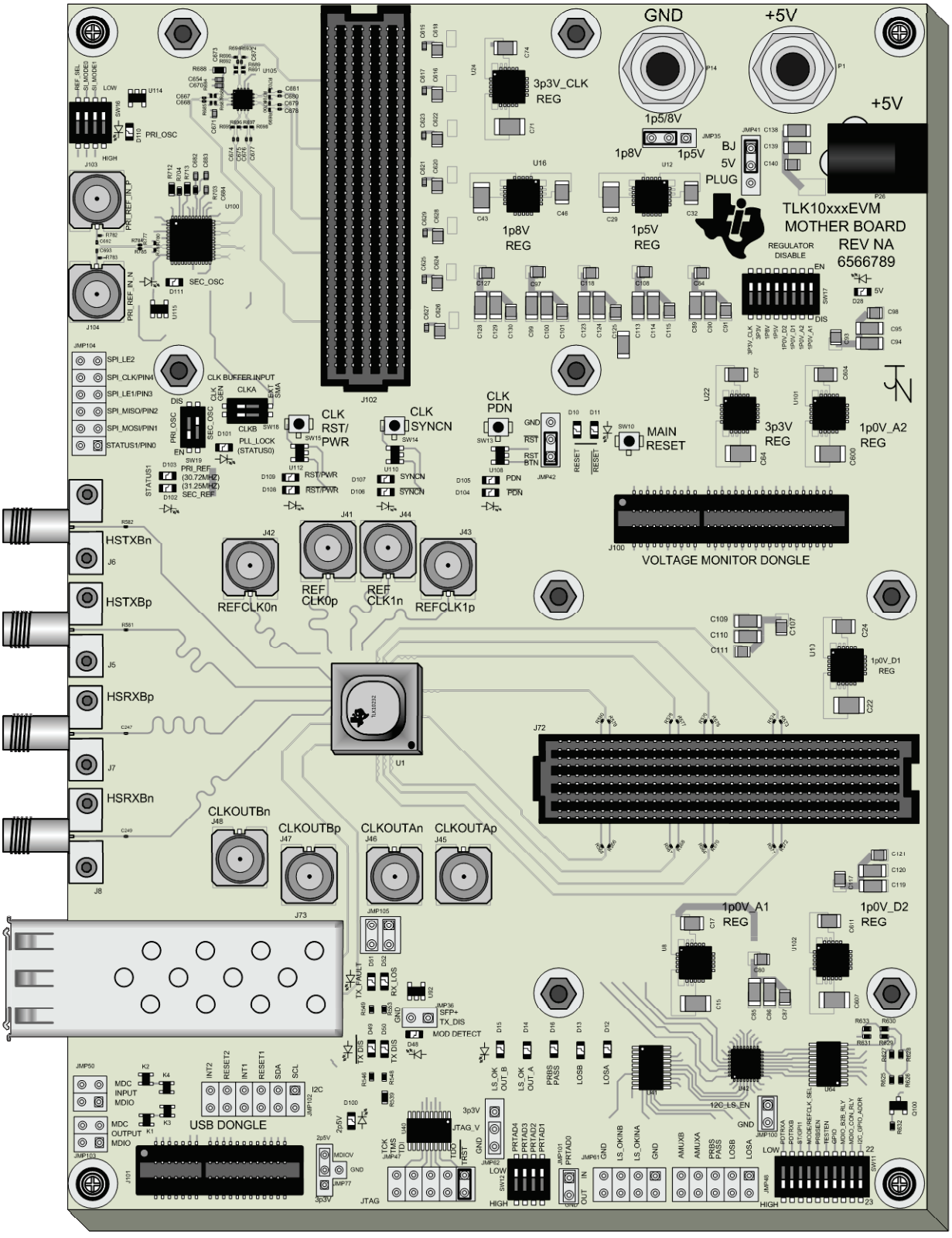

Figure 1. TLK10232 EVM Motherboard

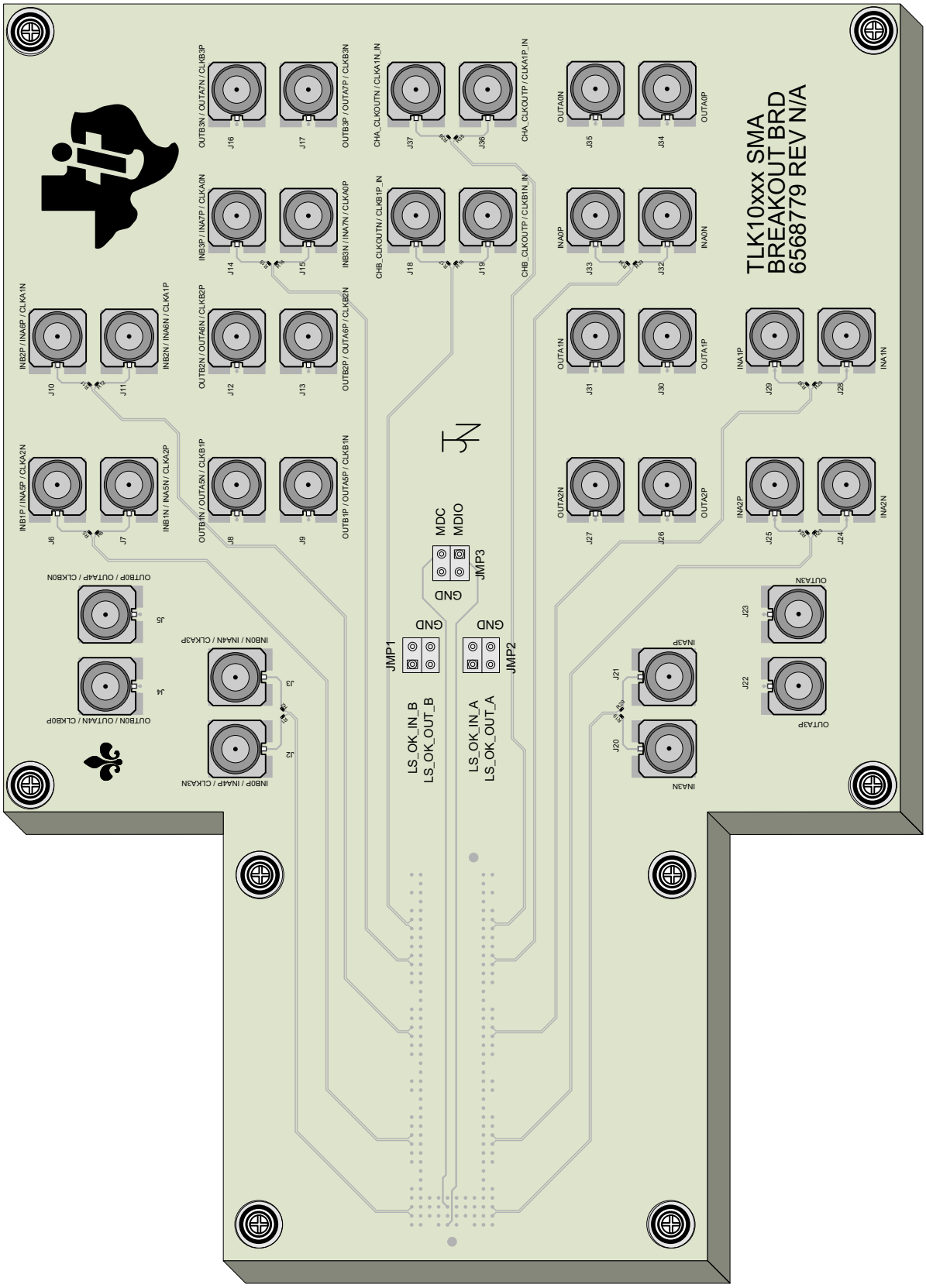

Figure 2. TLK10232 EVM SMA Breakout Board

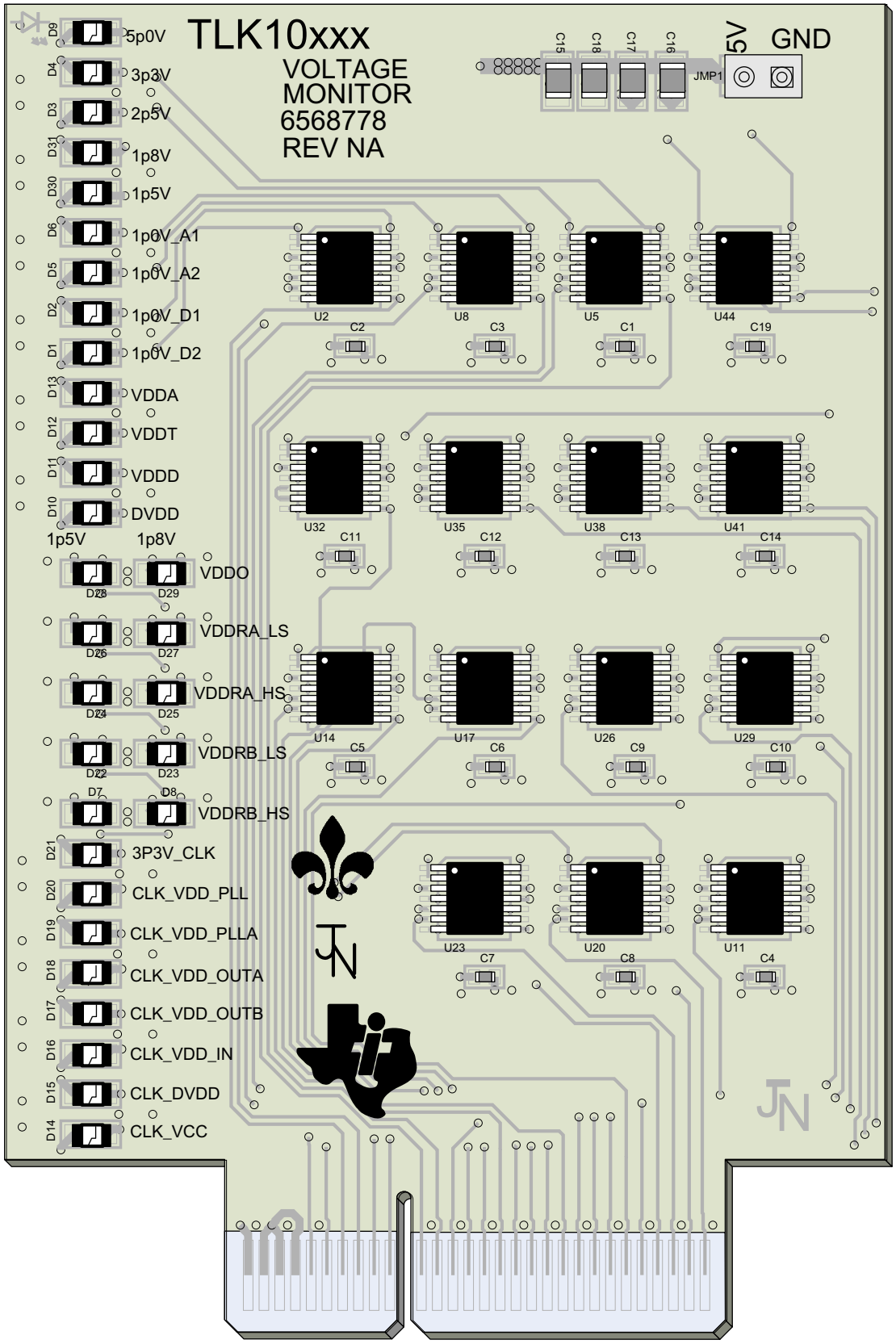

Figure 3. TLK10232 EVM Voltage Monitor Board

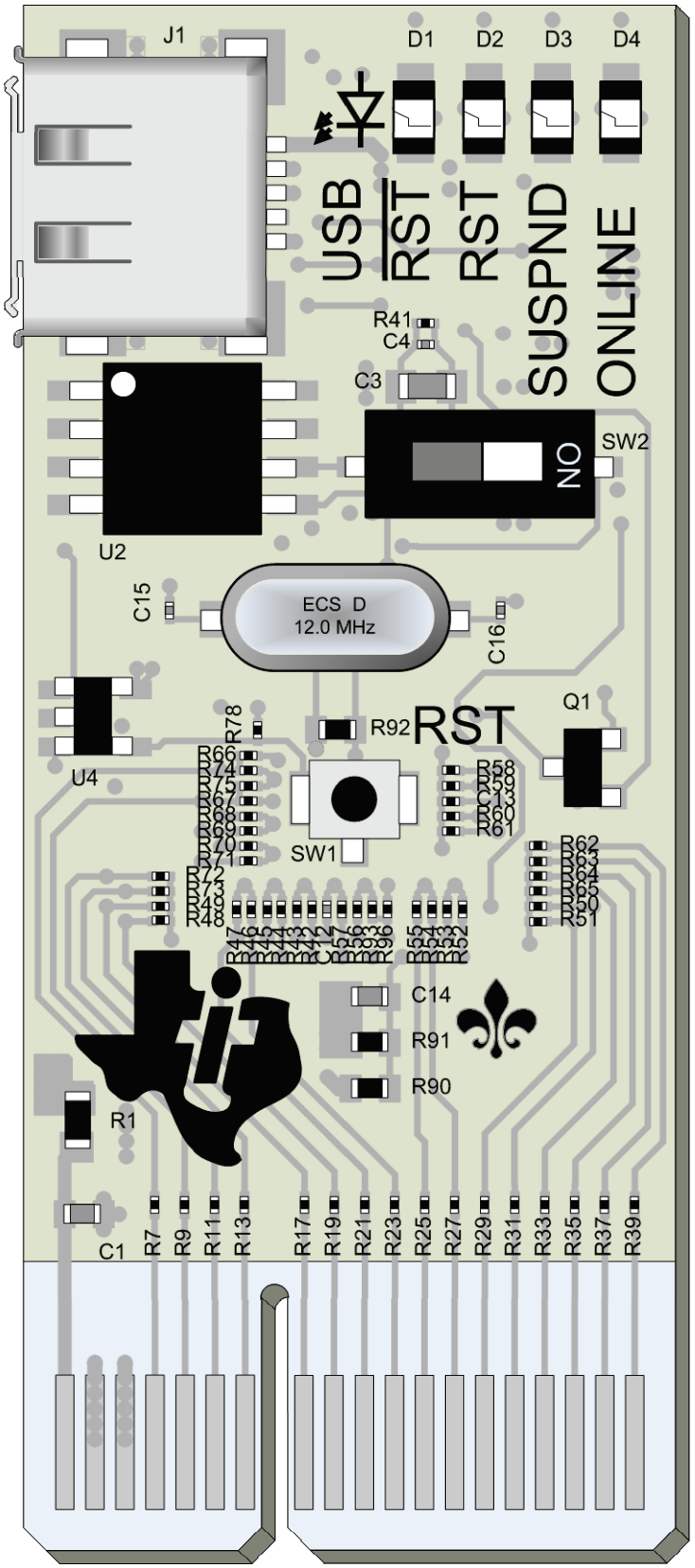

Figure 4. TLK10232 EVM USB Dongle Board

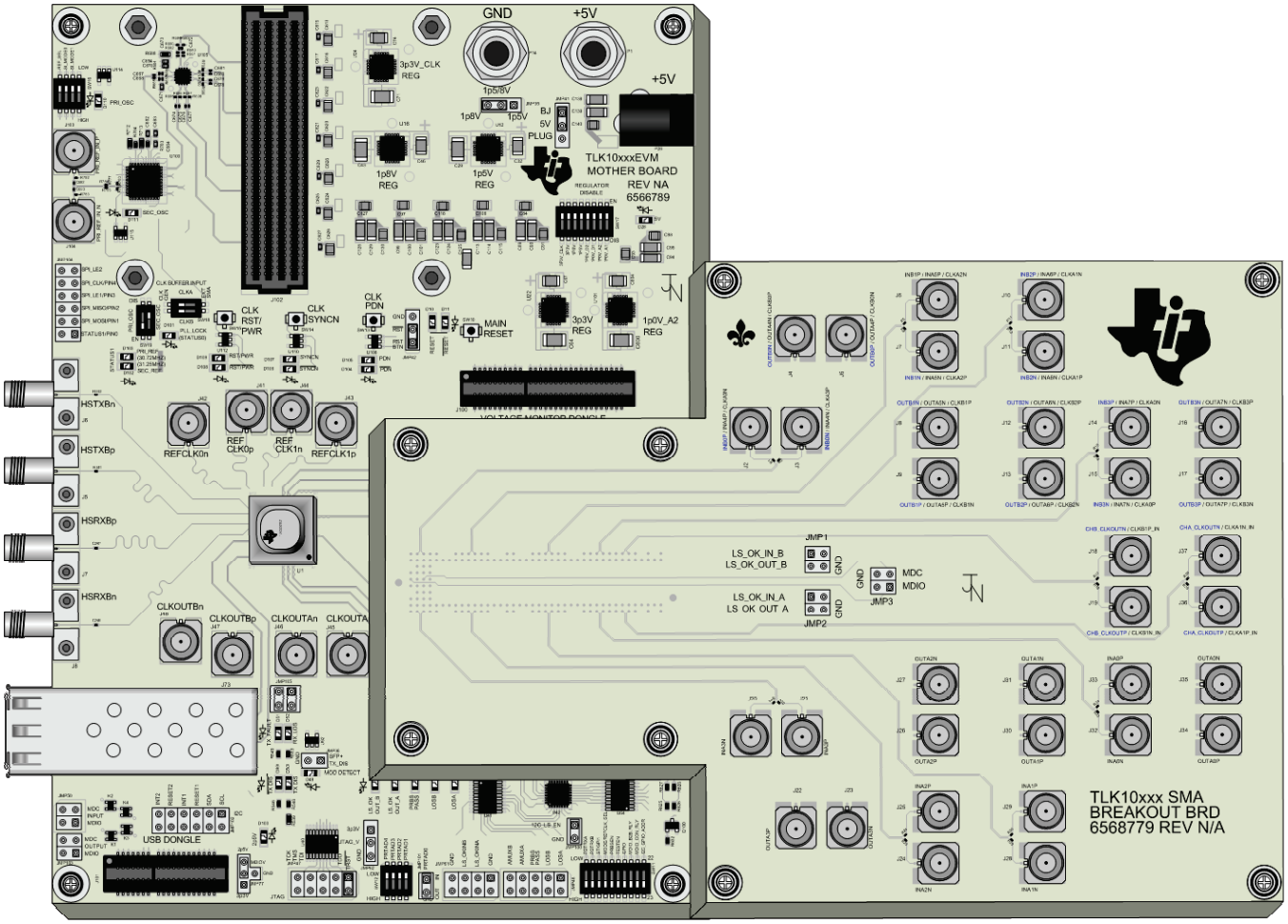

Figure 5. TLK10232 EVM Motherboard and SMA Breakout Board for Channels A/B

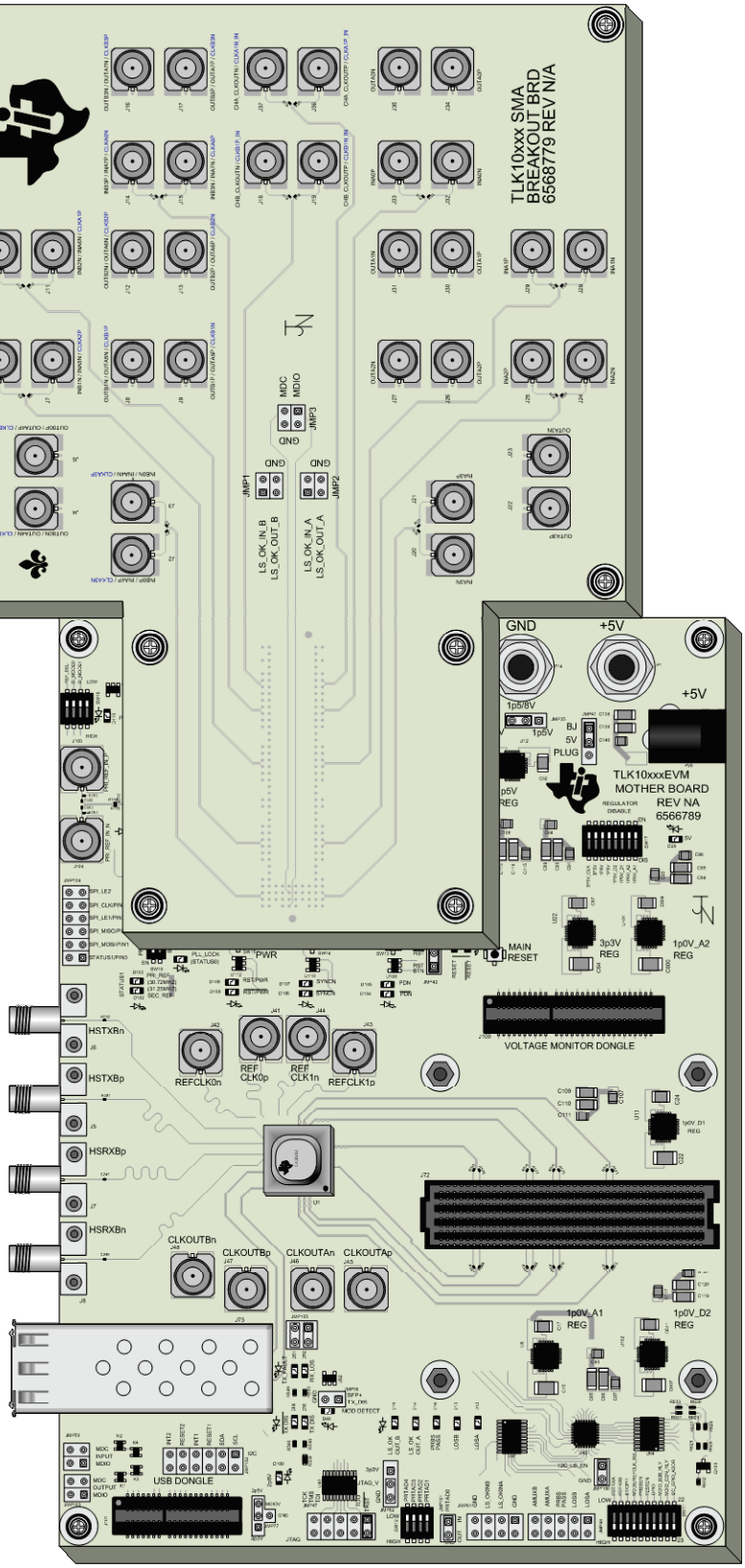

Figure 6. TLK10232 EVM Motherboard and SMA Breakout Board for Clock Channels

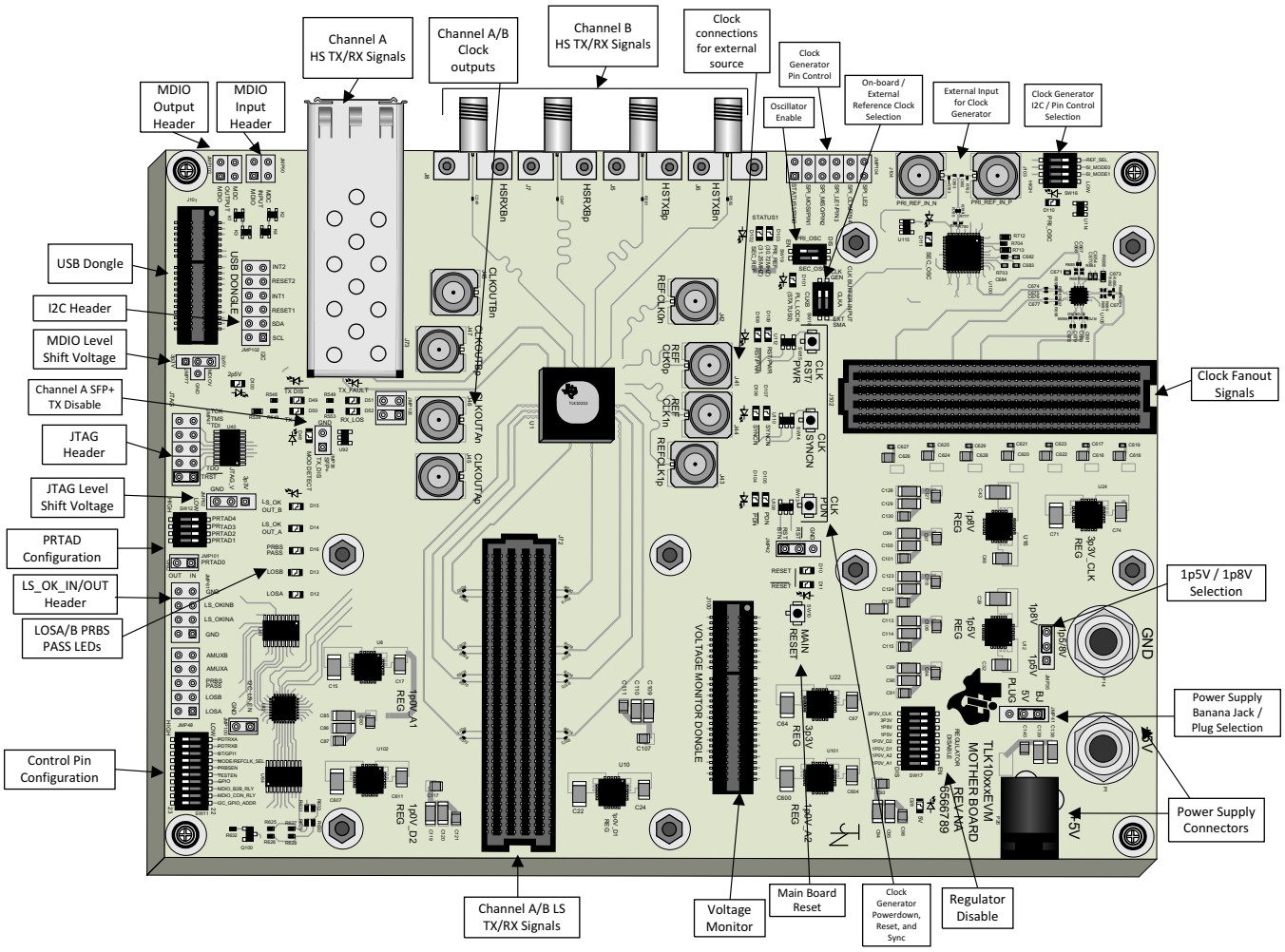

Figure 7. TLK10232 EVM Board Features

11 TLK10232 EVM Motherboard Schematics

Figure 8 through Figure 22 show the EVM motherboard schematics.

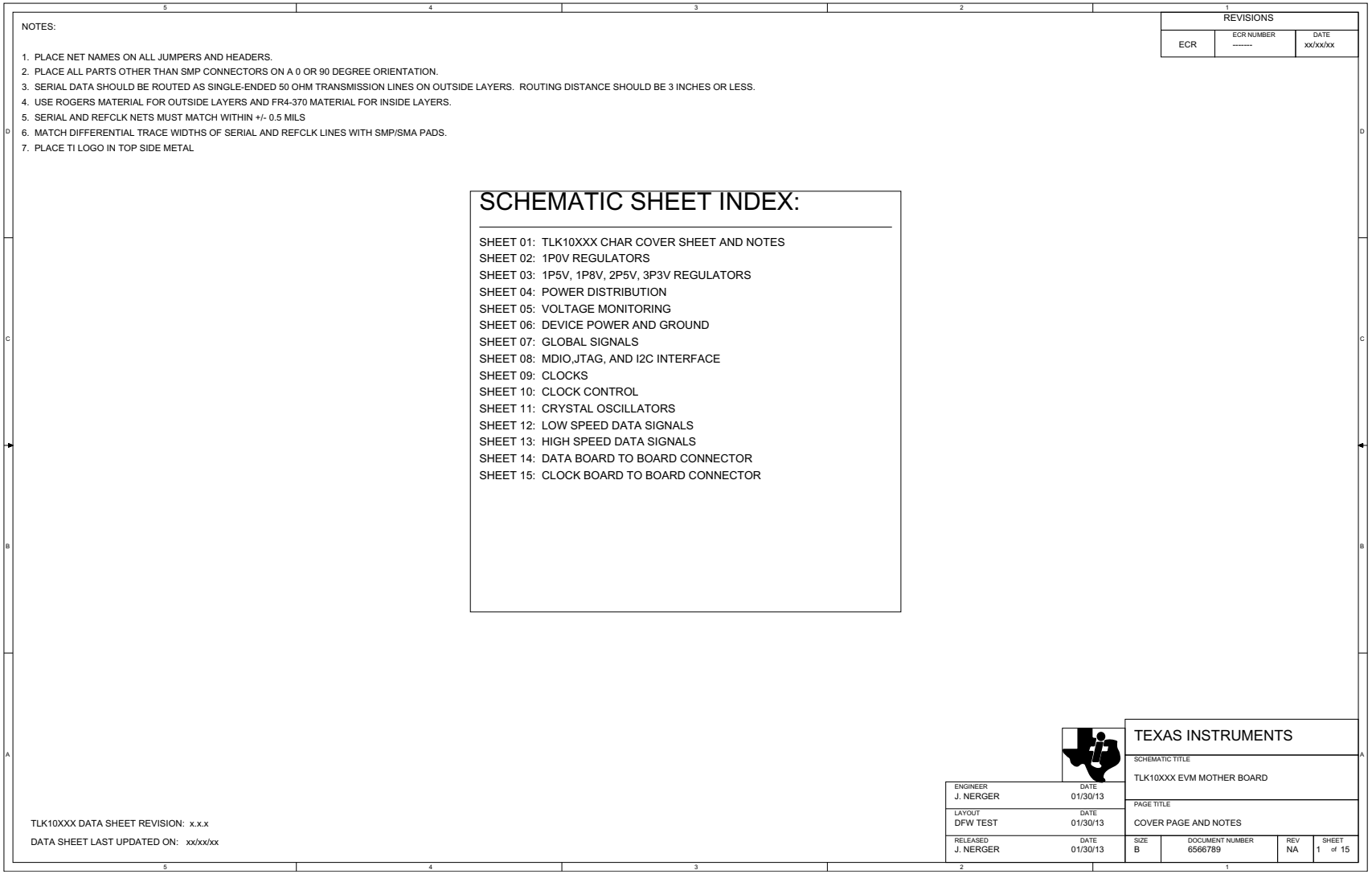

Figure 8. TLK10232 EVM Schematic, Sheet 1 Cover Page and Index

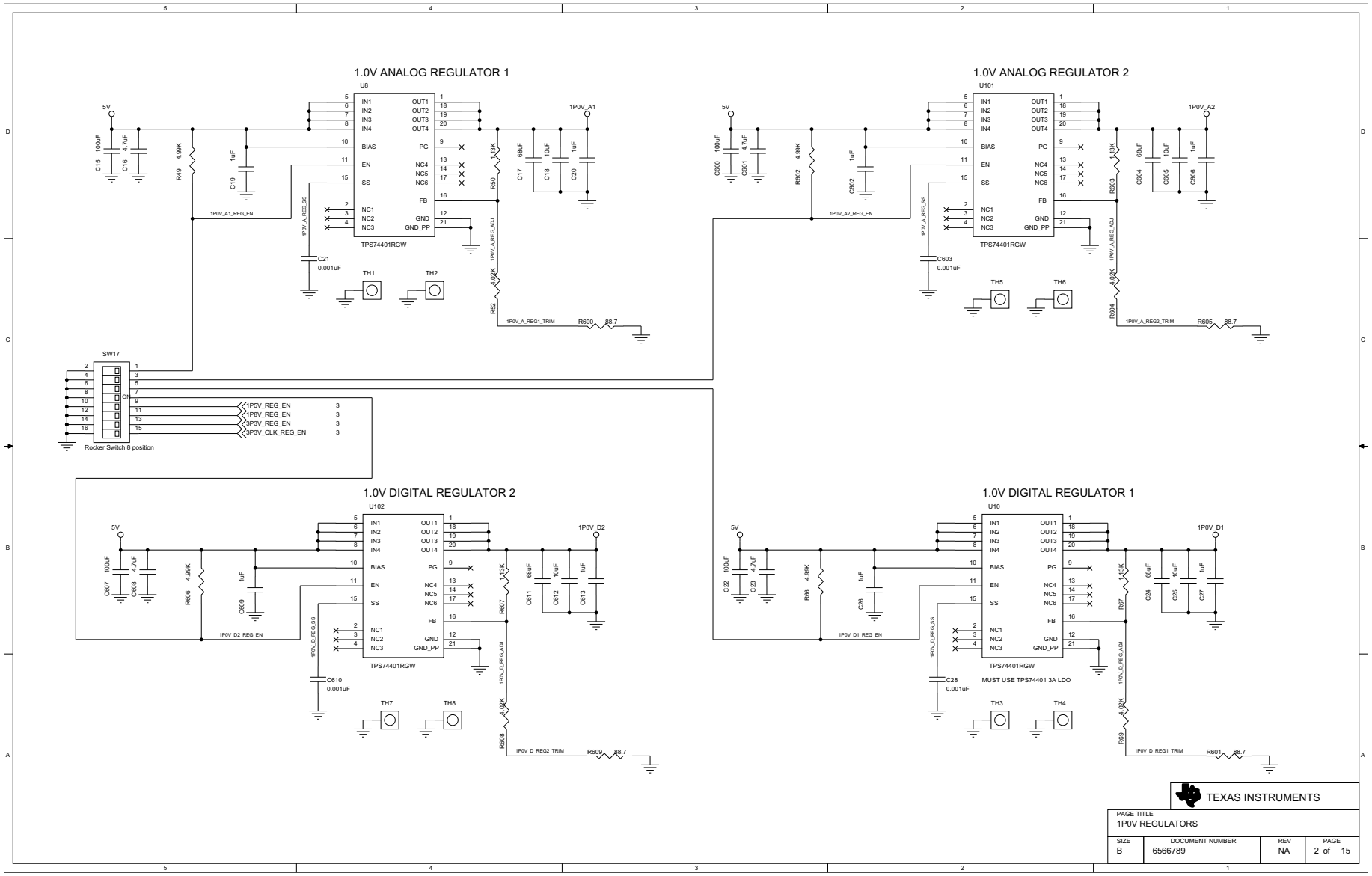

Figure 9. TLK10232 EVM Schematic, Sheet 2 1p0V Regulators

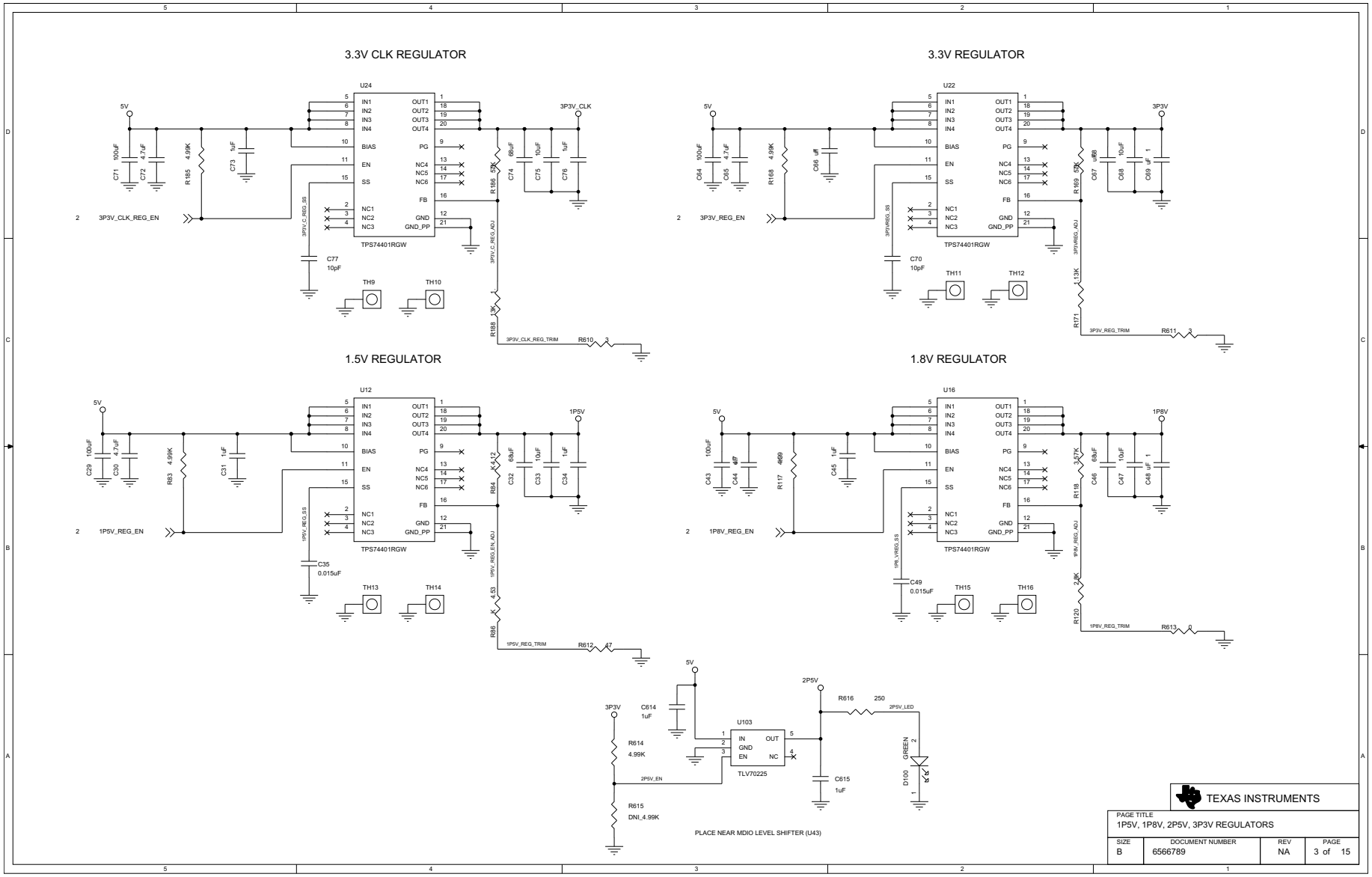

Figure 10. TLK10232 EVM Schematic, Sheet 3 1p5V, 1p8V, 2p5V, And 3p3V Regulators

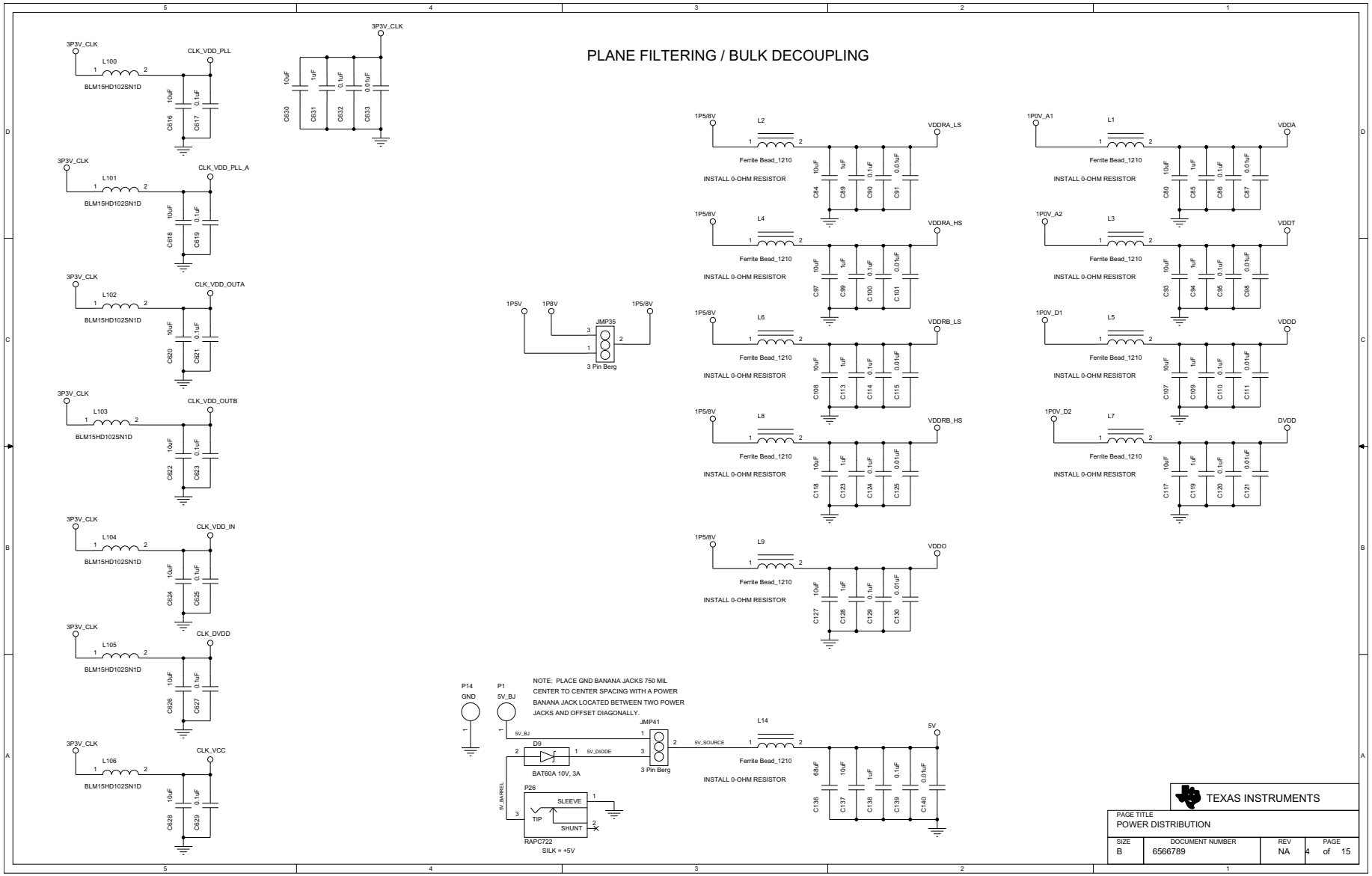

Figure 11. TLK10232 EVM Schematic, Sheet 4 Power Distribution

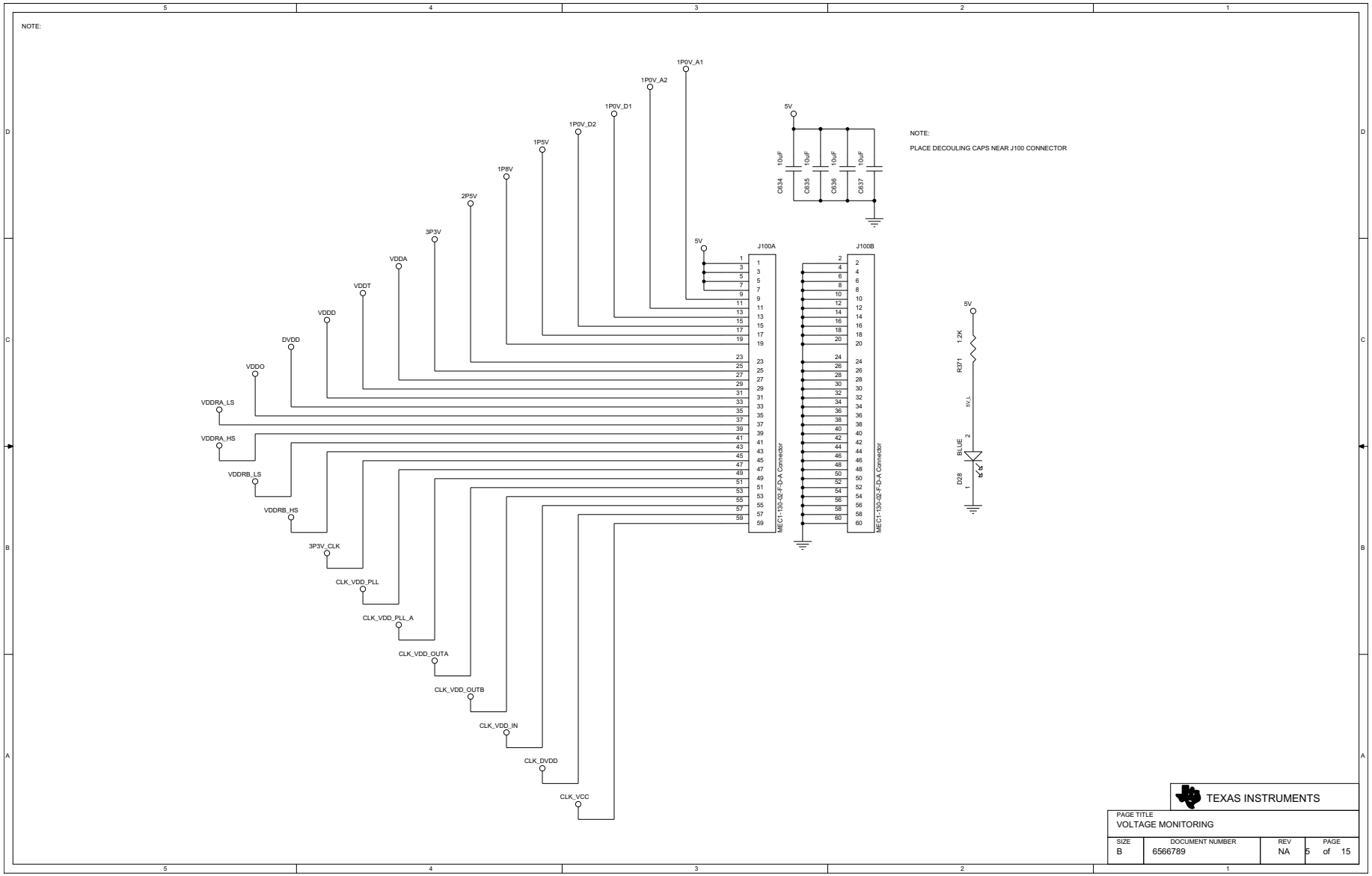

Figure 12. TLK10232 EVM Schematic, Sheet 5 Voltage Monitoring

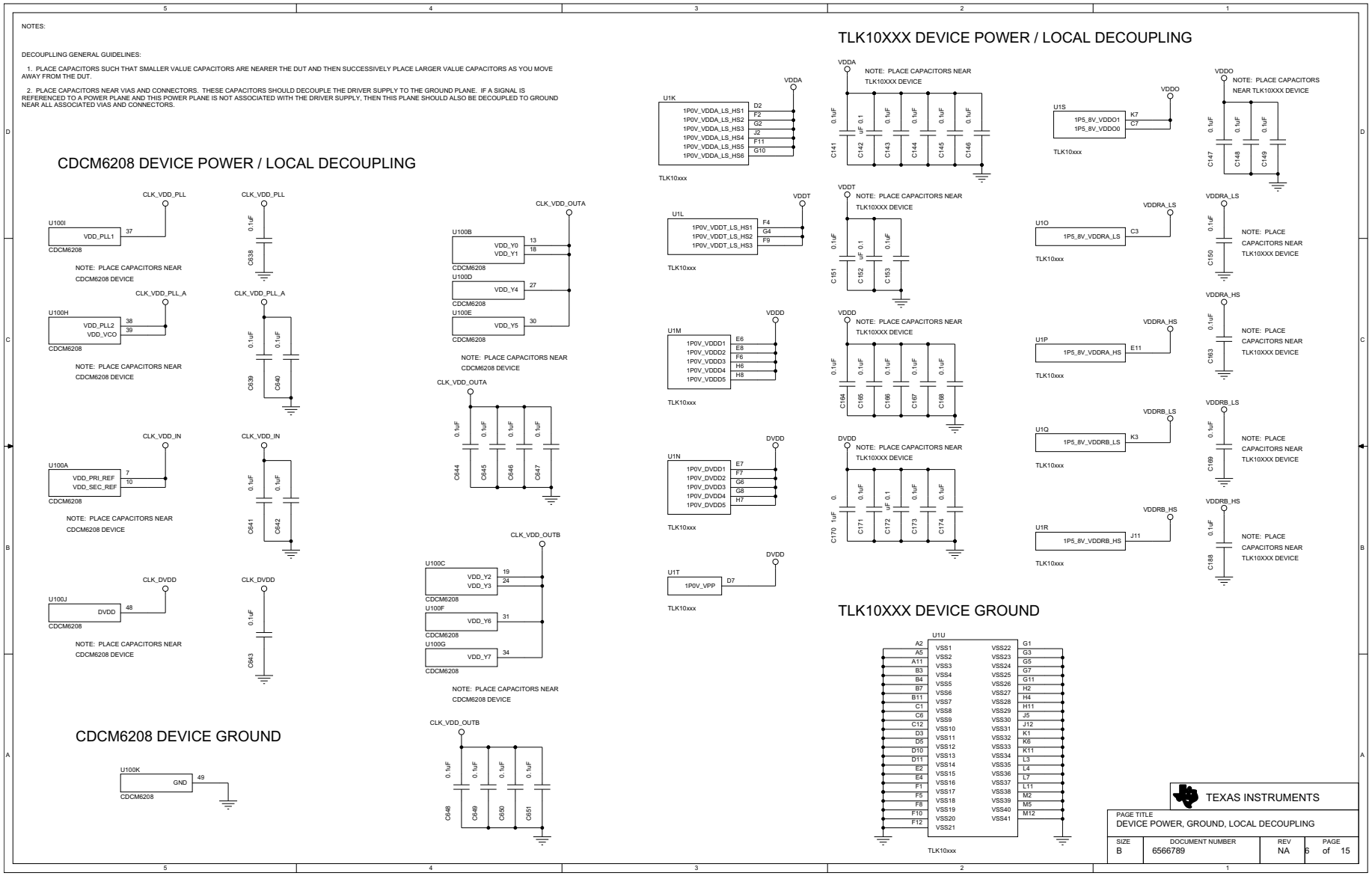

Figure 13. TLK10232 EVM Schematic, Sheet 6 Device Power, Ground, and Local Decoupling

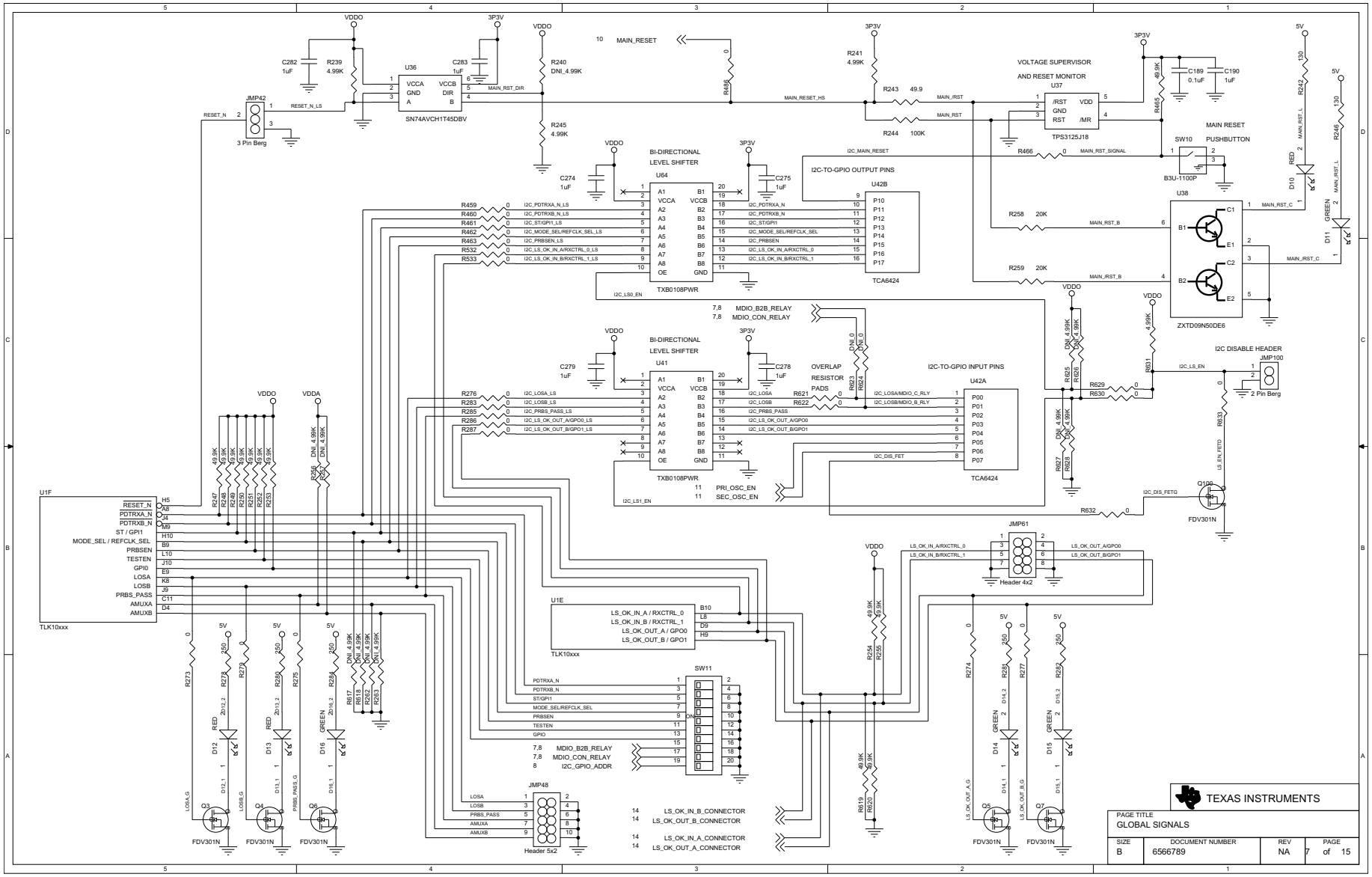

Figure 14. TLK10232 EVM Schematic, Sheet 7 Global and Control Signals

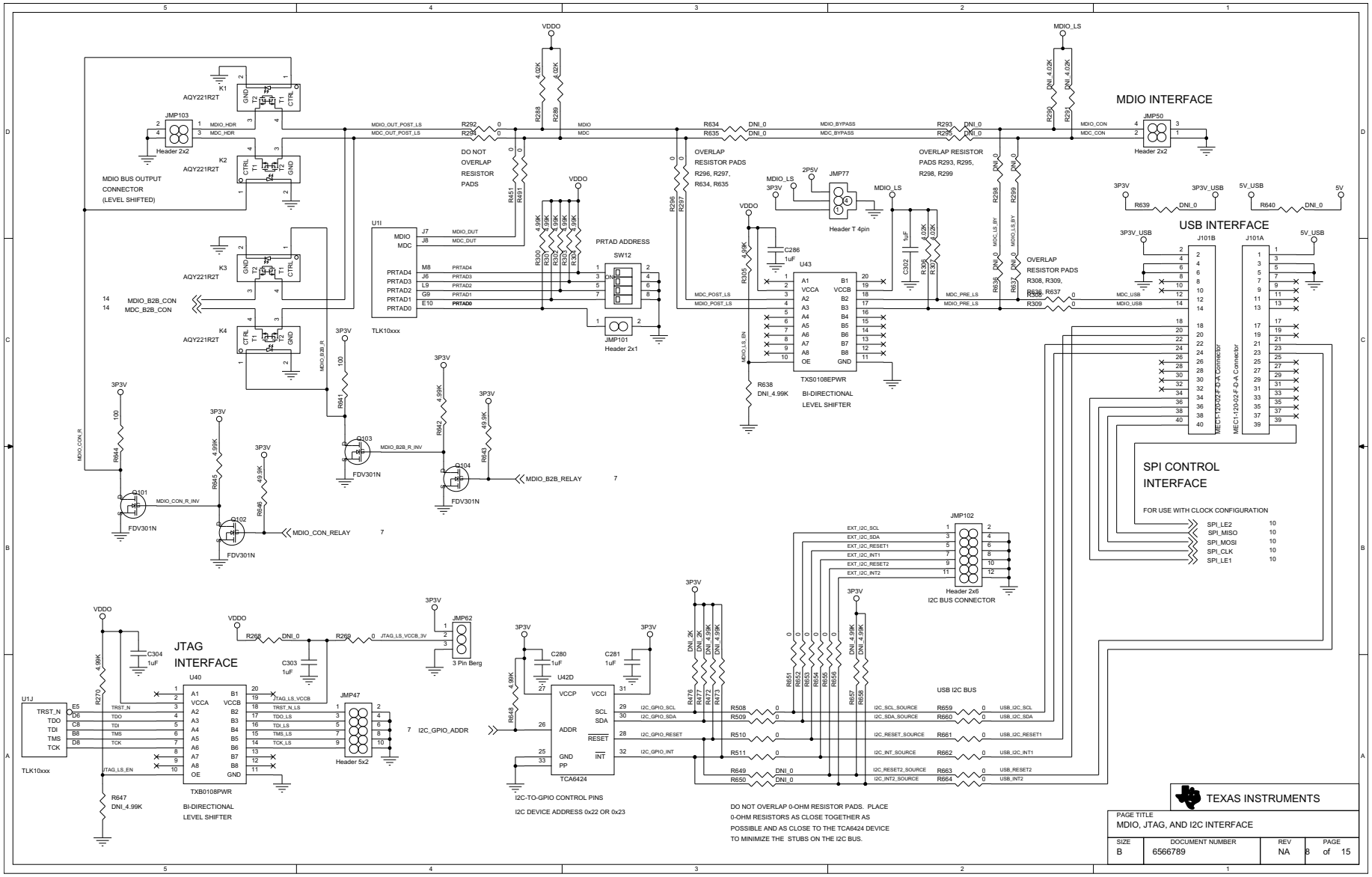

Figure 15. TLK10232 EVM Schematic, Sheet 8 USB, MDIO, JTAG, and I²C Interface

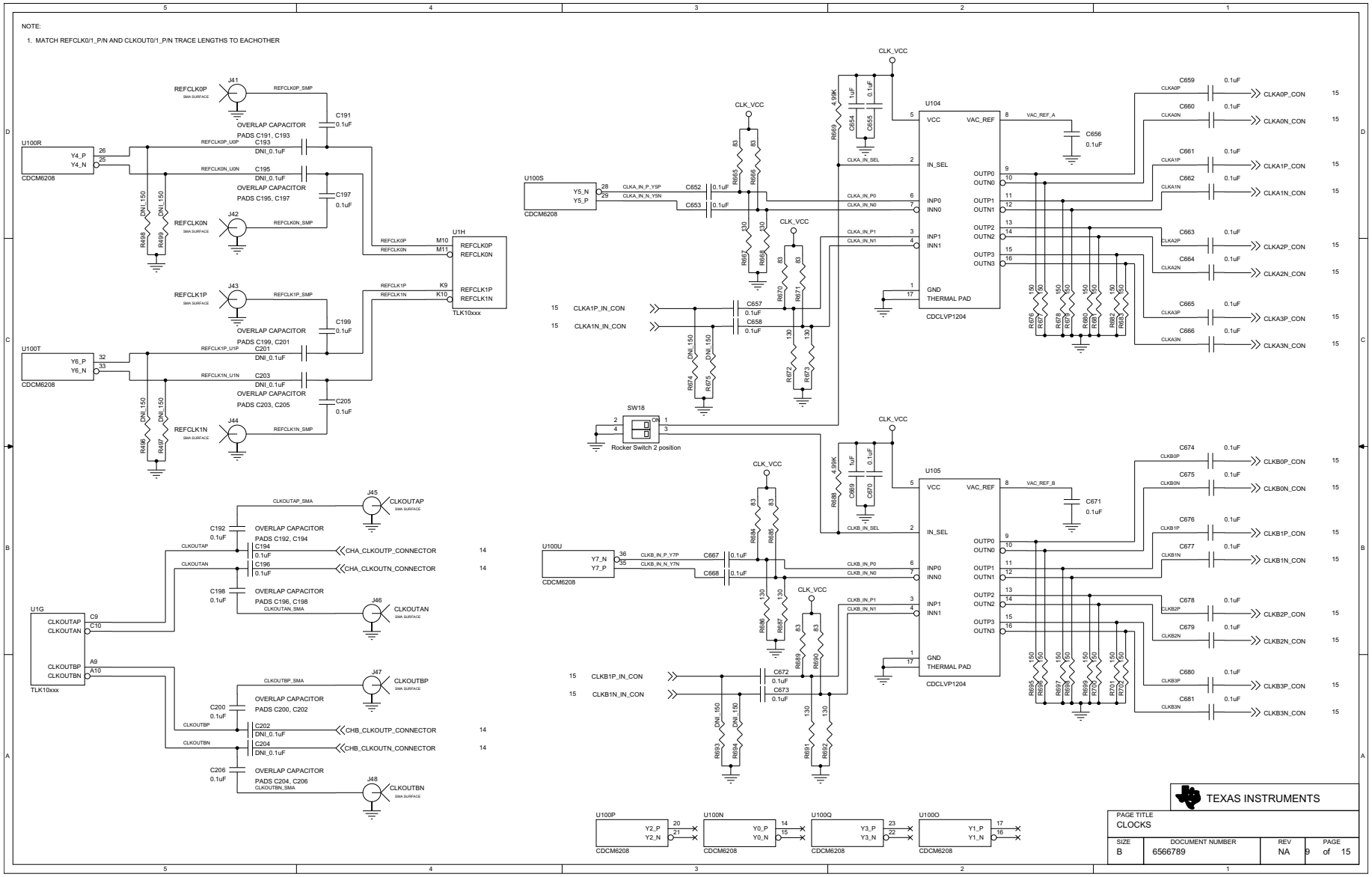

Figure 16. TLK10232 EVM Schematic, Sheet 9 Clocks

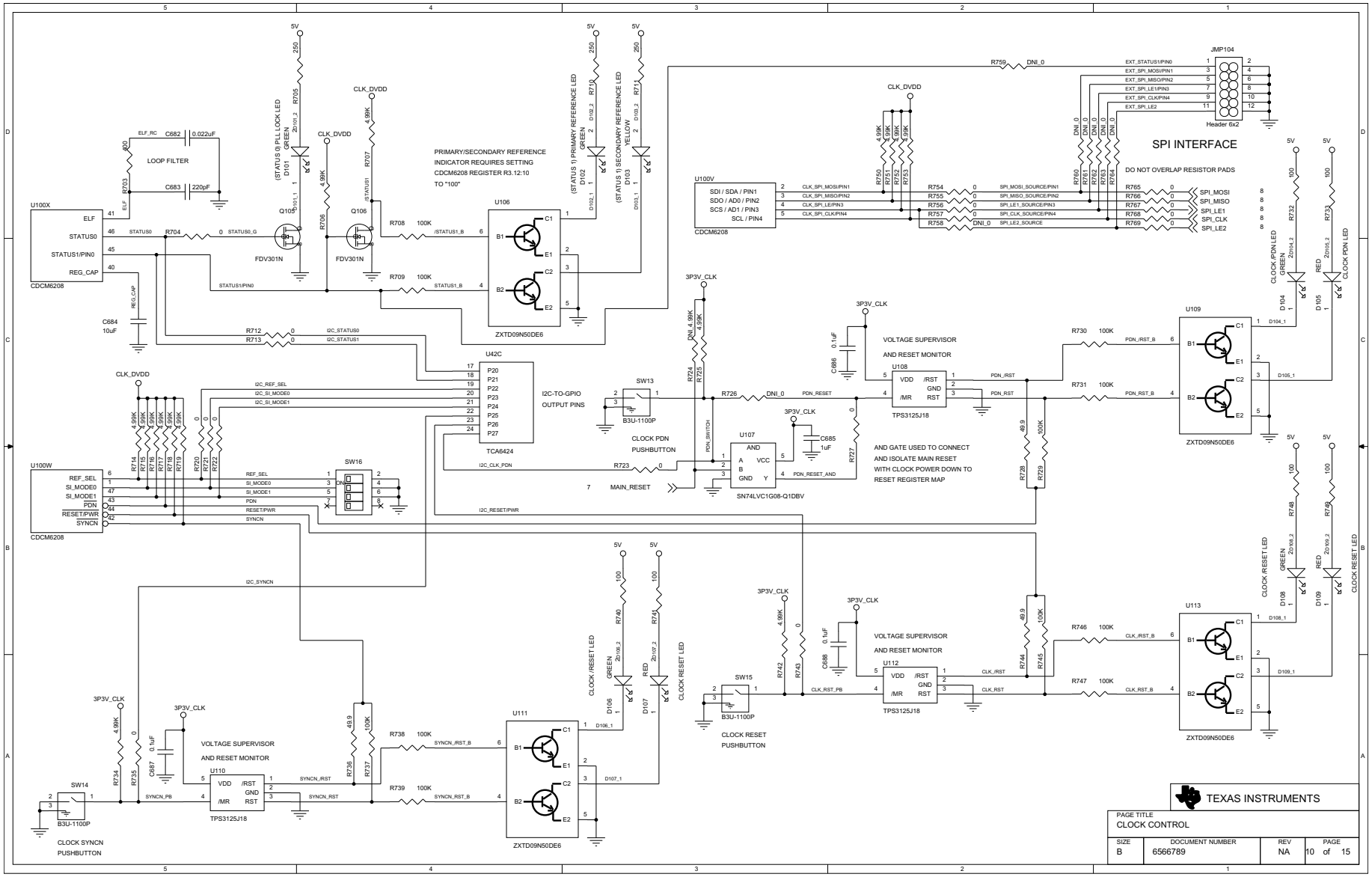

Figure 17. TLK10232 EVM Schematic, Sheet 10 Clock Control

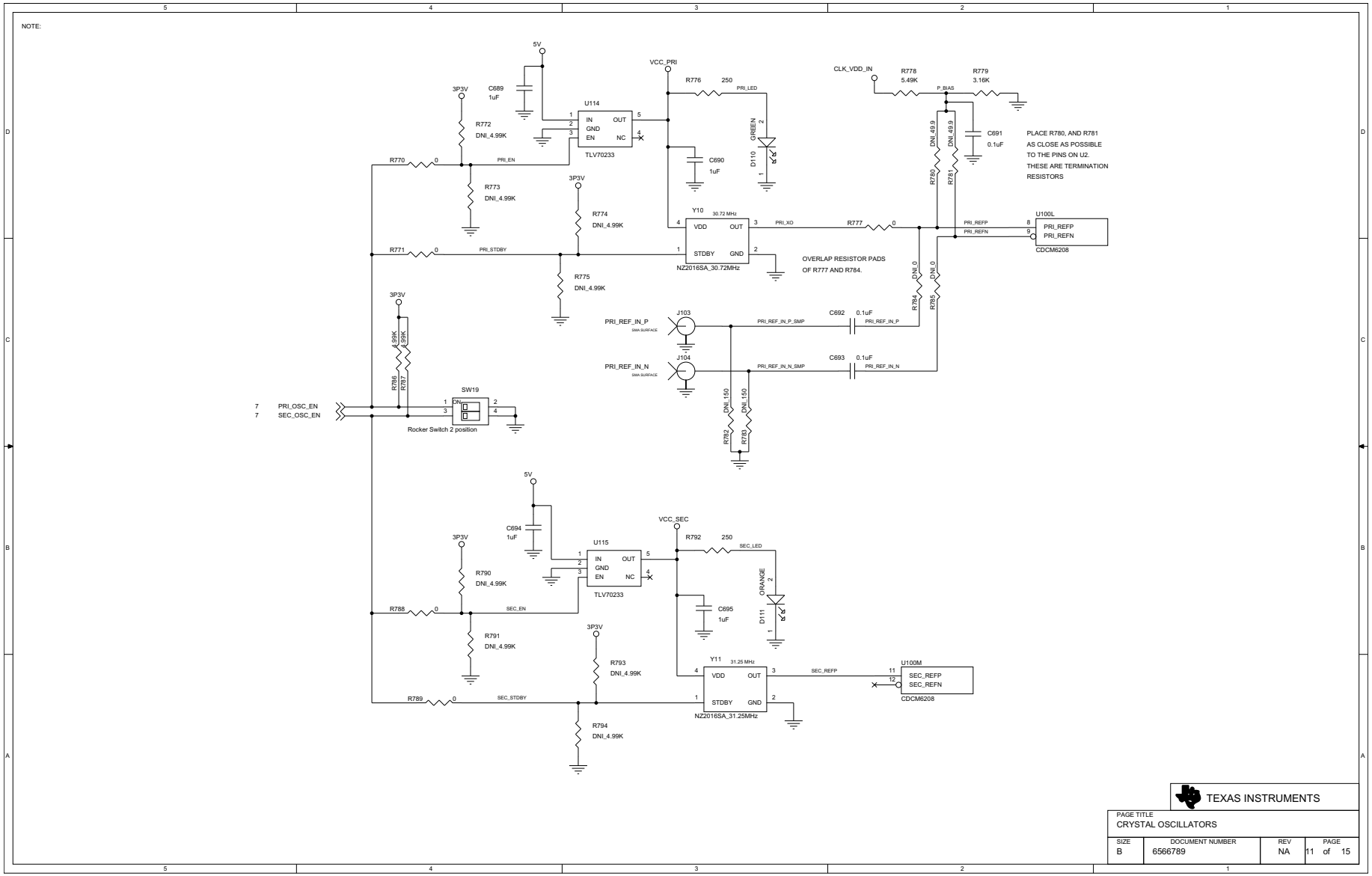

Figure 18. TLK10232 EVM Schematic, Sheet 11 Crystal Oscillators

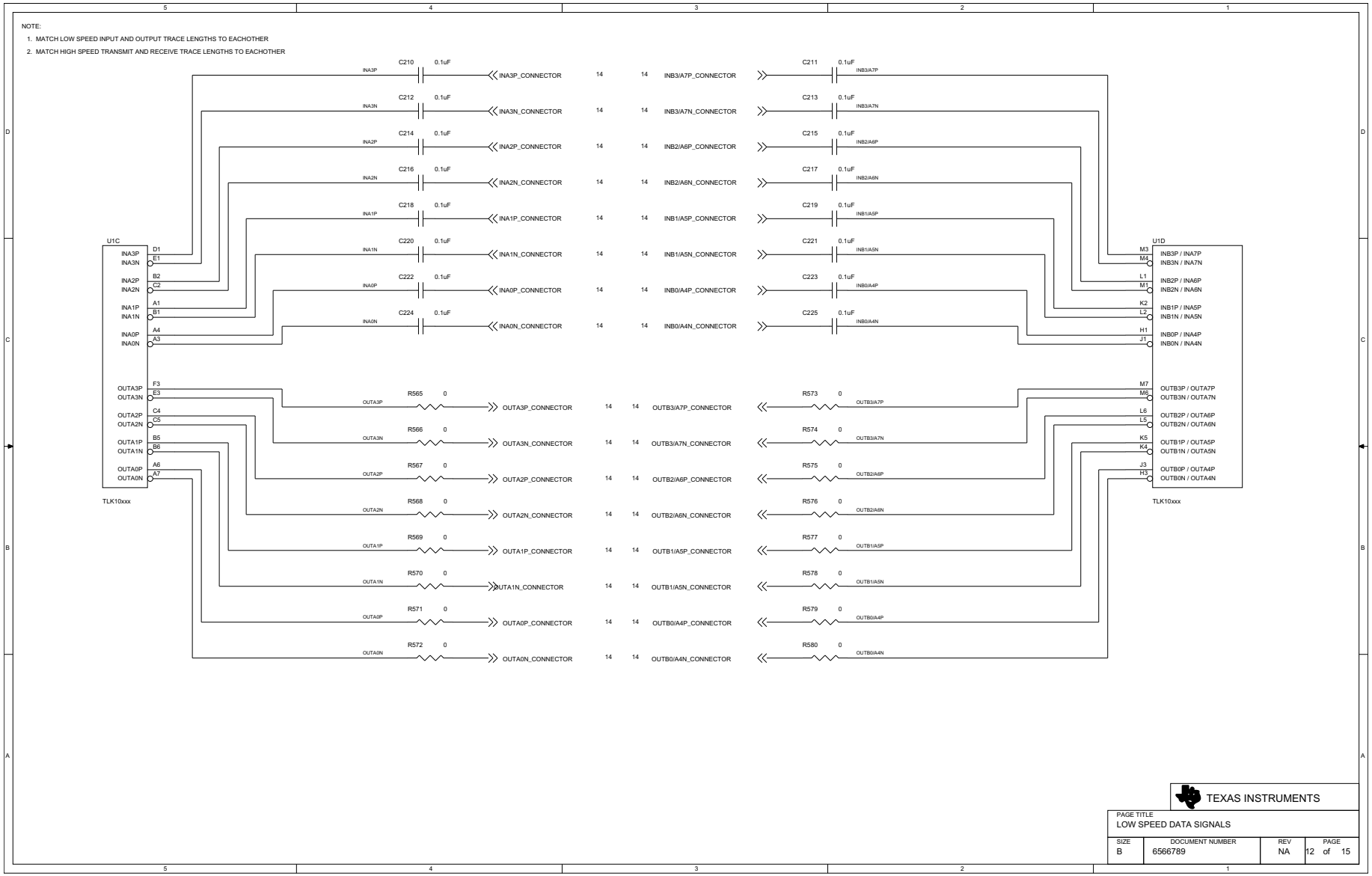

Figure 19. TLK10232 EVM Schematic, Sheet 12 Low-Speed Data Signals

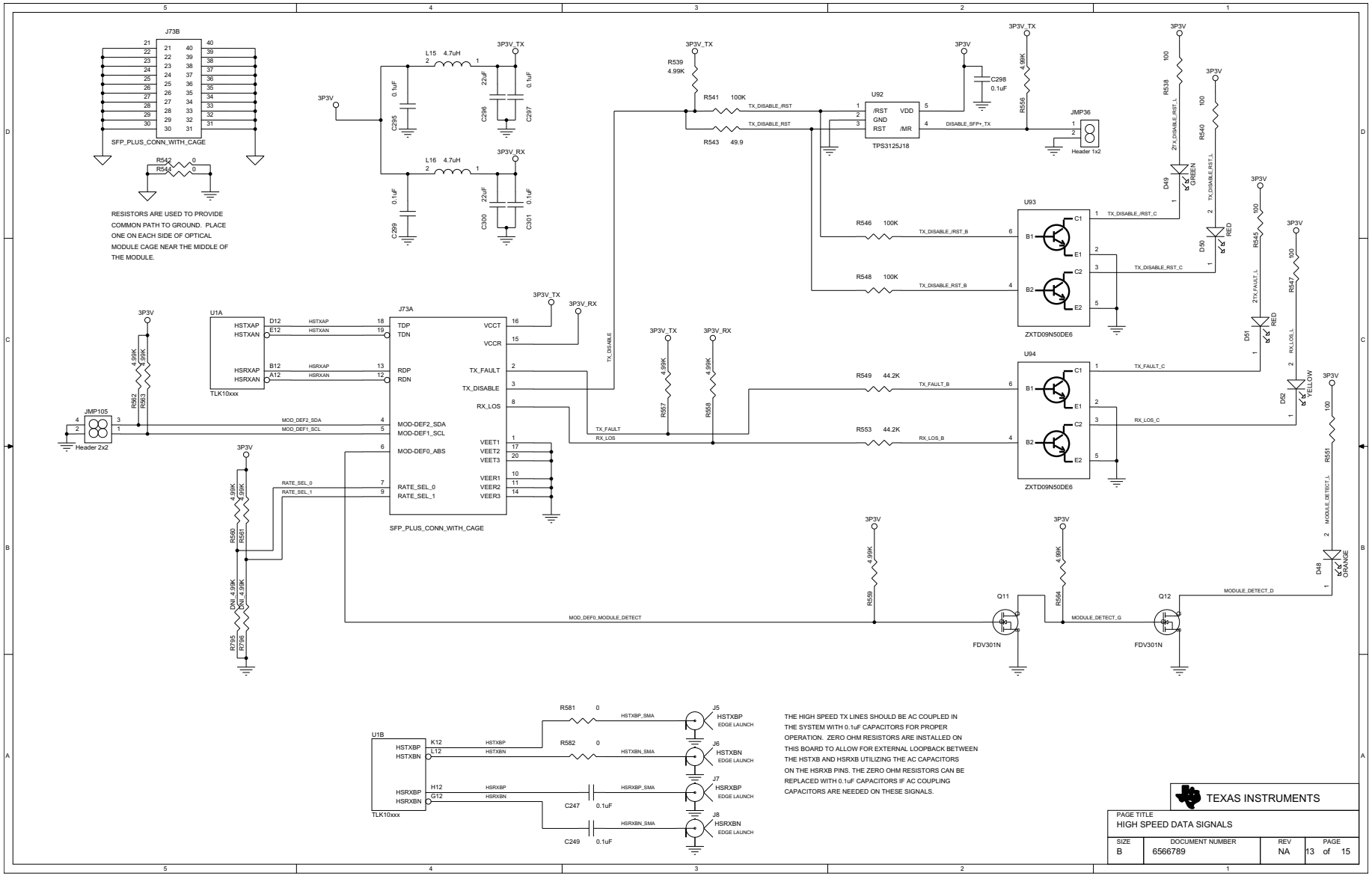

Figure 20. TLK10232 EVM Schematic, Sheet 13 High-Speed Data Signals

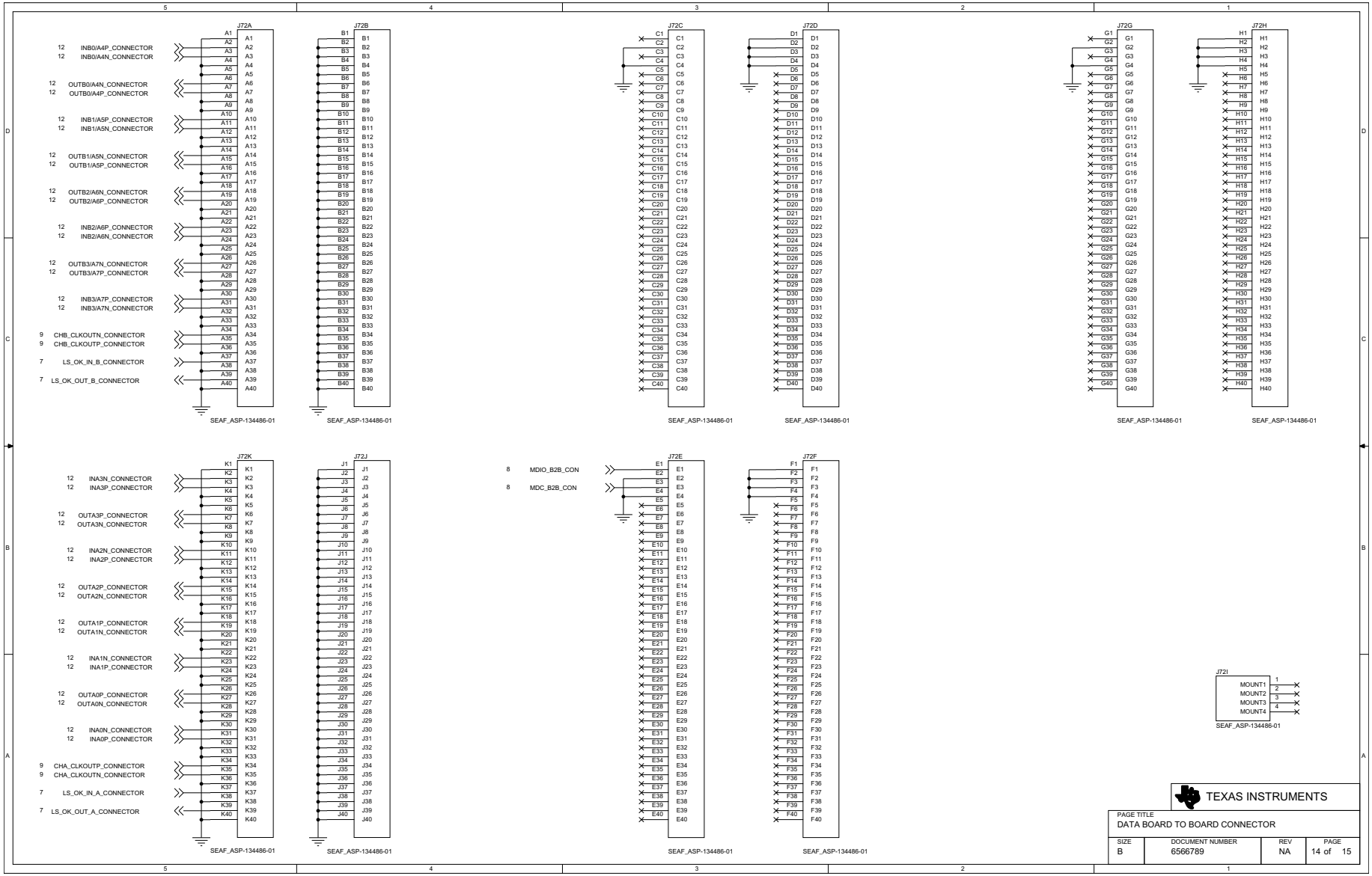

Figure 21. TLK10232 EVM Schematic, Sheet 14 Data Board to Board Connector

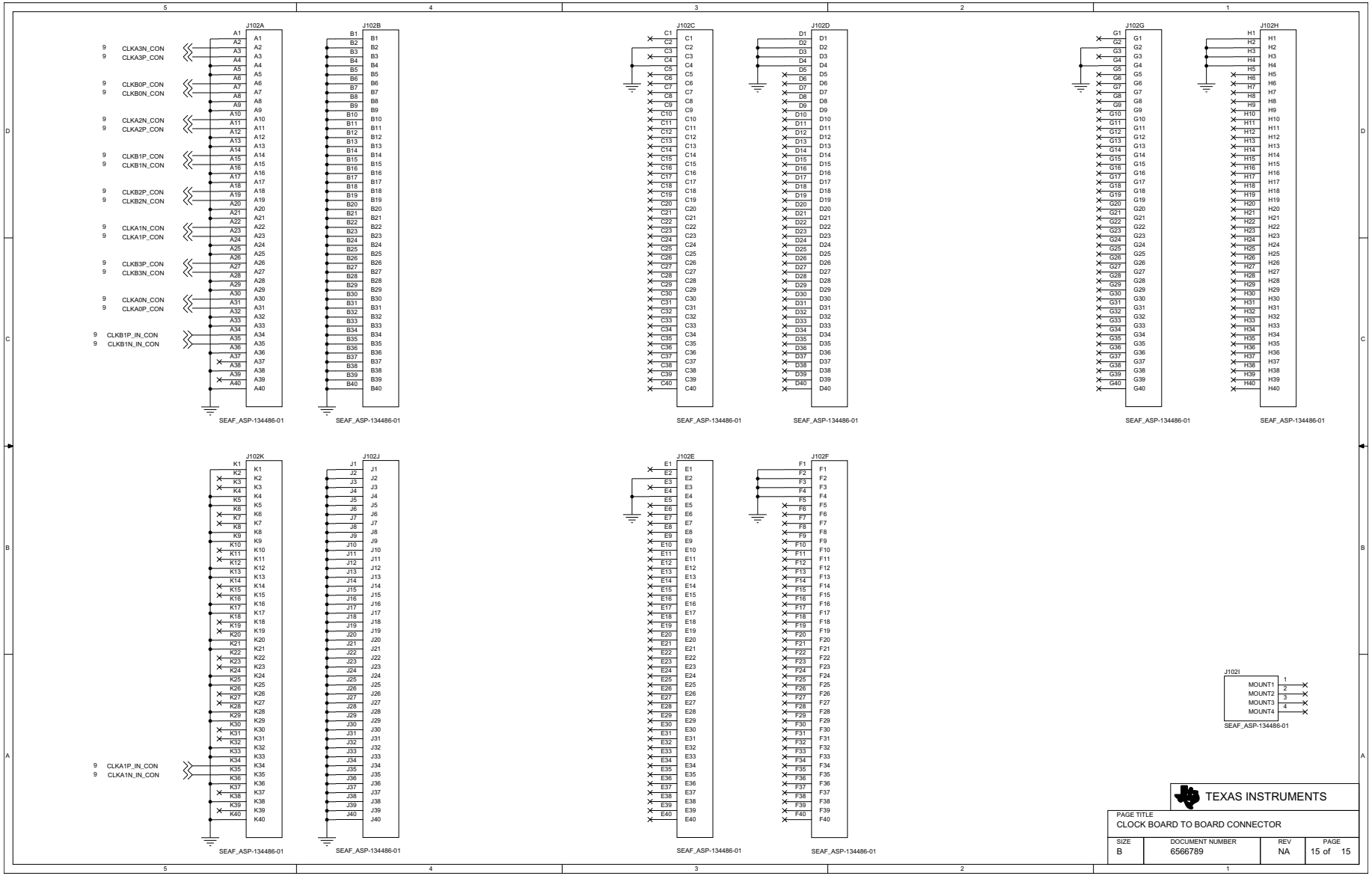

Figure 22. TLK10232 EVM Schematic, Sheet 15 Clock Board to Board Connector

12 TLK10232 EVM Motherboard Layout

Figure 23 through Figure 32 show the EVM motherboard layouts.

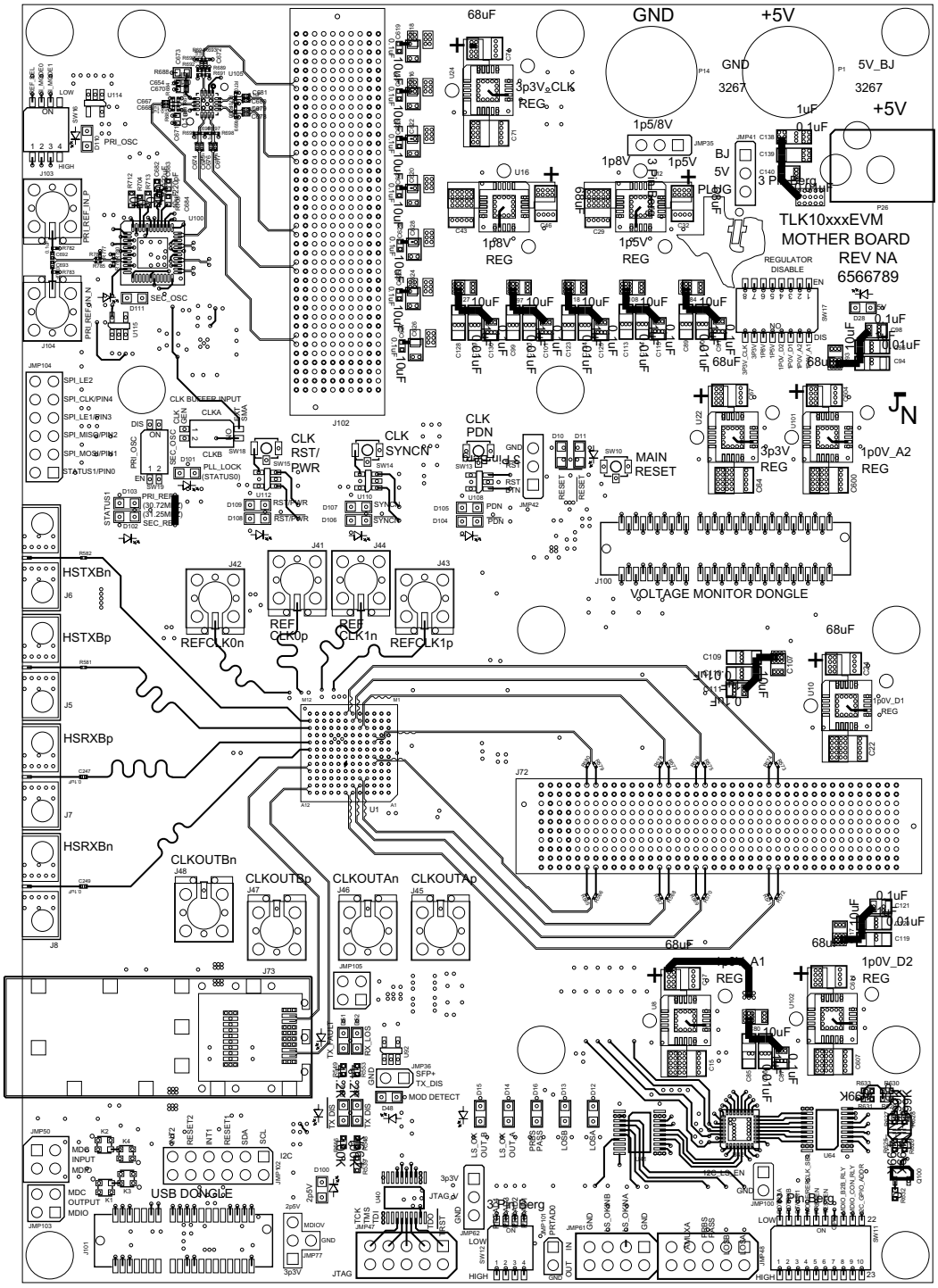

Figure 23. TLK10232 EVM Layout, Top Signal (Layer 1)

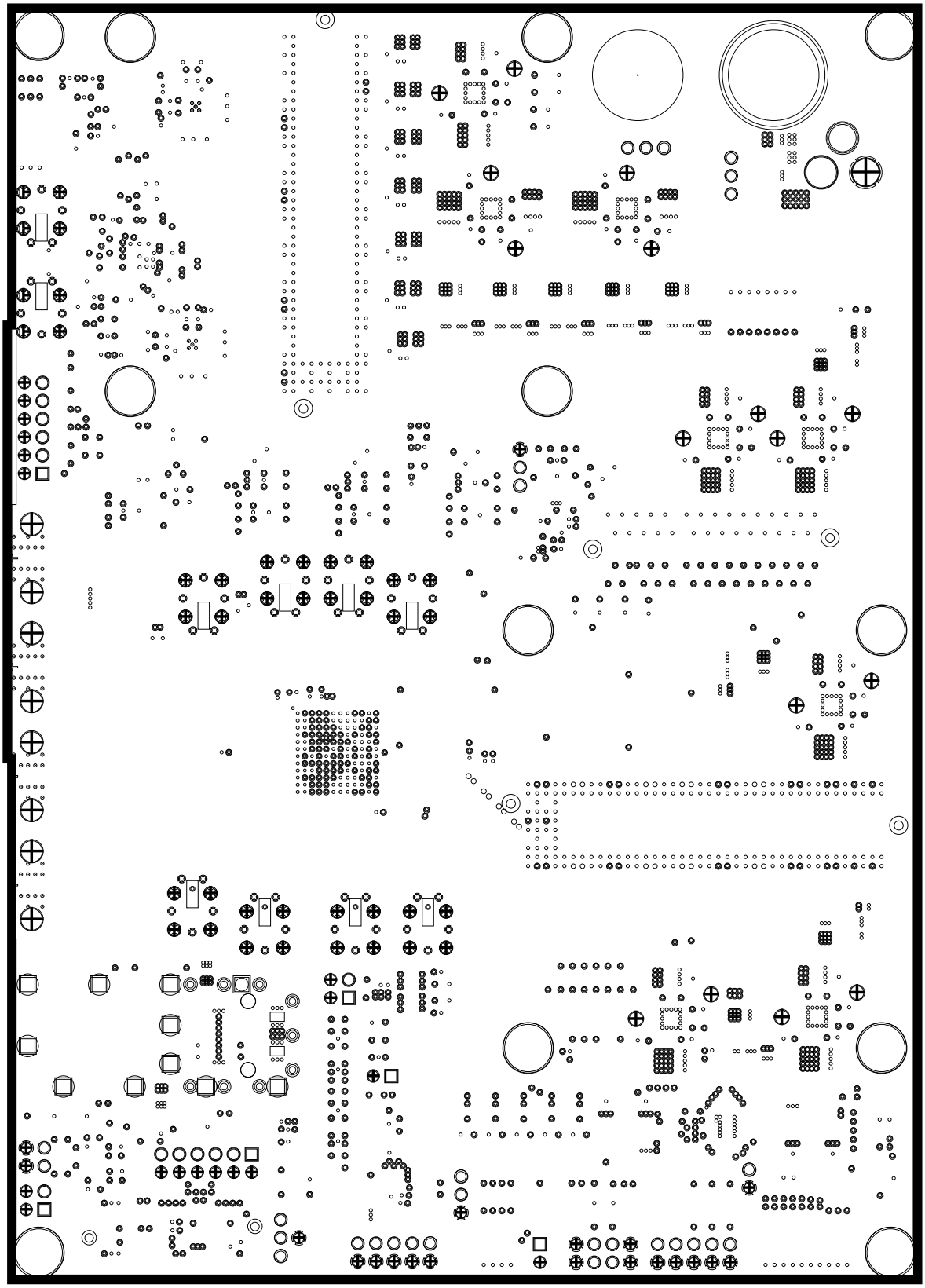

Figure 24. TLK10232 EVM Layout, Internal Ground (Layer 2)

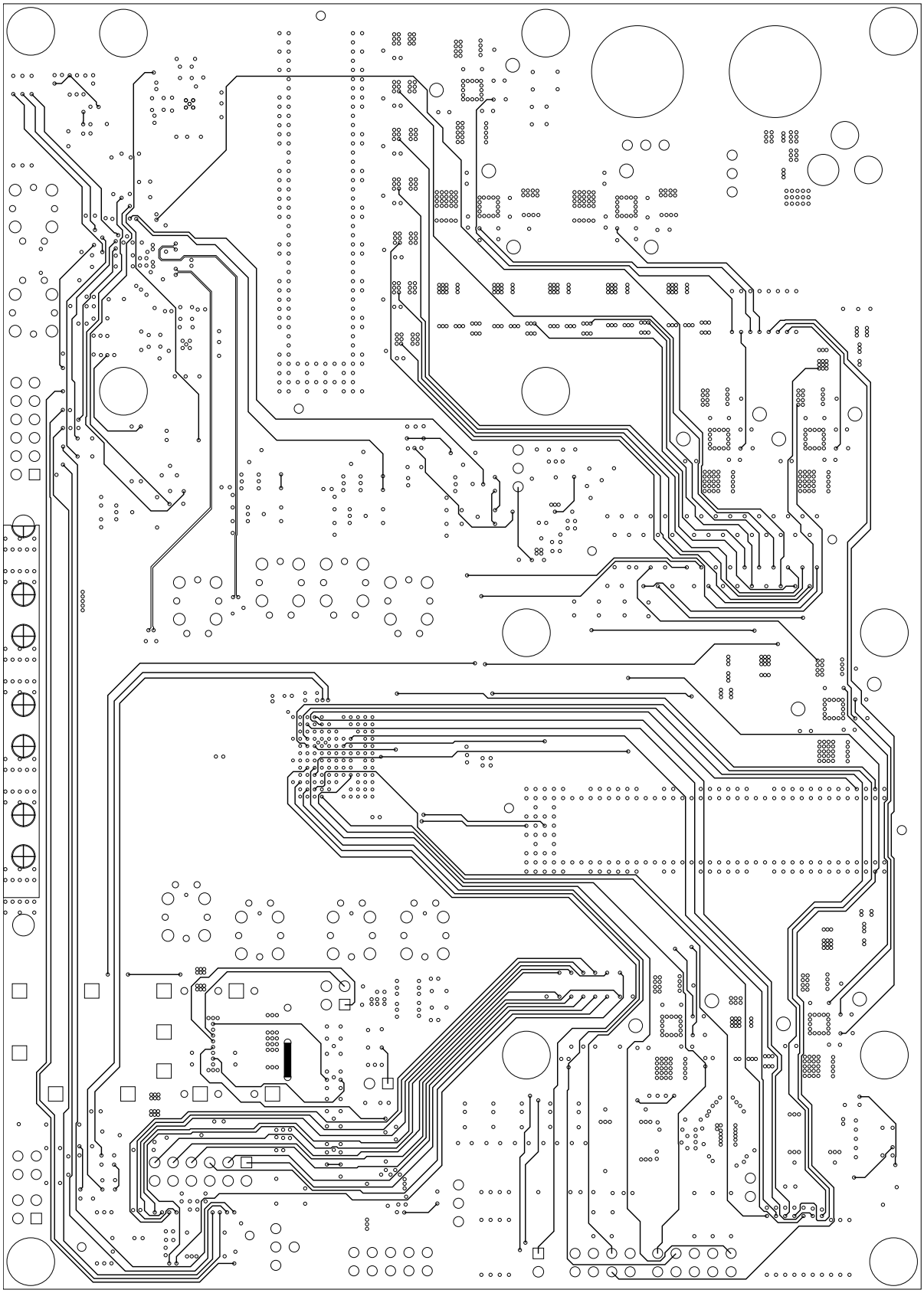

Figure 25. TLK10232 EVM Layout, Internal Signal (Layer 3)

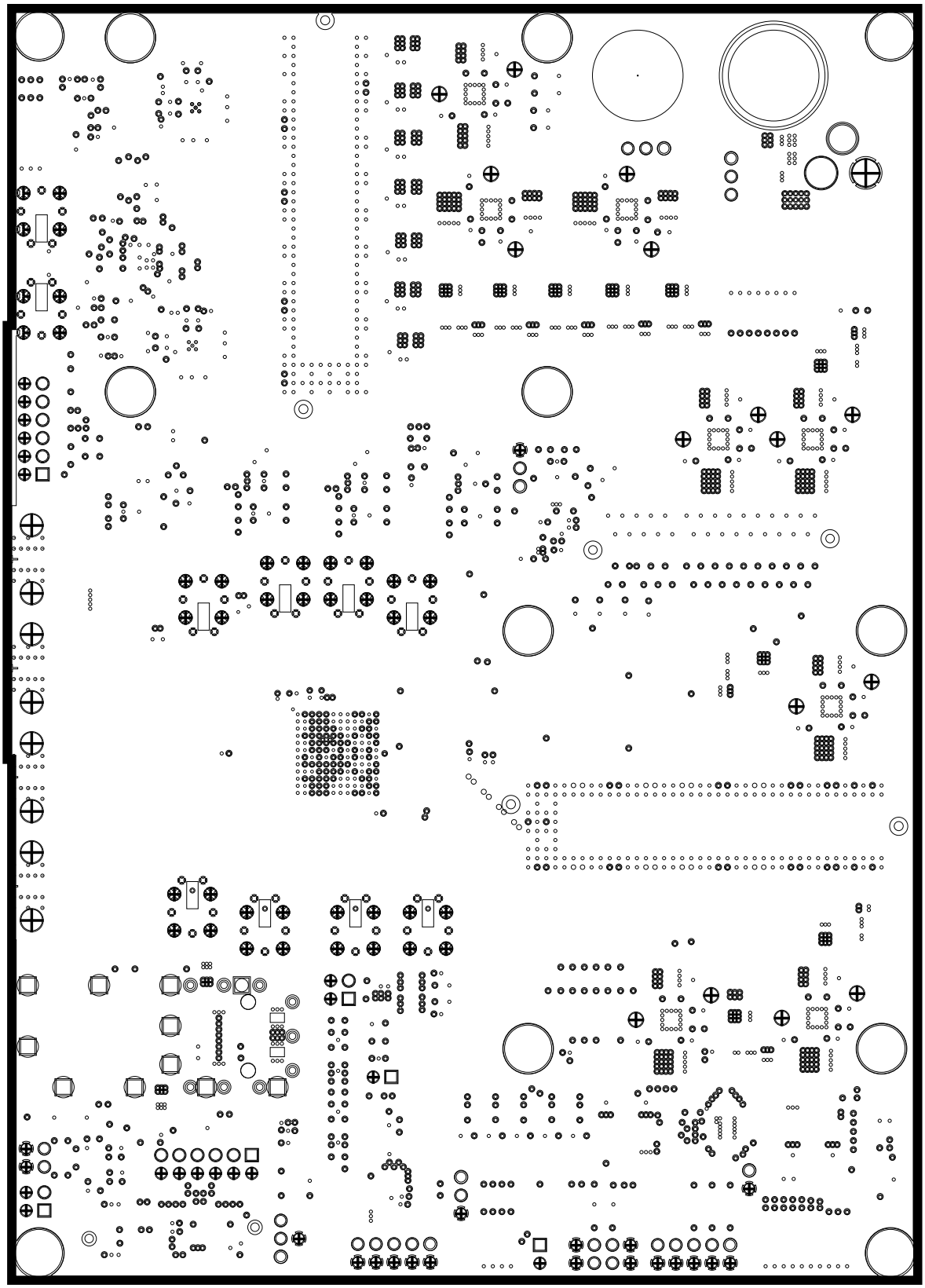

Figure 26. TLK10232 EVM Layout, Internal Ground (Layers 4, 6, 7, 9, 11, 13, 15)

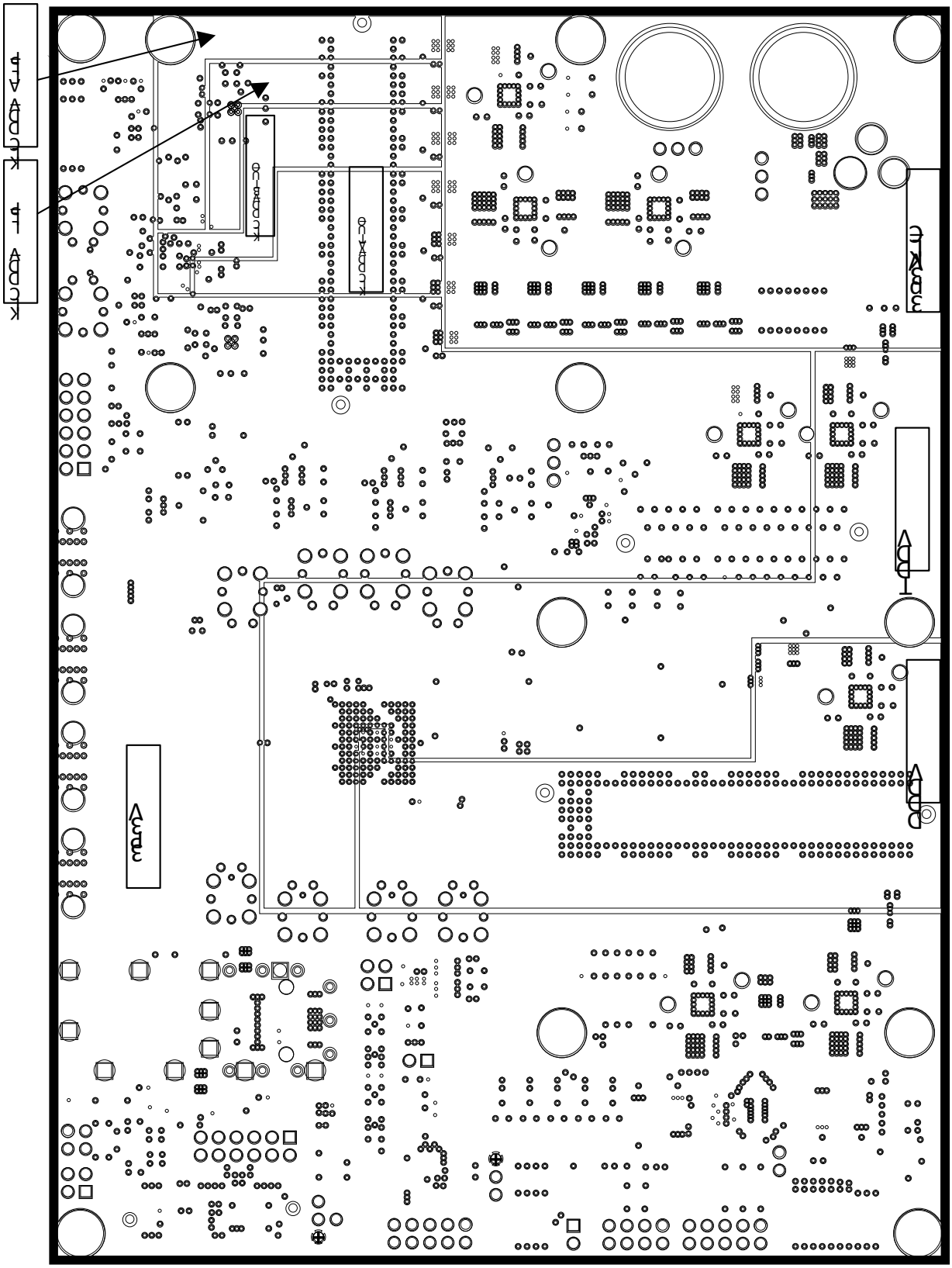

Figure 27. TLK10232 EVM Layout, Internal Power (Layer 5)

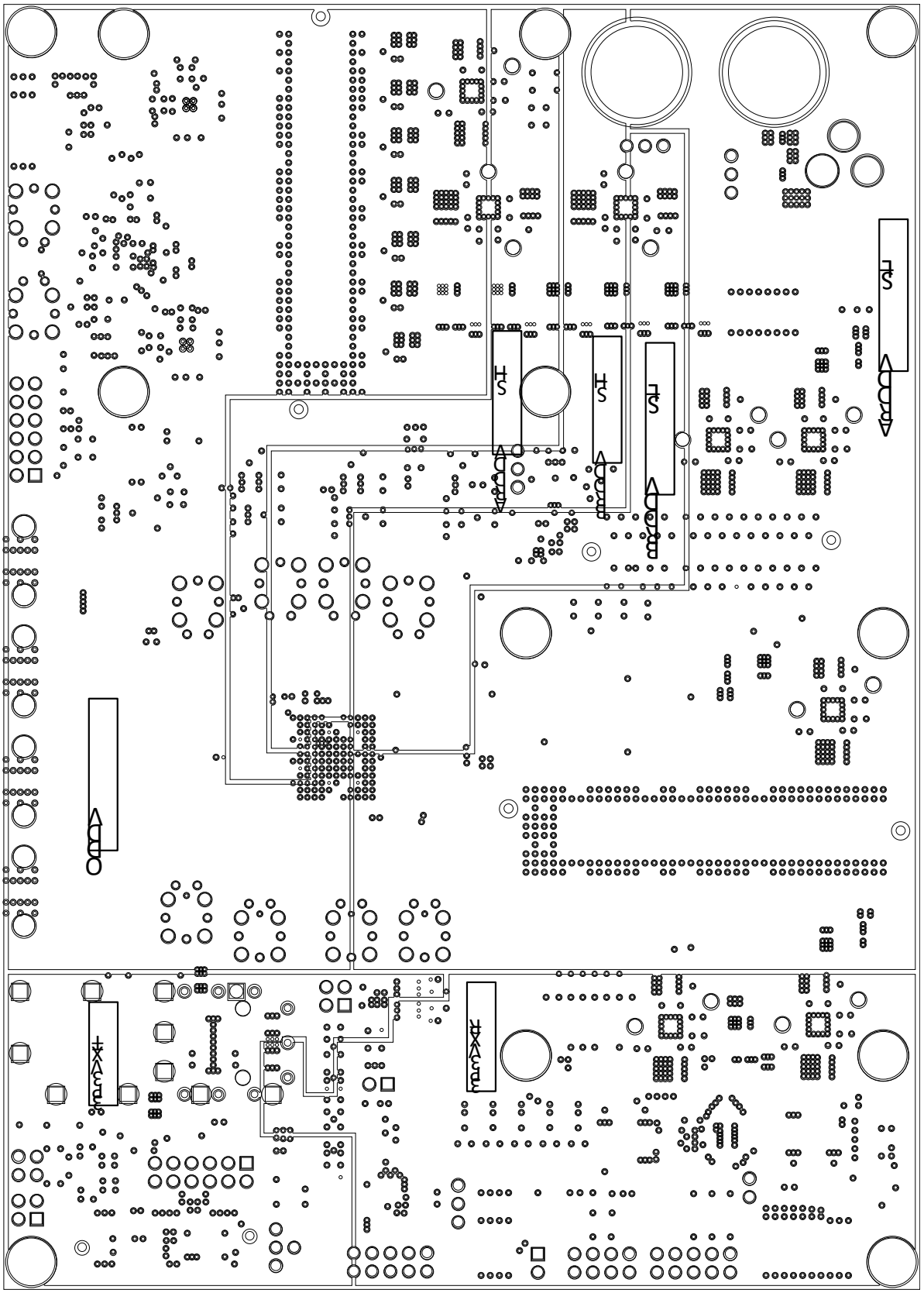

Figure 28. TLK034 EVM Layout, Internal 5-V Power (Layer 8)

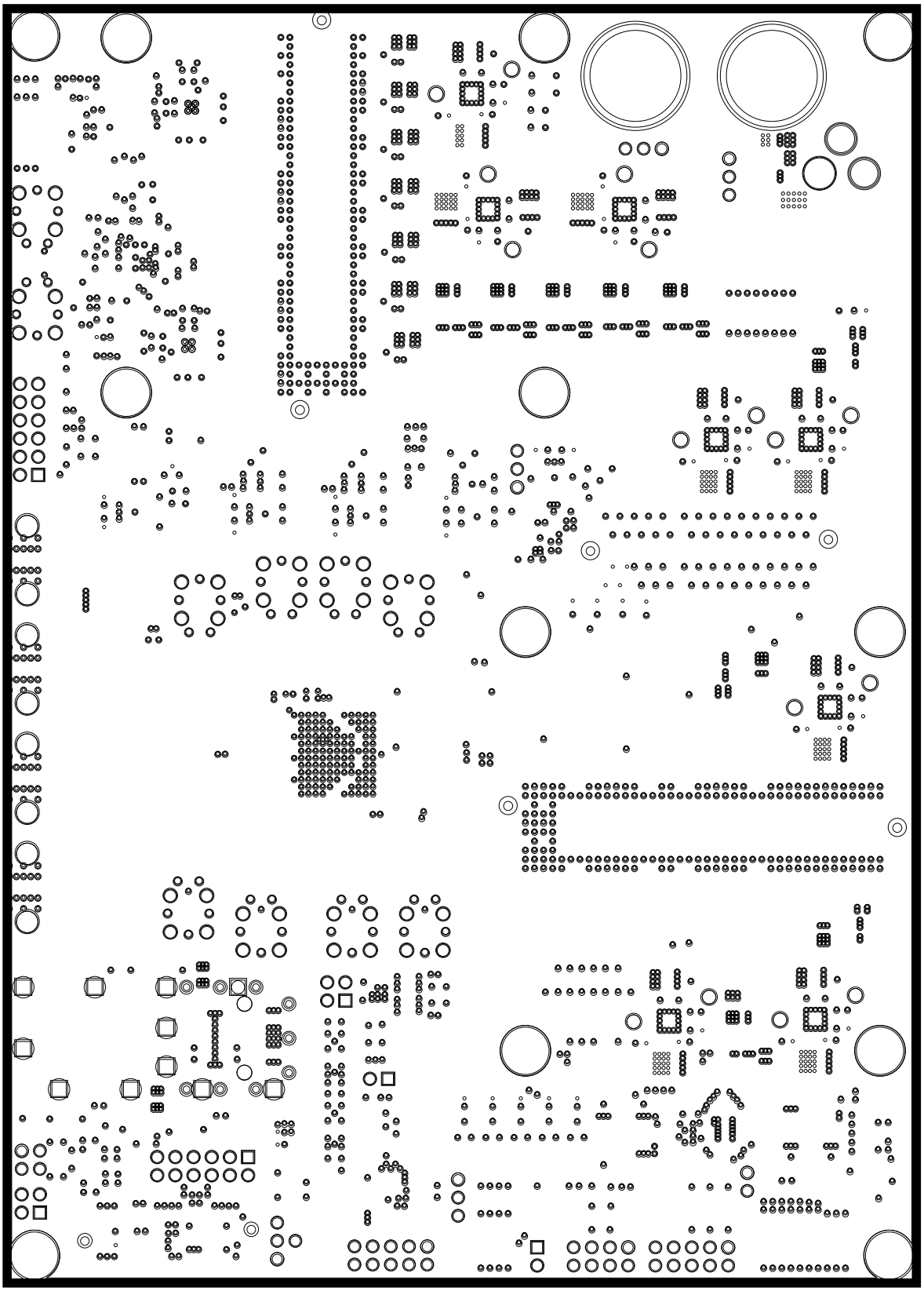

Figure 29. TLK10232 EVM Layout, Internal 5-V Power (Layer 10)

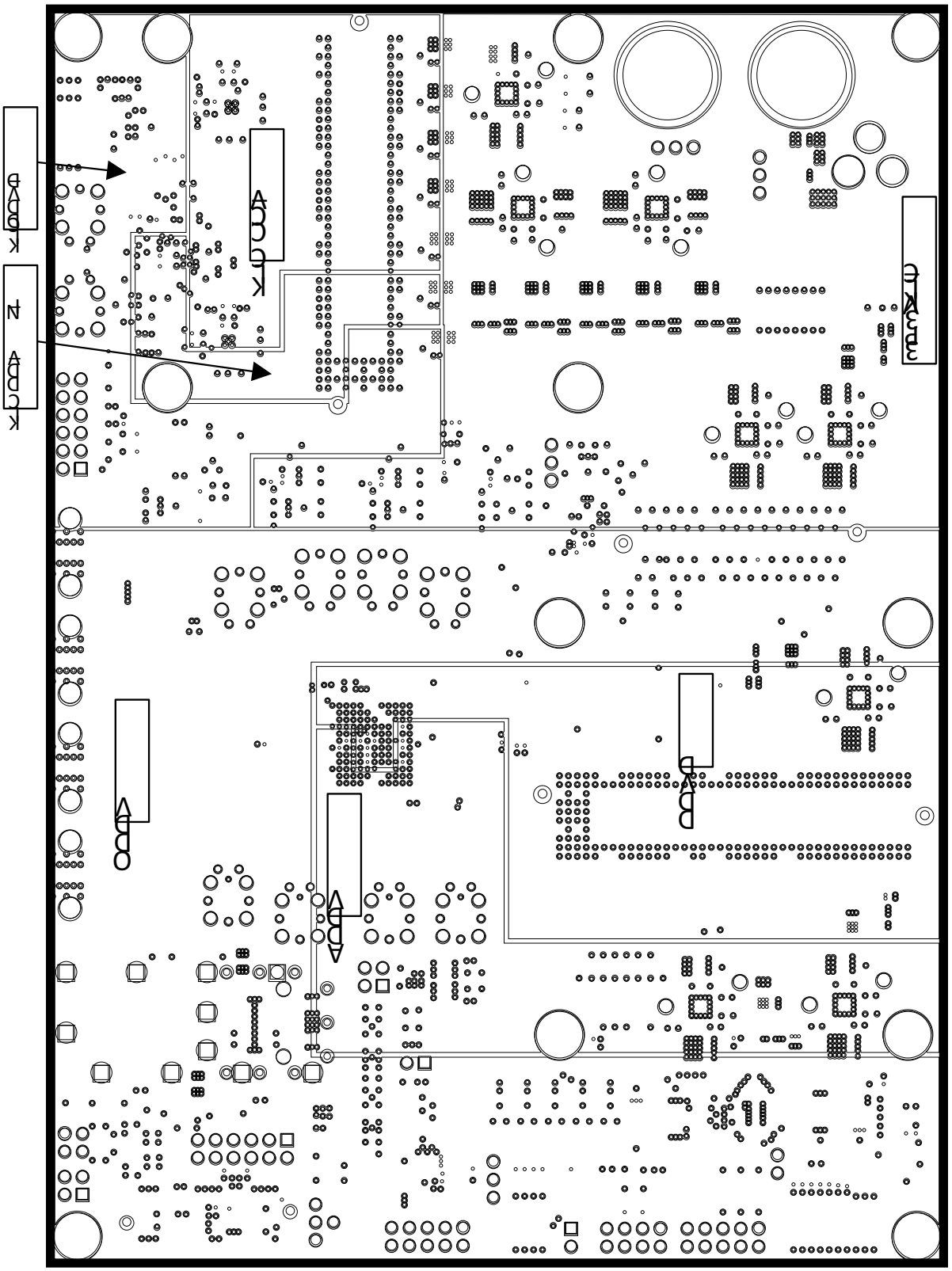

Figure 30. TLK10232 EVM Layout, Internal Power (Layer 12)

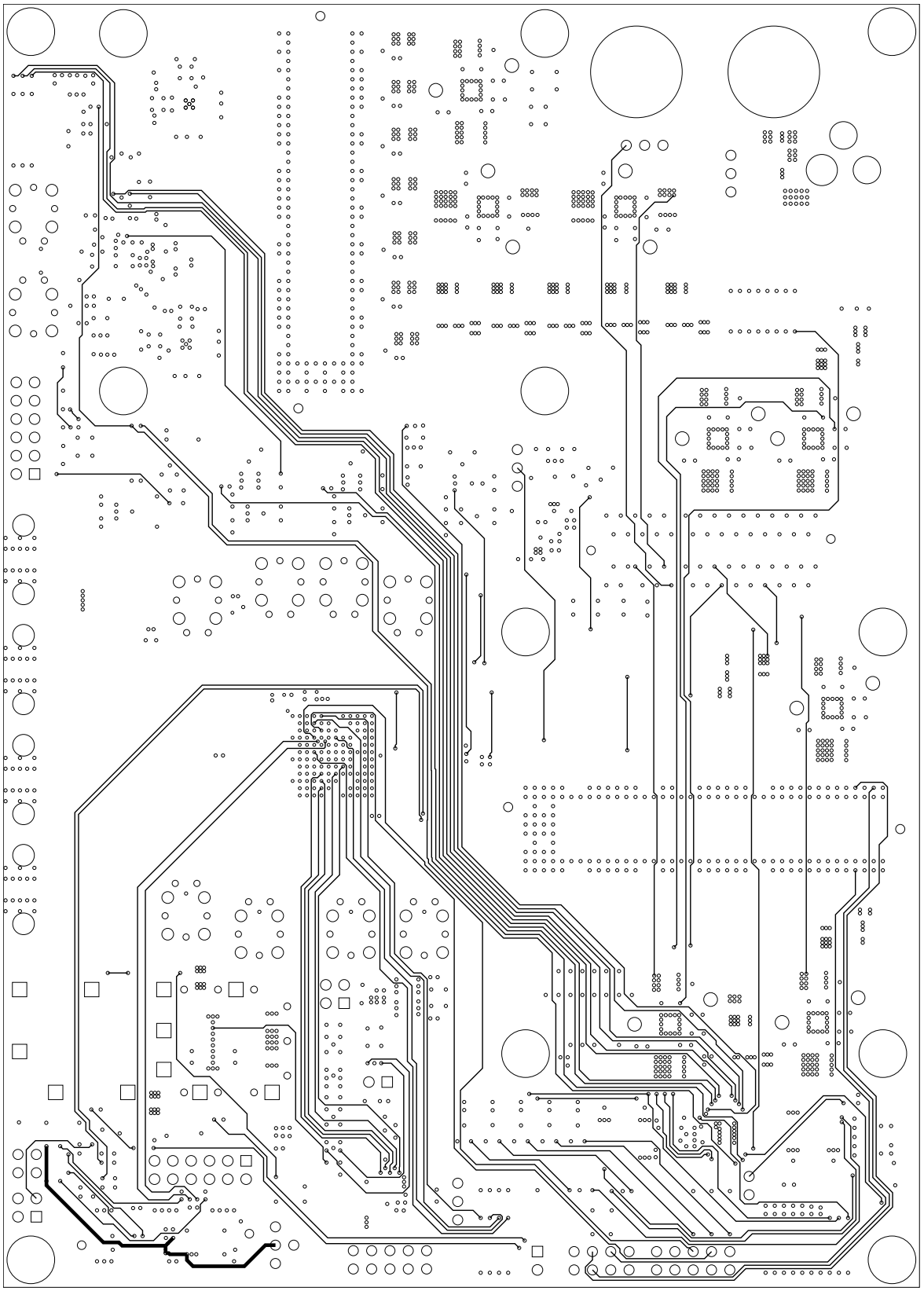

Figure 31. TLK10232 EVM Layout, Internal Signal (Layer 14)

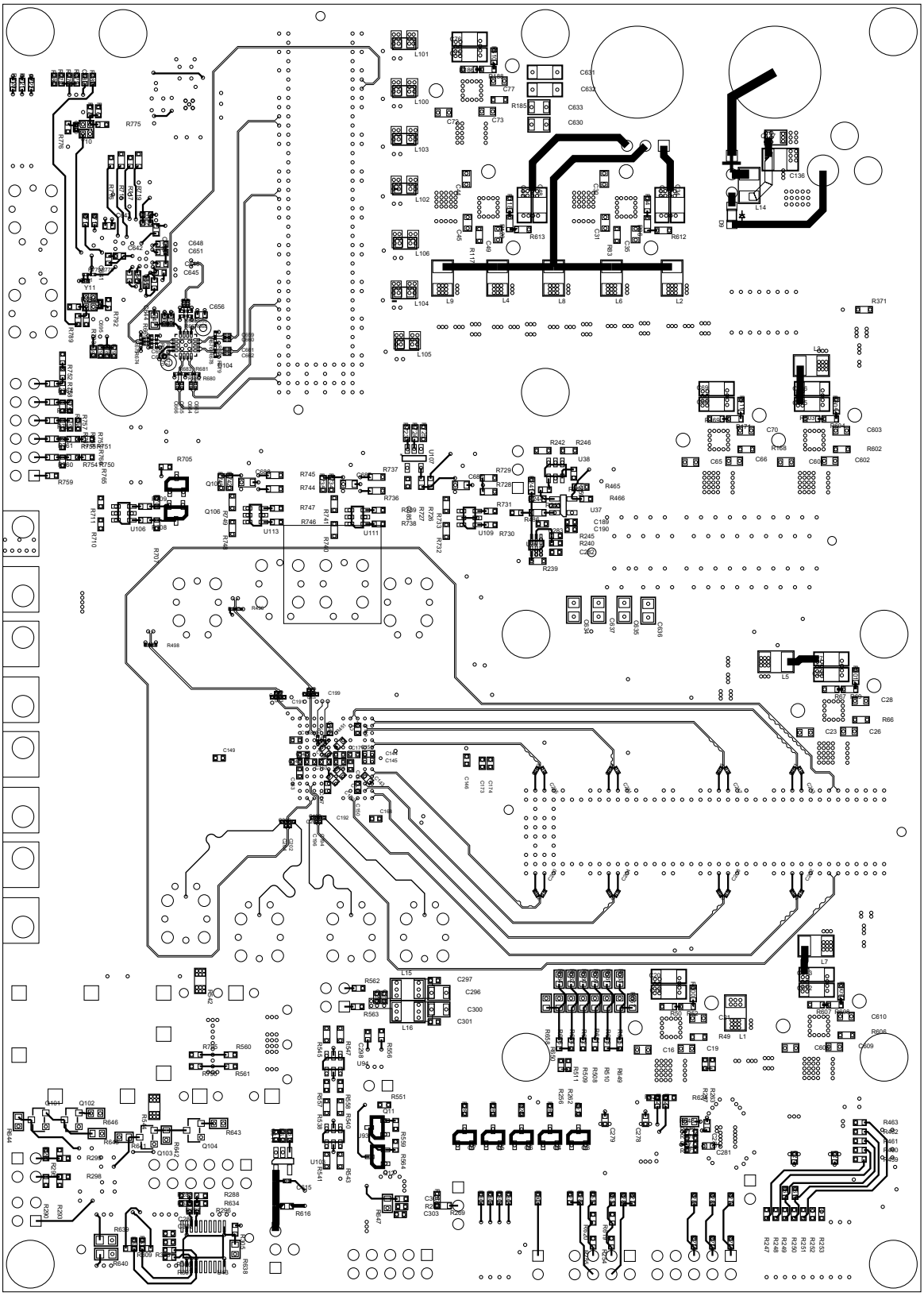

Figure 32. TLK10232 EVM Layout, Bottom Signal (Layer 16 Top View)

Table 1 contains the EVM motherboard layer construction.

Table 1. TLK10232 EVM Motherboard Layer Construction

Subclass Name	Type	Material	Thickness (MIL)	Dielectric Constant	Width (MIL)	Coupling Type / Spacing (MIL)
	SURFACE	AIR		1		
TOP	CONDUCTOR	COPPER	1.9	2.8	4.5 (Diff) 10.0 (Single)	Edge / 4.0 (Diff) None/None (Single)
	DIELECTRIC	Rogers	5	3.6		
L2_GND	PLANE	COPPER	1.2	1		
	DIELECTRIC	FR-4	5	4.1		
L3_SIG2	CONDUCTOR	COPPER	1.2	1	6.0 (Single)	None/None (Single)
	DIELECTRIC	FR-4	10	4.1		
L4_GND	PLANE	COPPER	1.2	1		
	DIELECTRIC	FR-4	5	4.1		
L5_PWR	CONDUCTOR	COPPER	1.2	1		
	DIELECTRIC	FR-4	5	4.1		
L6_GND	PLANE	COPPER	1.2	1		
	DIELECTRIC	FR-4	5	4.5		
L7_GND	PLANE	COPPER	1.2	4.5		
	DIELECTRIC	FR-4	5	4.5		
L8_PWR	PLANE	COPPER	1.2	4.5		
	DIELECTRIC	FR-4	5	4.5		
L9_GND	PLANE	COPPER	1.2	4.5		
	DIELECTRIC	FR-4	5	4.1		
L10_PWR	CONDUCTOR	COPPER	1.2	4.5		
	DIELECTRIC	FR-4	5	4.5		
L11_GND	PLANE	COPPER	1.2	1		
	DIELECTRIC	FR-4	5	4.1		
L12_PWR	CONDUCTOR	COPPER	1.2	1		
	DIELECTRIC	FR-4	5	4.1		
L13_GND	PLANE	COPPER	1.2	1		
	DIELECTRIC	FR-4	10	4.1		
L14_SIG3	CONDUCTOR	COPPER	1.2	1	6.0 (Single)	None/None (Single)
	DIELECTRIC	FR-4	5	4.1		
L15_GND	PLANE	COPPER	1.2	1		
	DIELECTRIC	Rogers	5	3.6		
BOTTOM	CONDUCTOR	COPPER	1.9	1	4.5 (Diff) 10.0 (Single)	Edge / 4.0 (Diff) None/None (Single)
	SURFACE	AIR		1		

Note: The impedance is set to be slightly less than 50 Ω or 100 Ω on the traces in order to compensate for slight over-etching during the manufacturing process. The end impedance after etching should result in a 50- or 100-Ω impedance. Always consult with your board manufacturer for their process and design requirements to ensure the desired impedance is achieved.

13 TLK10232 EVM SMA Breakout Board Schematics

Figure 33 through Figure 36 show the EVM SMA breakout board schematics.

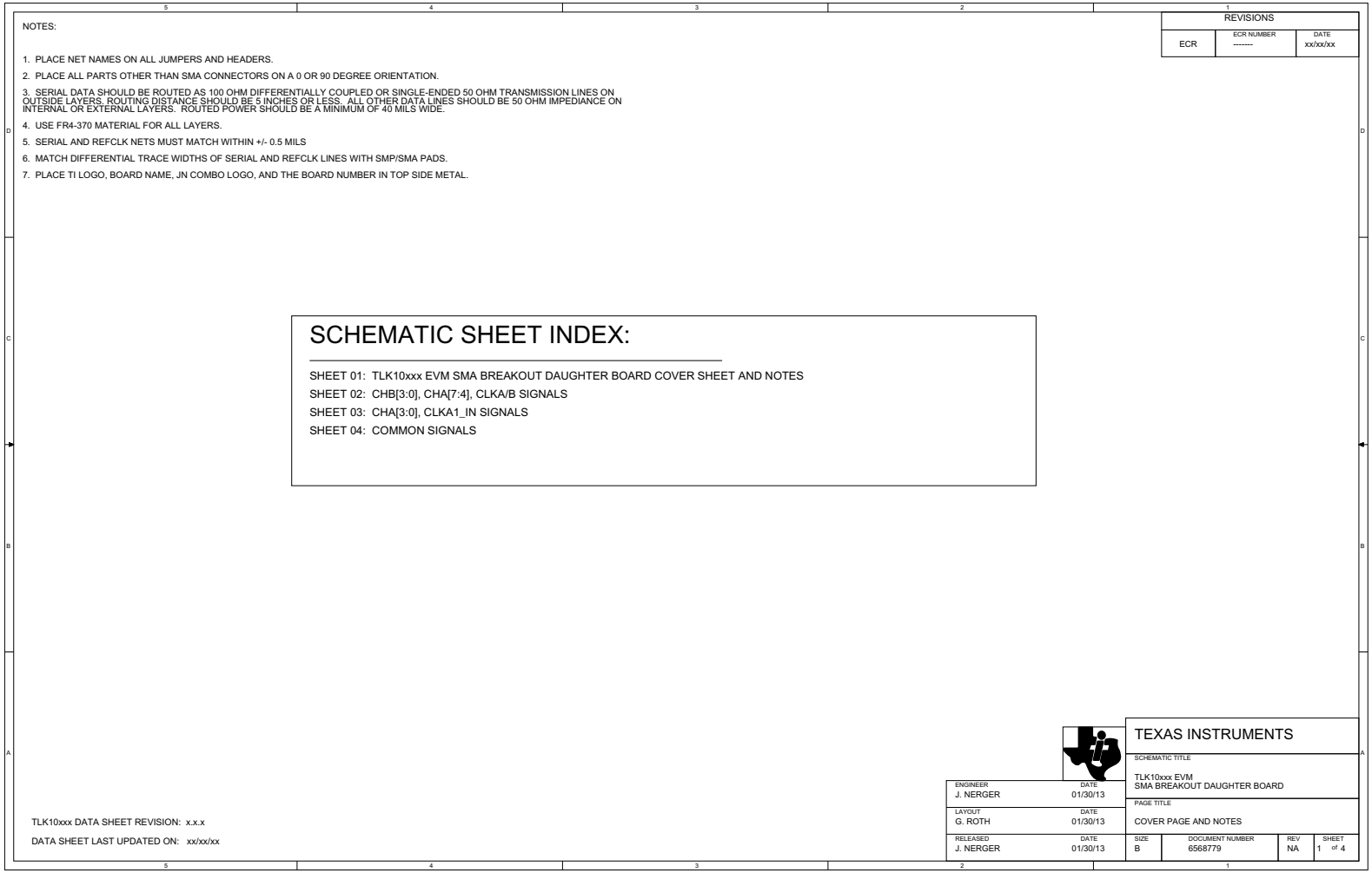

Figure 33. TLK10232 EVM SMA Breakout Board Schematic, Sheet 1 Cover Page and Index

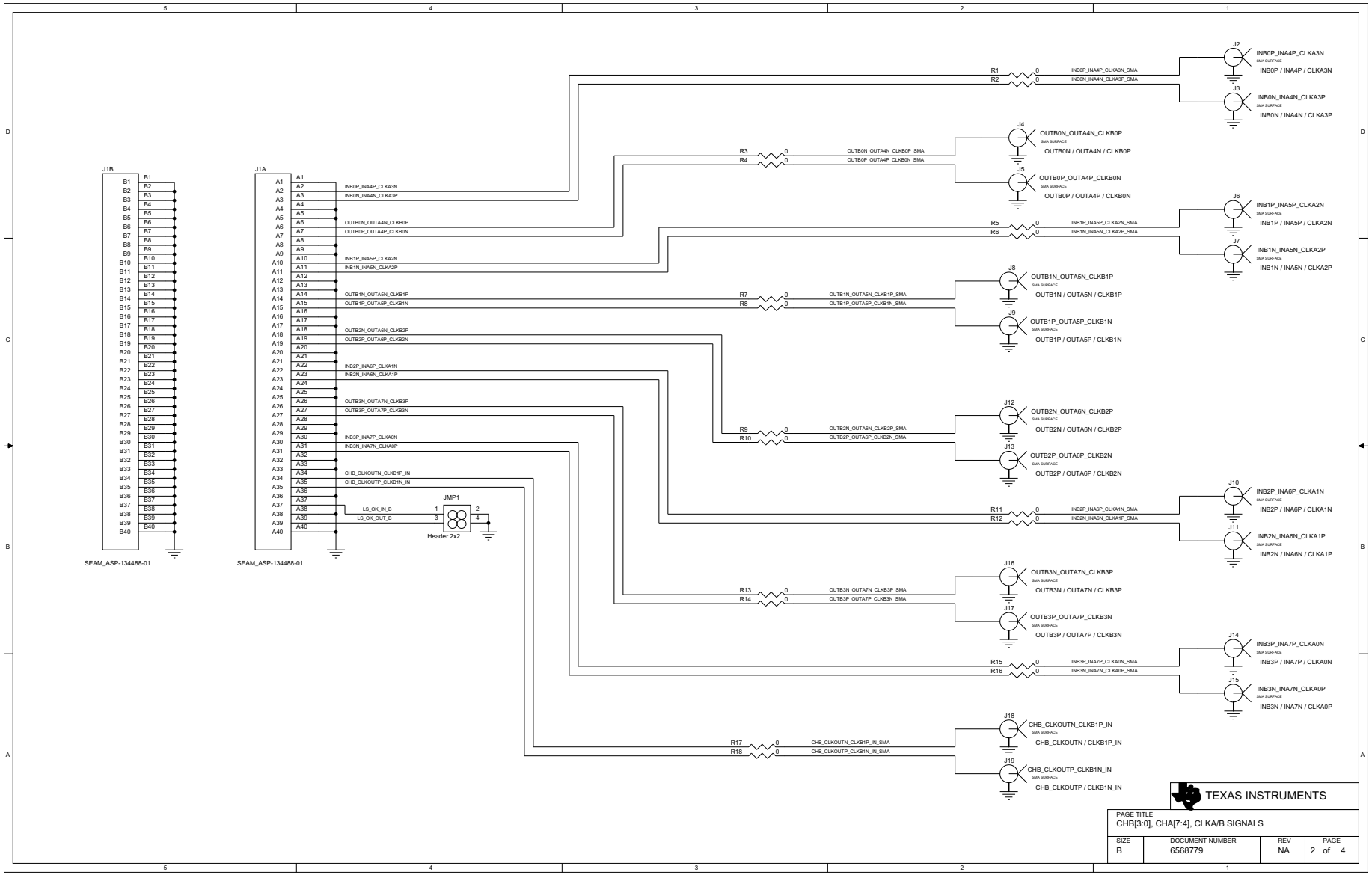

Figure 34. TLK10232 EVM SMA Breakout Board Schematic, Sheet 2 Channel B and CLKA/B Signals

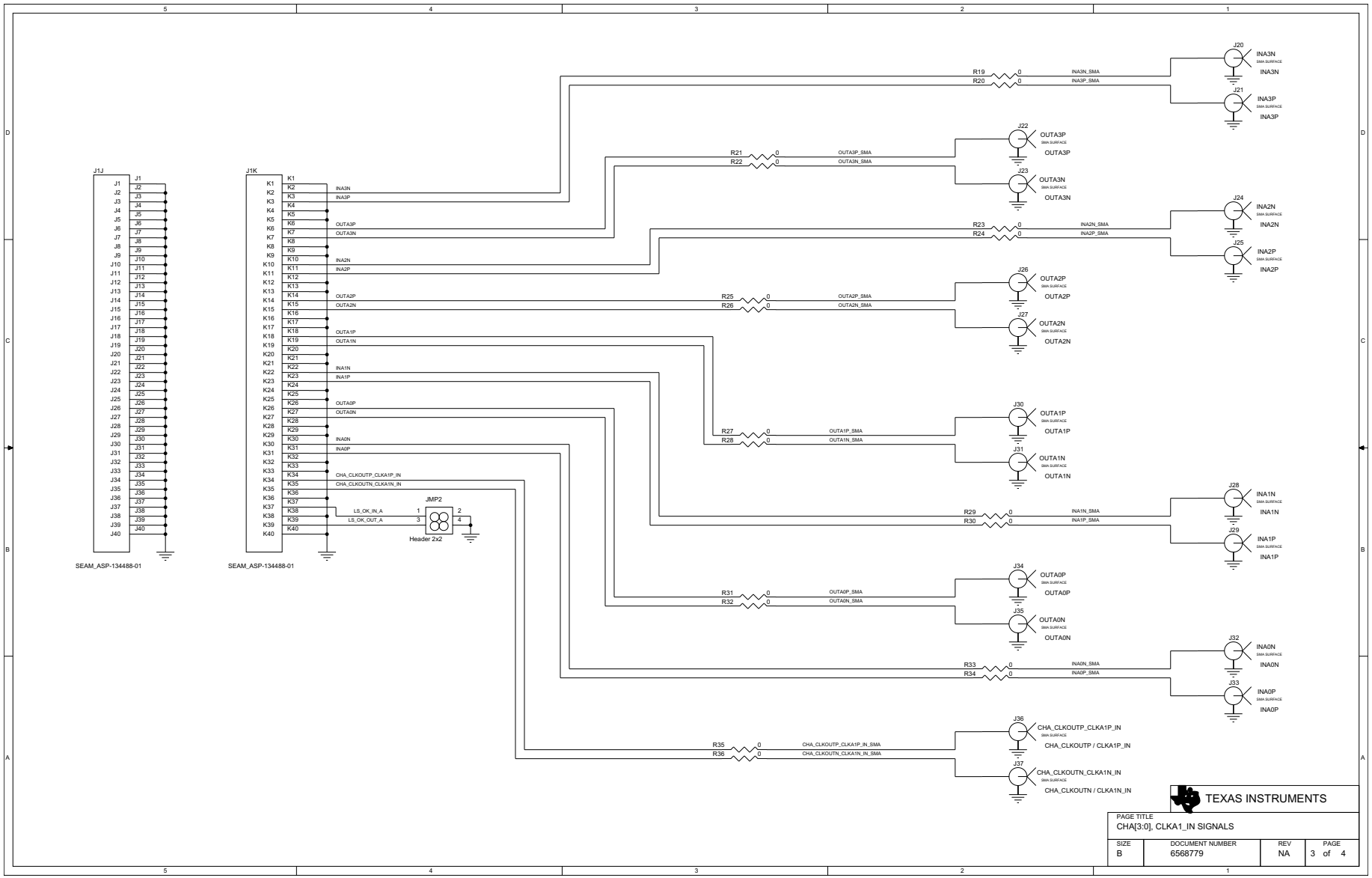

Figure 35. TLK10232 EVM SMA Breakout Board Schematic, Sheet 3 Channel A and CLKA1_IN Signals

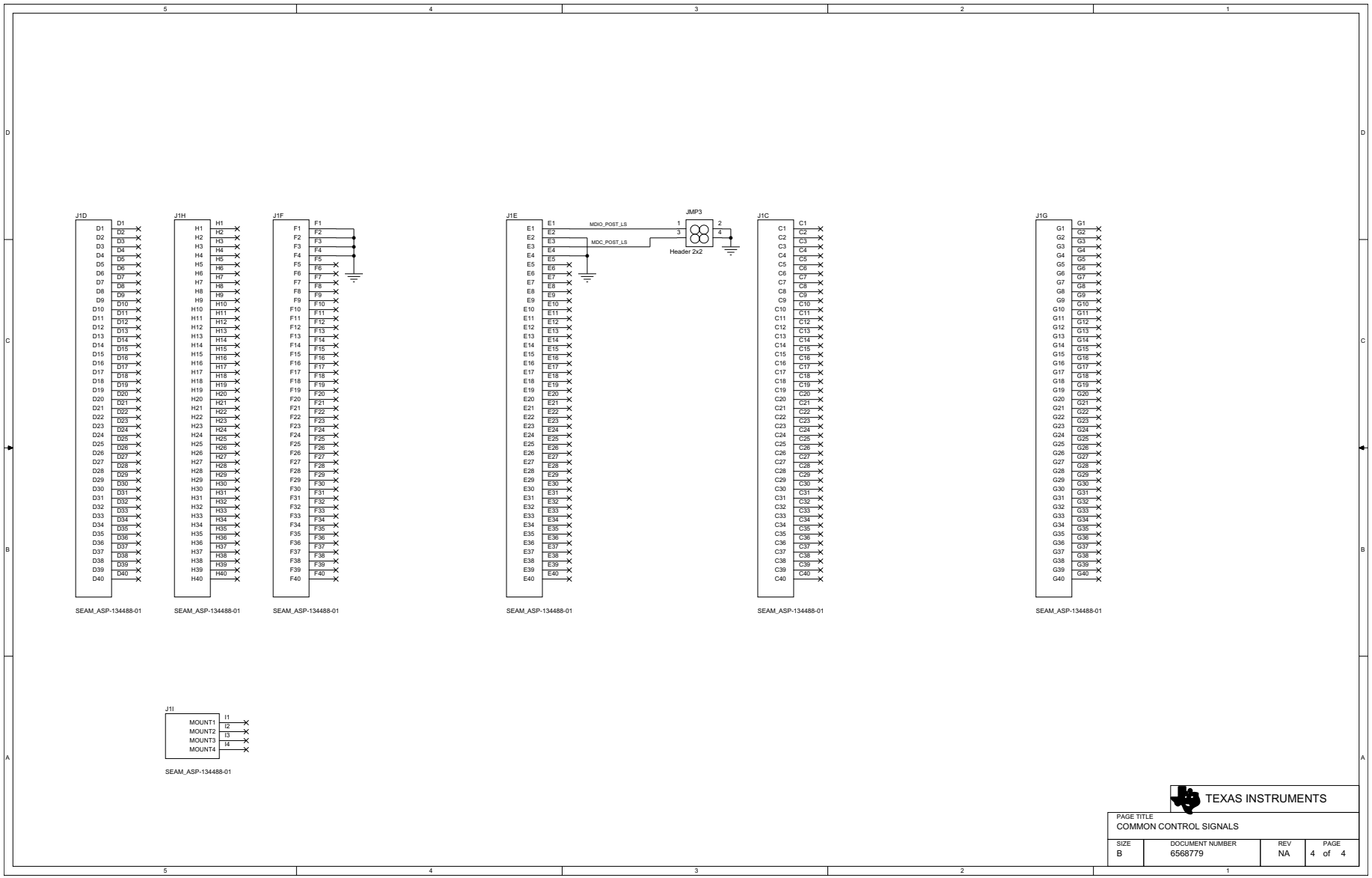

Figure 36. TLK10232 EVM SMA Breakout Board Schematic, Sheet 4 Common Control Signals

14 TLK10232 EVM SMA Breakout Board Layout

Figure 37 through Figure 40 show the EVM SMA breakout board layouts.

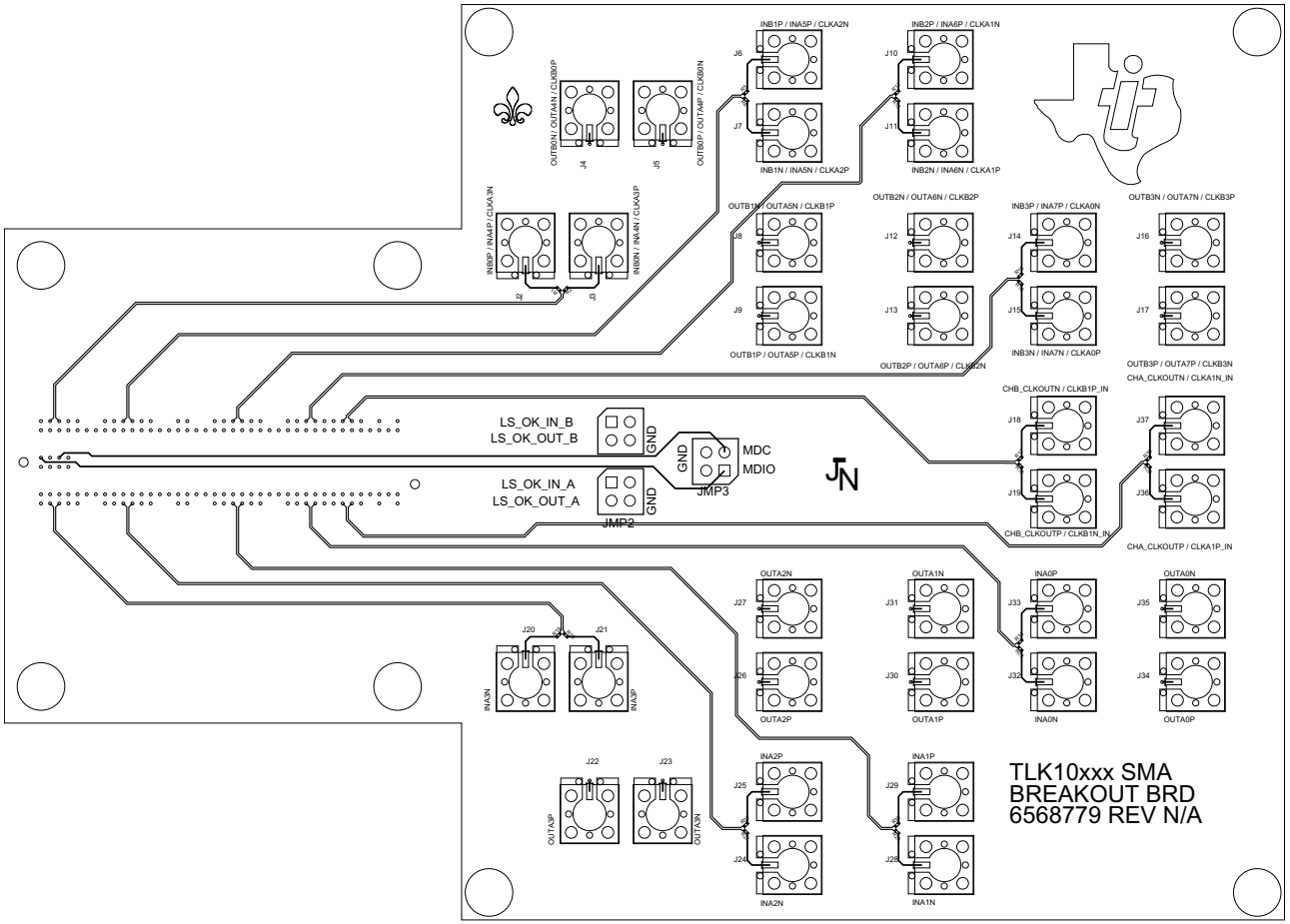

Figure 37. TLK10232 EVM SMA Breakout Board Layout, Top Signal (Layer 1)

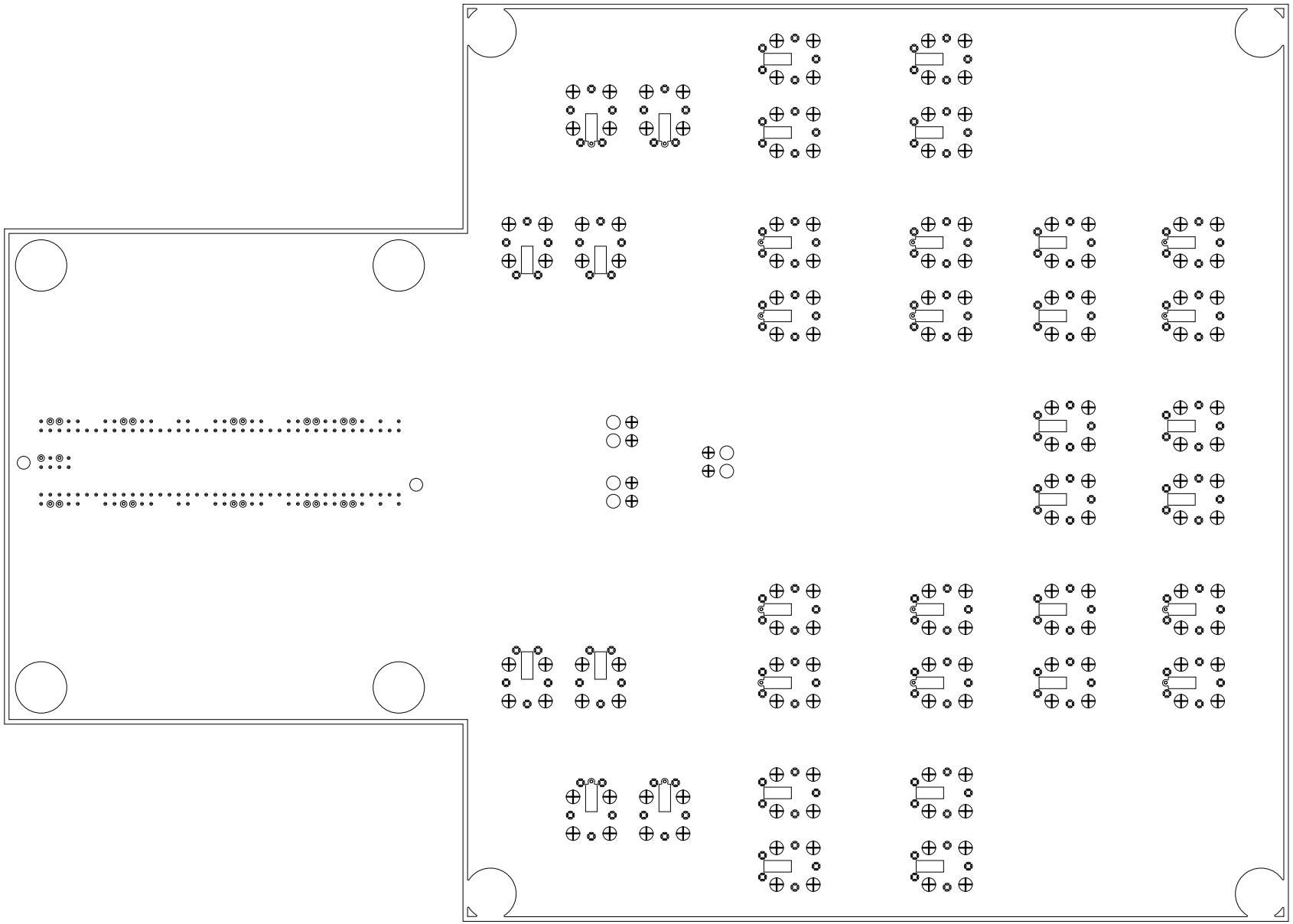

Figure 38. TLK10232 EVM SMA Breakout Board Layout, Internal Ground (Layer 2)

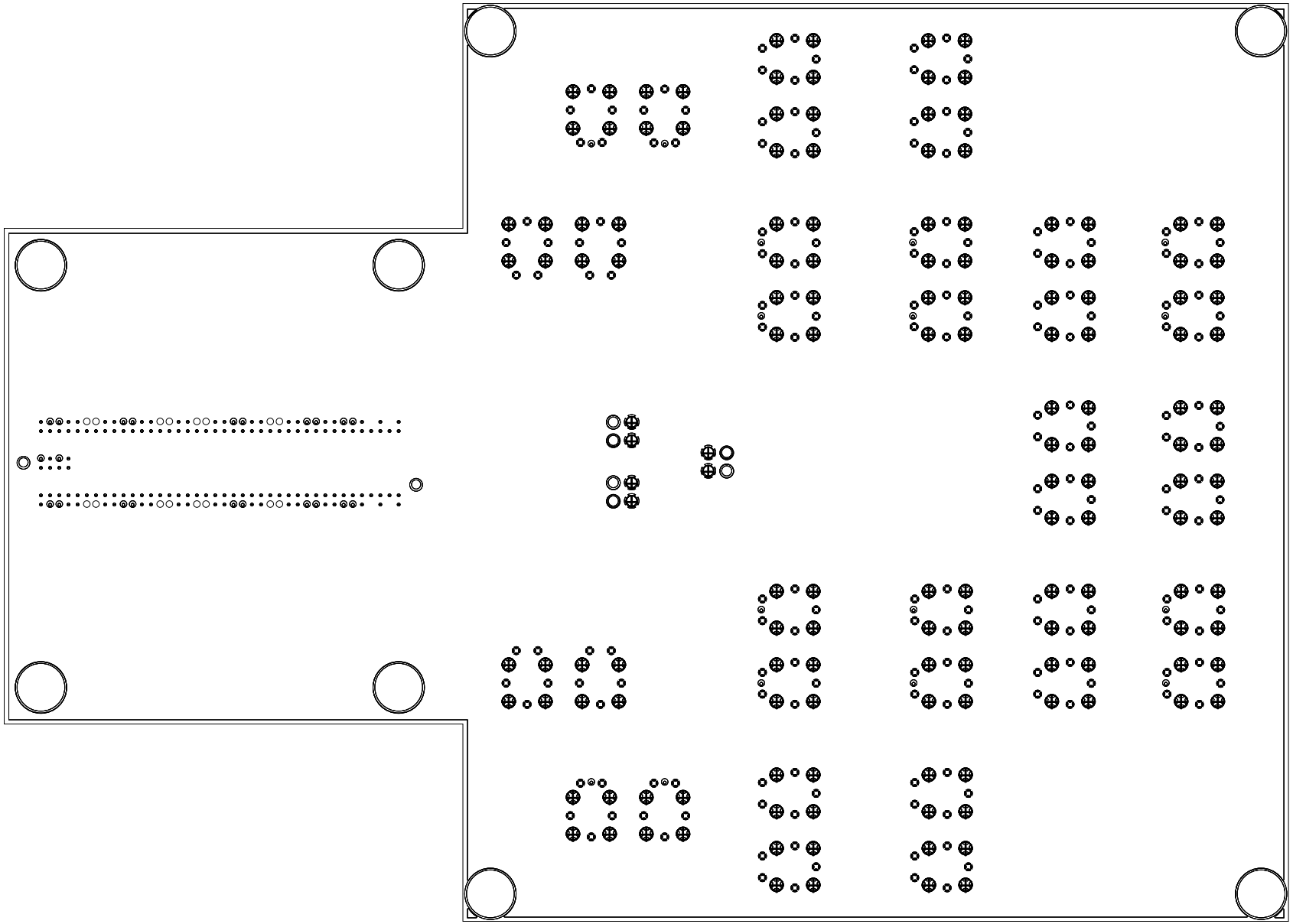

Figure 39. TLK10232 EVM SMA Breakout Board Layout, Internal GND (Layers 3, 4, 5)

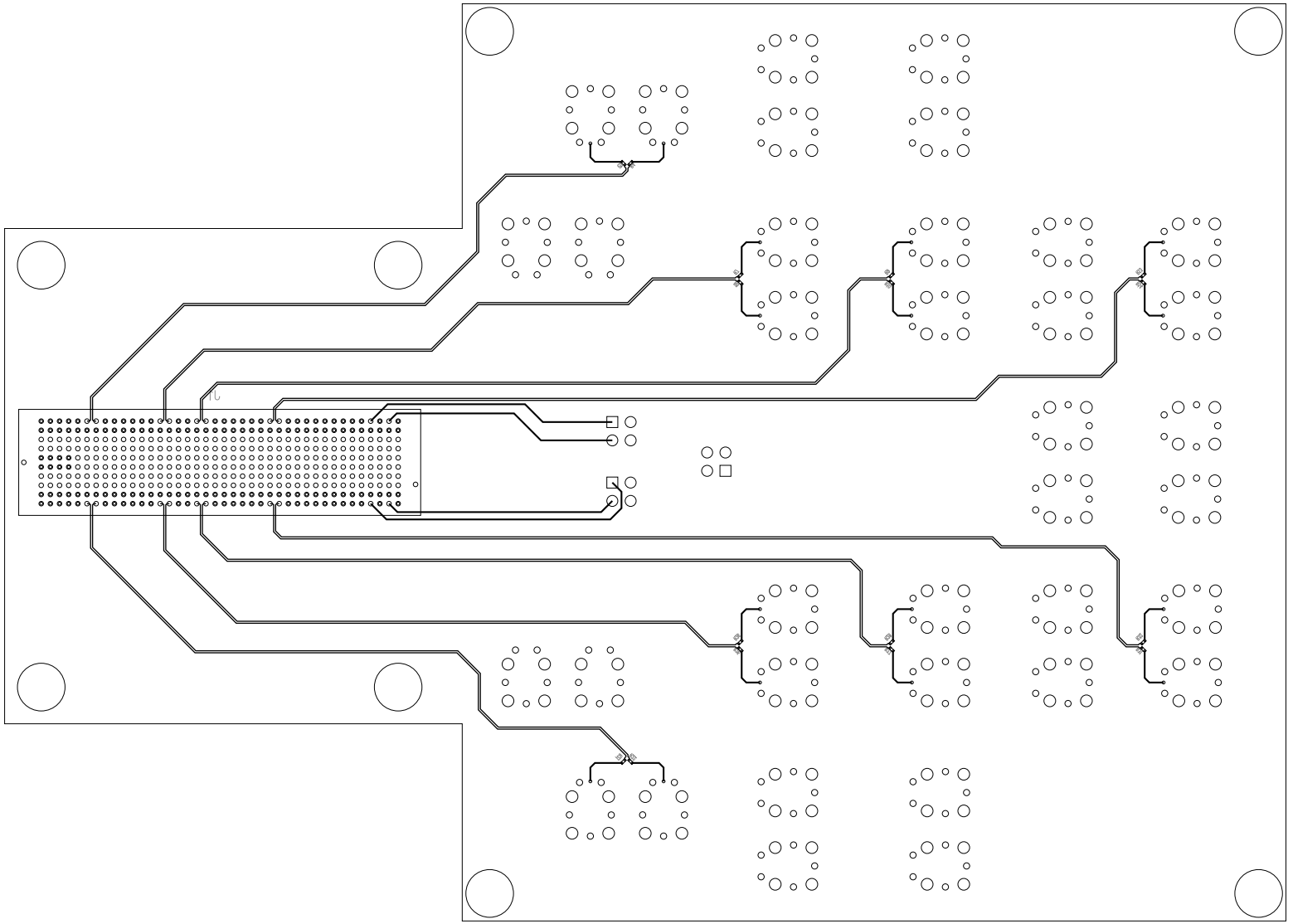

Figure 40. TLK10232 EVM SMA Breakout Board Layout, Bottom Signal (Layers 6)

Table 2 shows the EVM SMA breakout board layer construction.

Table 2. TLK10232 EVM SMA Breakout Board Layer Construction

Subclass Name	Type	Material	Thickness (MIL)	Dielectric Constant	Width (MIL)	Coupling Type / Spacing (MIL)
	SURFACE	AIR		1		
TOP	CONDUCTOR	COPPER	2	1	6.00 (Diff) 9.5 (Single)	Edge / 5.0 (Diff) None/None (Single)
	DIELECTRIC	FR-4	5	4.5		
L2_GND	PLANE	COPPER	1.2	1		
	DIELECTRIC	FR-4	20	4.5		
L3_GND	PLANE	COPPER	1.2	1	6.50 (Single)	None/None (Single)
	DIELECTRIC	FR-4	4	4.5		
L4_GND	PLANE	COPPER	1.2	1		
	DIELECTRIC	FR-4	20	4.5		
BOTTOM	CONDUCTOR	COPPER	2	1	6.00 (Diff) 9.5 (Single)	Edge / 5.0 (Diff) None/None (Single)
	SURFACE	AIR				

Note: The impedance is set to be slightly less than 50 Ω or 100 Ω on the traces in order to compensate for slight over-etching during the manufacturing process. The end impedance after etching should result in a 50- or 100-Ω impedance. Always consult with your board manufacturer for their process and design requirements to ensure the desired impedance is achieved.

15 TLK10232 EVM Voltage Monitor Board Schematics

Figure 41 through Figure 50 illustrate the EVM voltage monitor board schematics

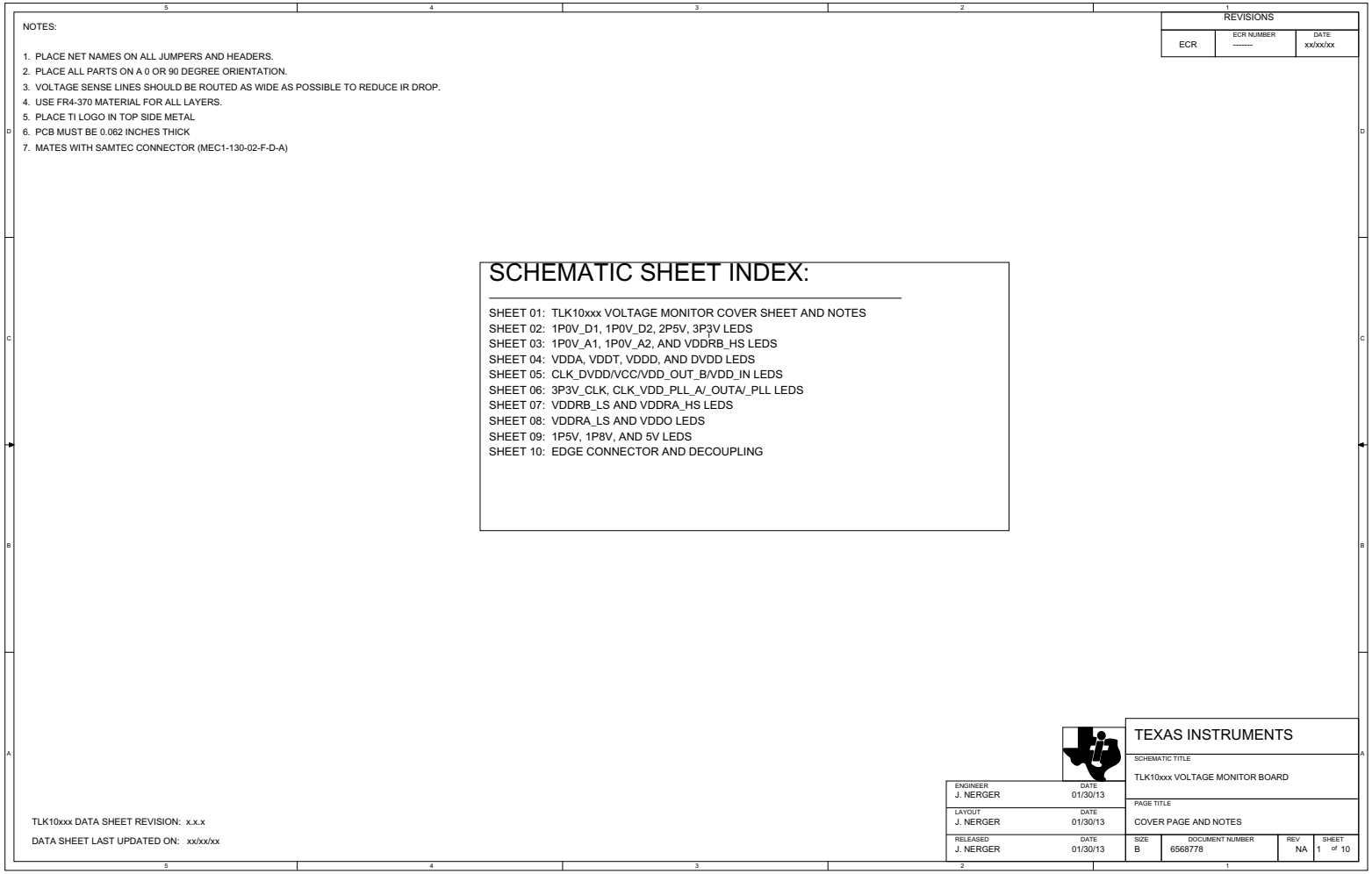

Figure 41. TLK10232 EVM Voltage Monitor Board Schematic, Sheet 1 Cover Page and Index

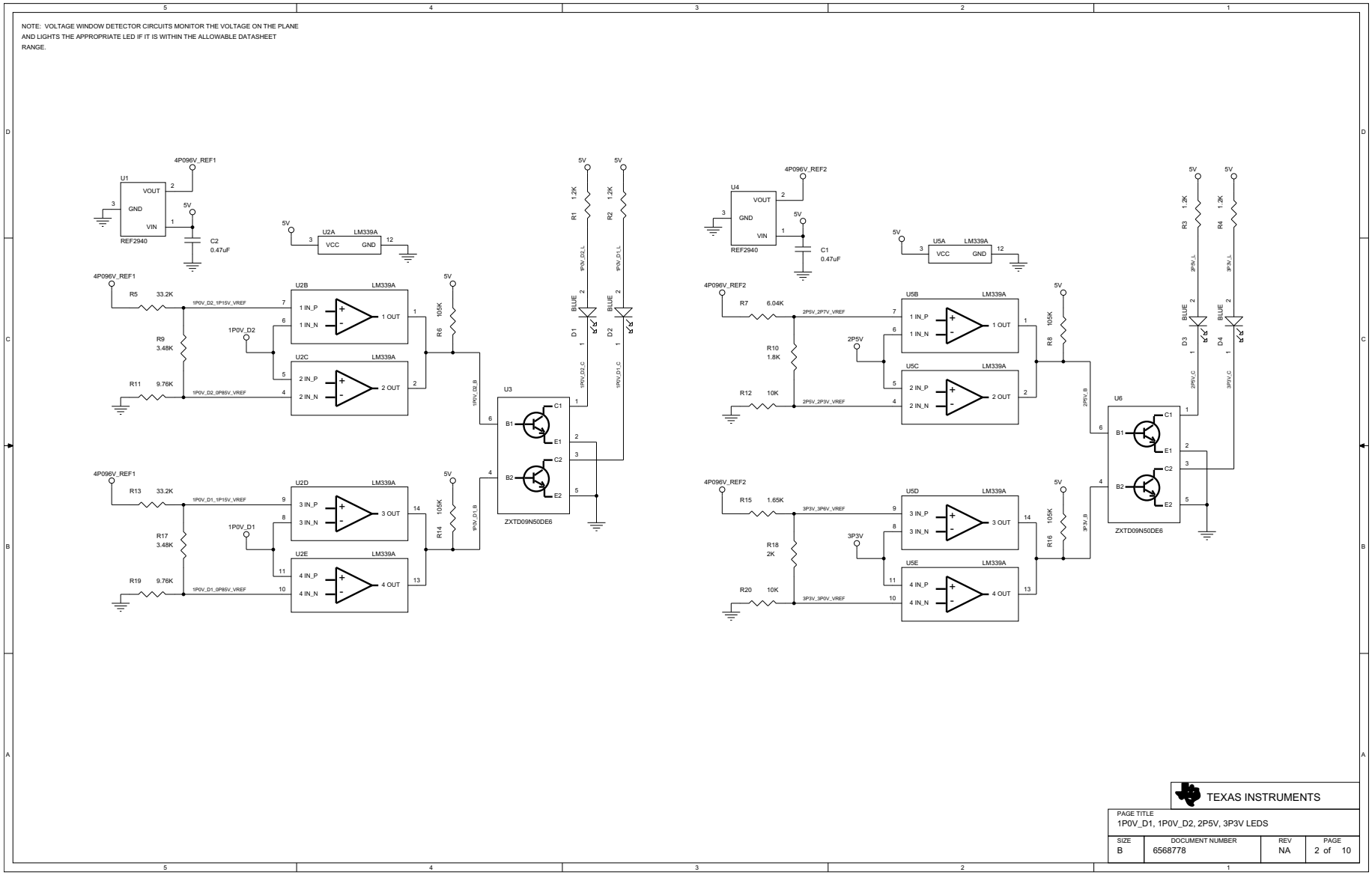

Figure 42. TLK10232 EVM Voltage Monitor Board Schematic, Sheet 2 1V_D1/D2, 2p5V, 3p3V LEDs

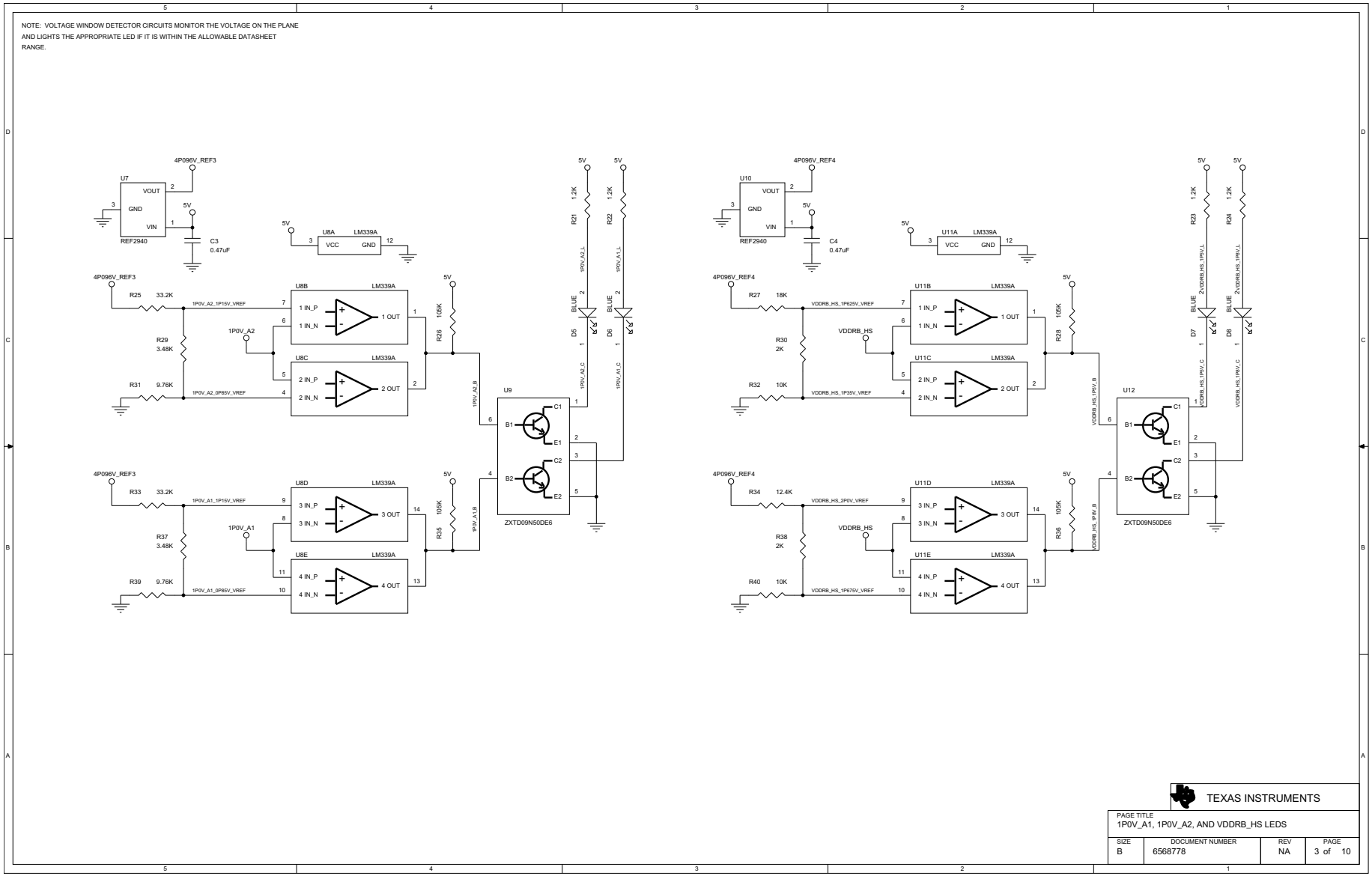

Figure 43. TLK10232 EVM Voltage Monitor Board Schematic, Sheet 3 1V_A1/A2, VDDRB_HS LEDs

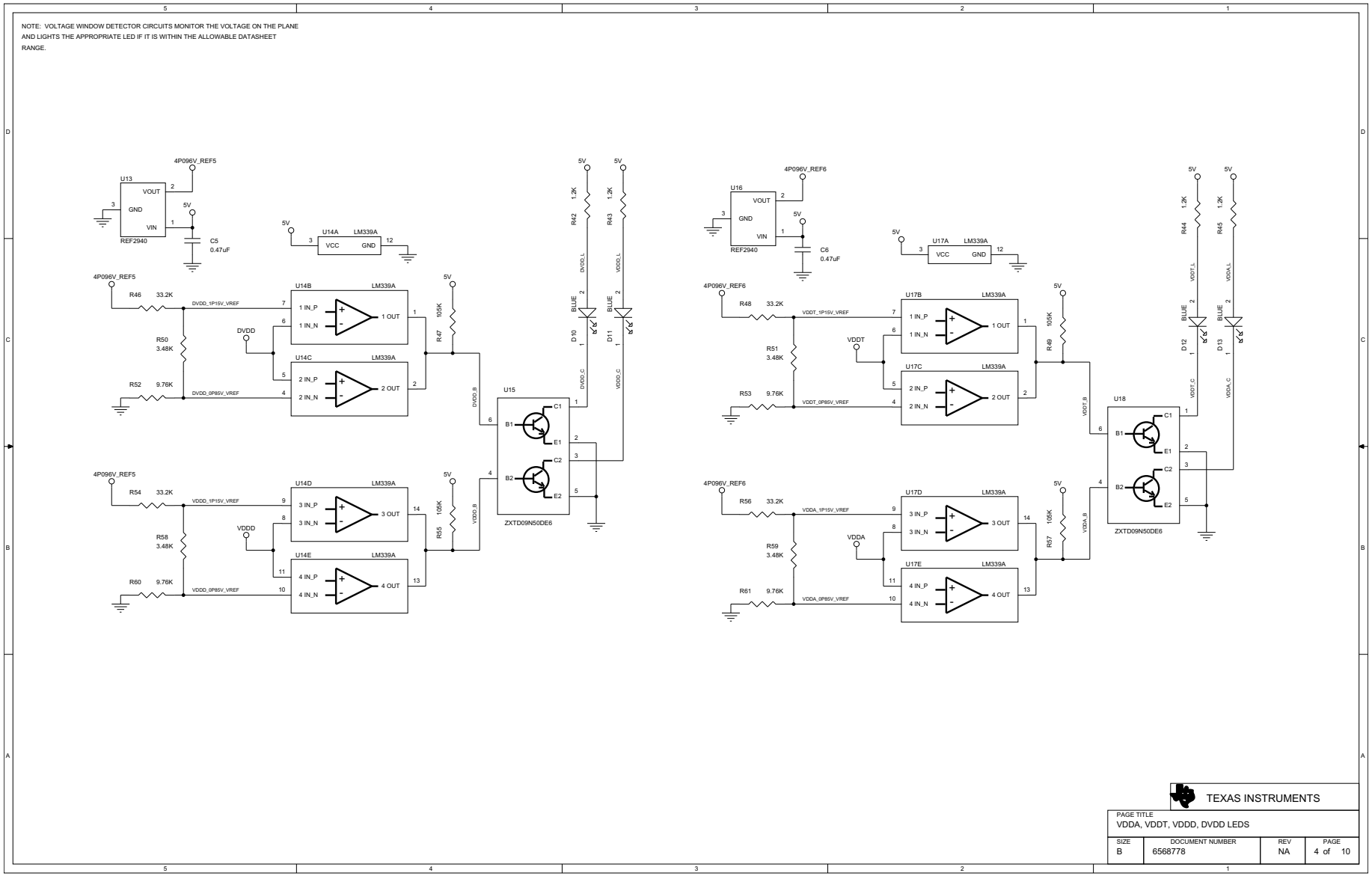

Figure 44. TLK10232 EVM Voltage Monitor Board Schematic, Sheet 4 VDDA, VDDT, VDDD, DVDD LEDs

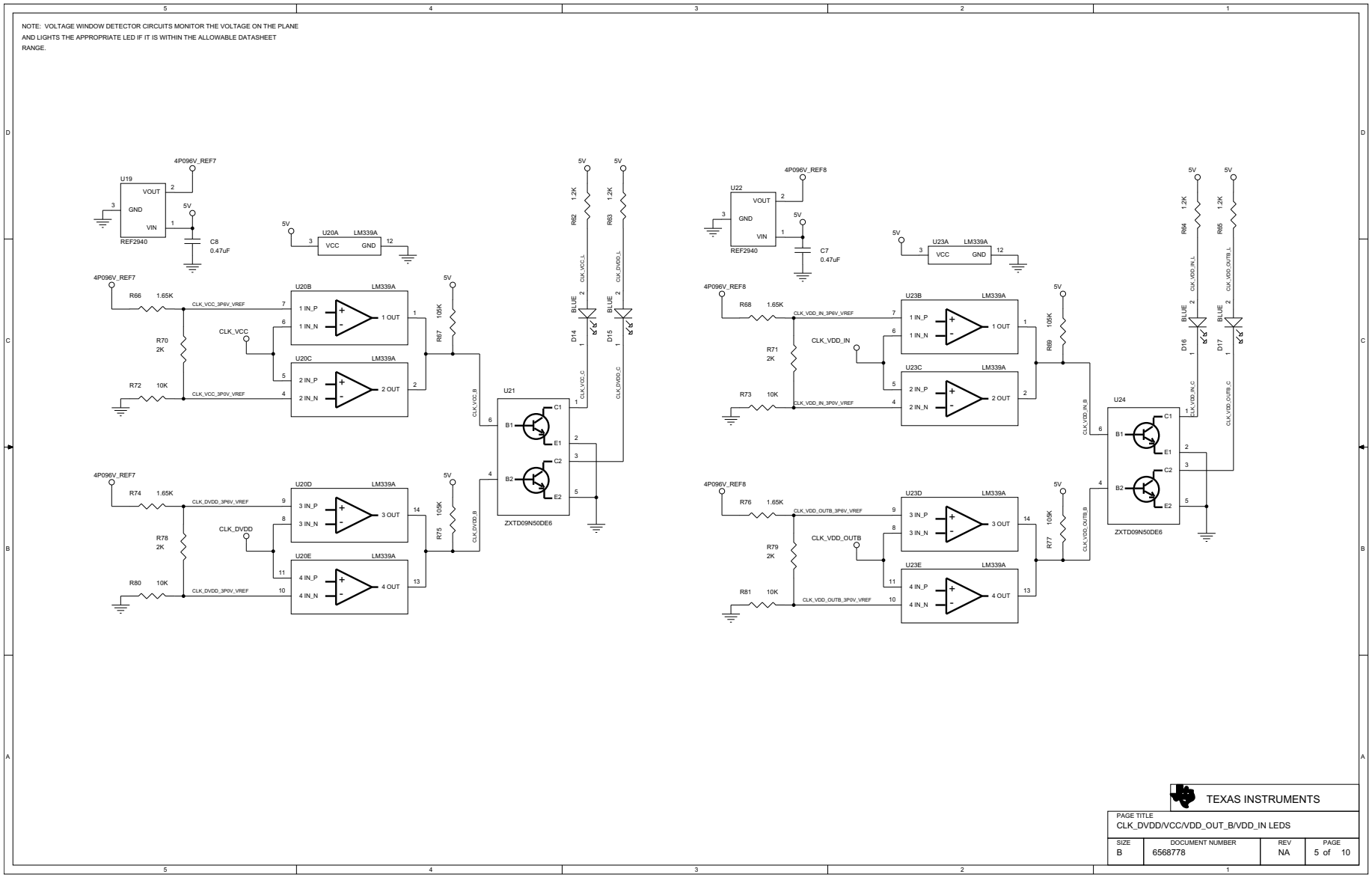

Figure 45. TLK10232 EVM Voltage Monitor Board Schematic, Sheet 5 CLK_DVDD/VCC/VDD_OUT_B/VDD_IN LEDs

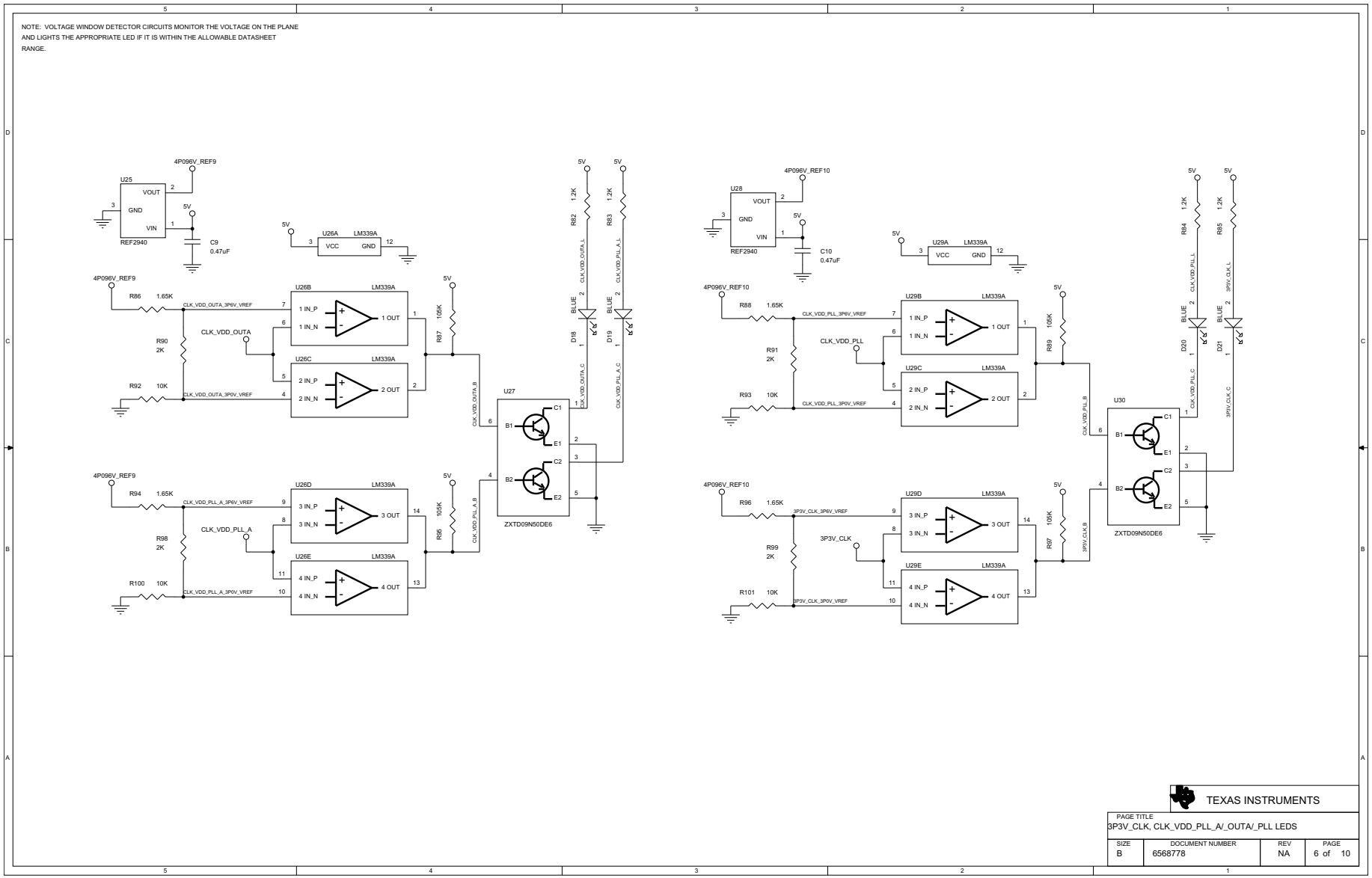

Figure 46. TLK10232 EVM Voltage Monitor Board Schematic, Sheet 6 3P3V_CLK, CLK_VDD_PLL_A/_OUTA/_PLL LEDs

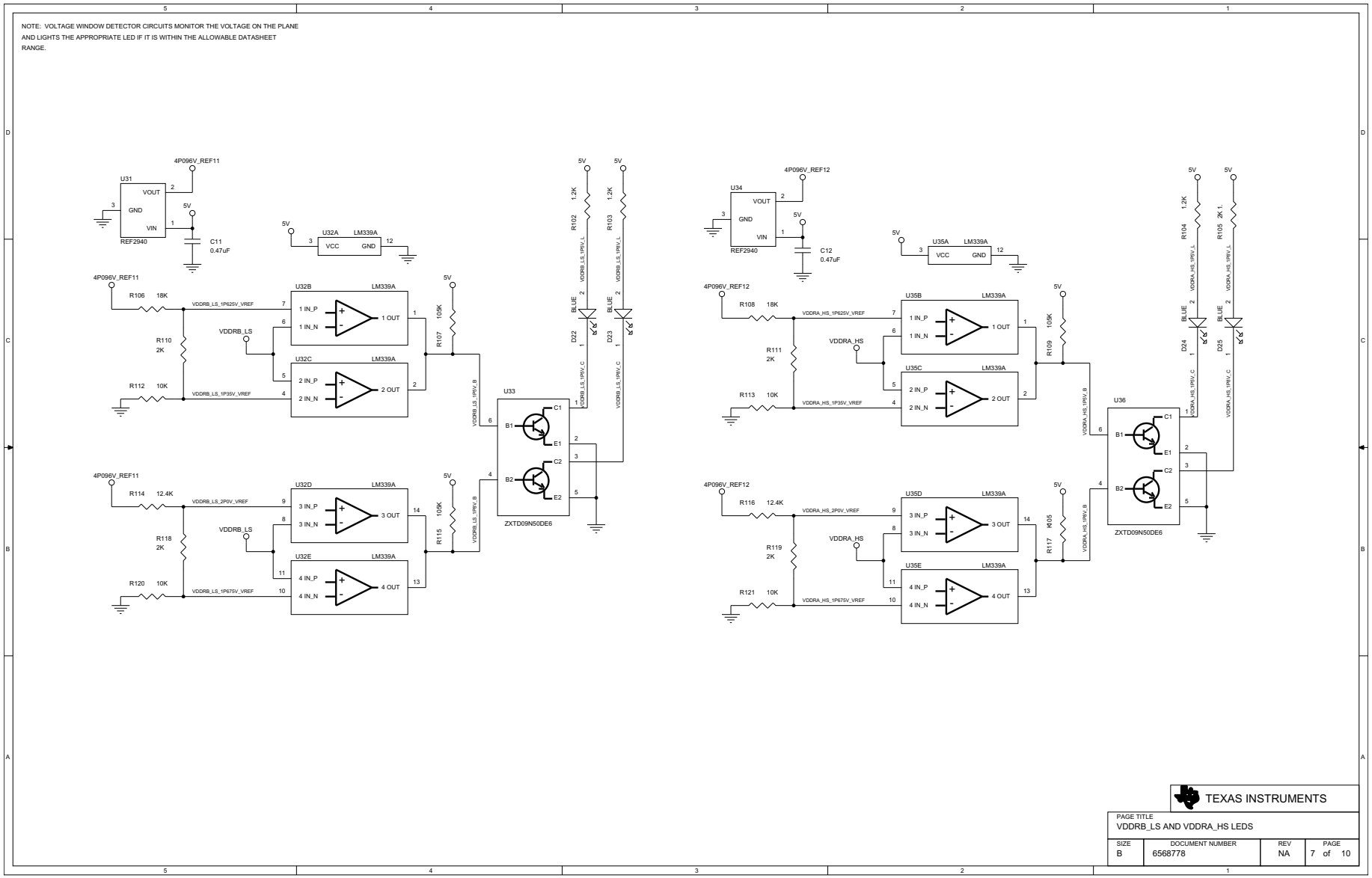

Figure 47. TLK10232 EVM Voltage Monitor Board Schematic, Sheet 7 VDDRB_LS AND VDDRA_HS LEDs

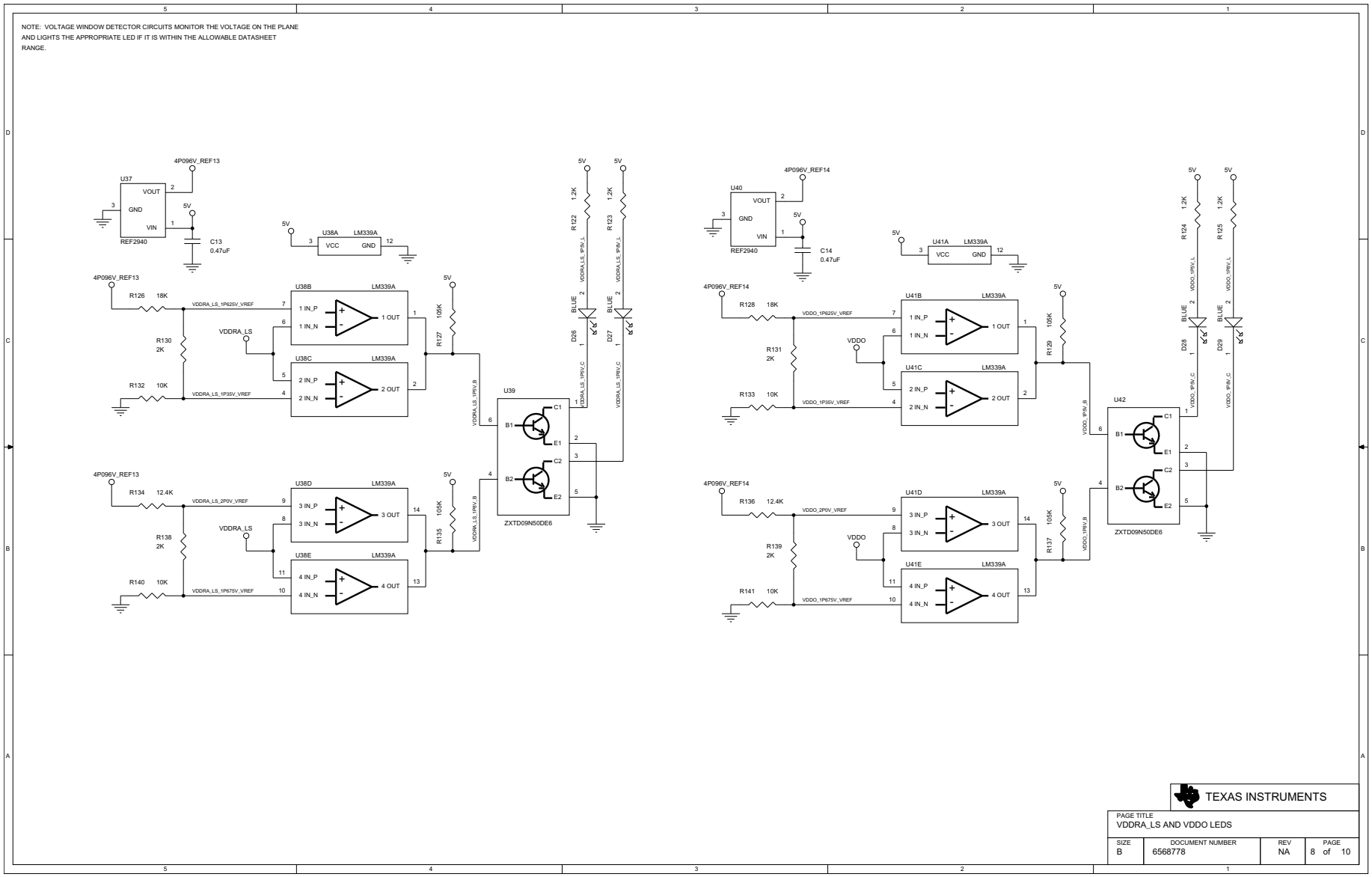

Figure 48. TLK10232 EVM Voltage Monitor Board Schematic, Sheet 8 VDDRA_LS AND VDDO LEDs

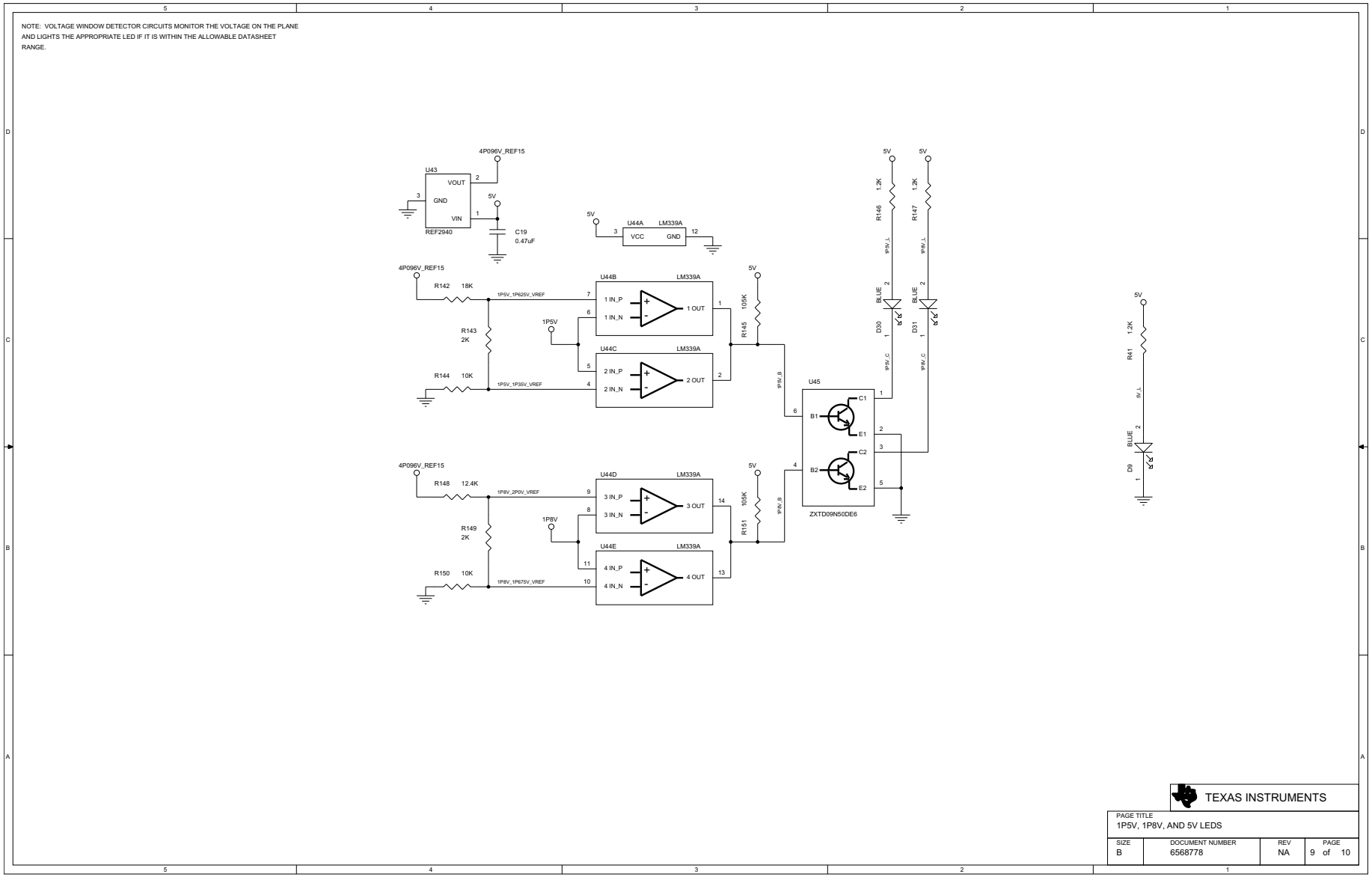

Figure 49. TLK10232 EVM Voltage Monitor Board Schematic, Sheet 9 1.5V, 1.8V, AND 5V LEDs

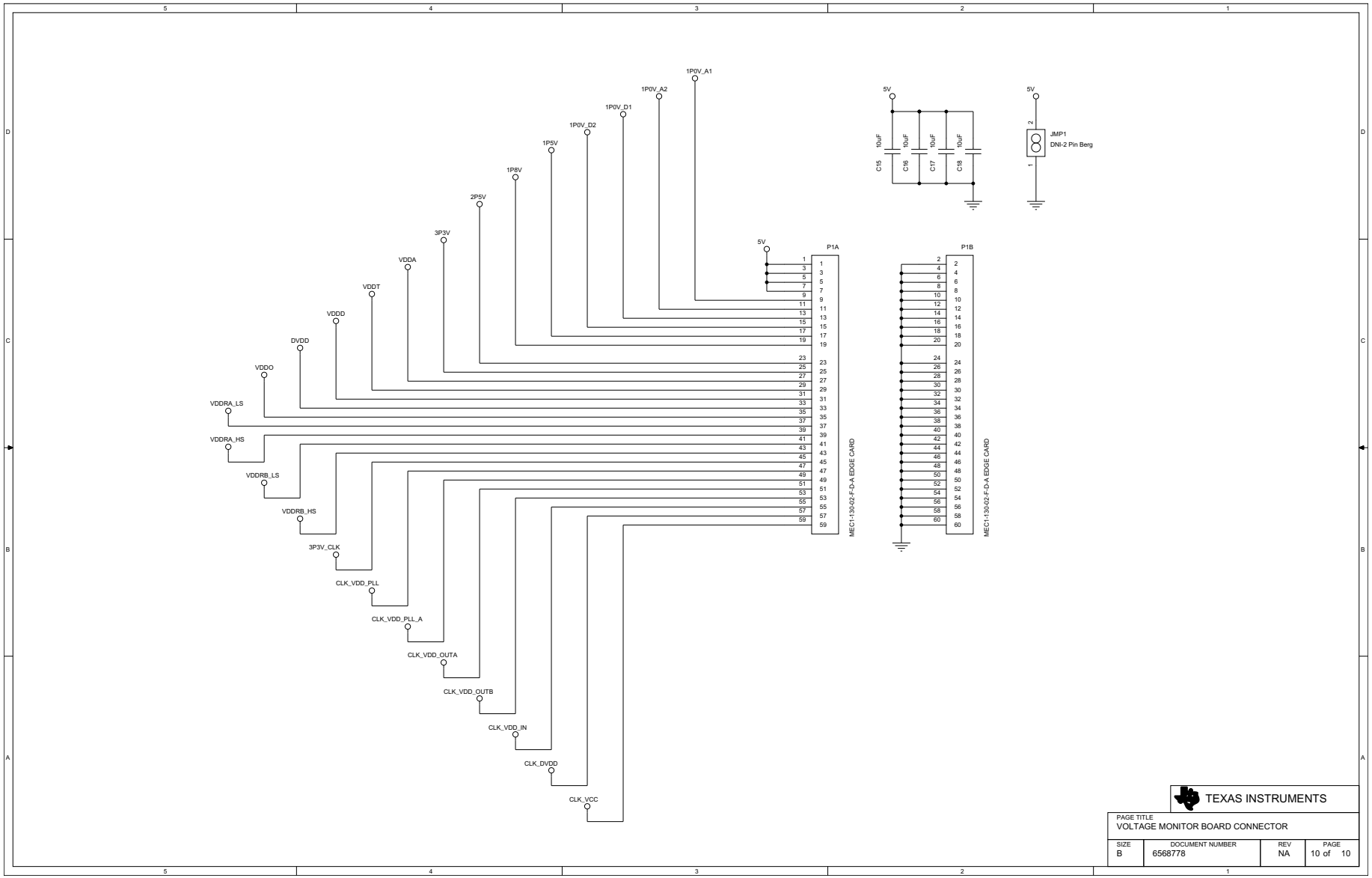

Figure 50. TLK10232 EVM Voltage Monitor Board Schematic, Sheet 10 Edge Connector

16 TLK10232 EVM Voltage Monitor Board Layout

Figure 51 through Figure 54 illustrate the EVM voltage monitor board layout.

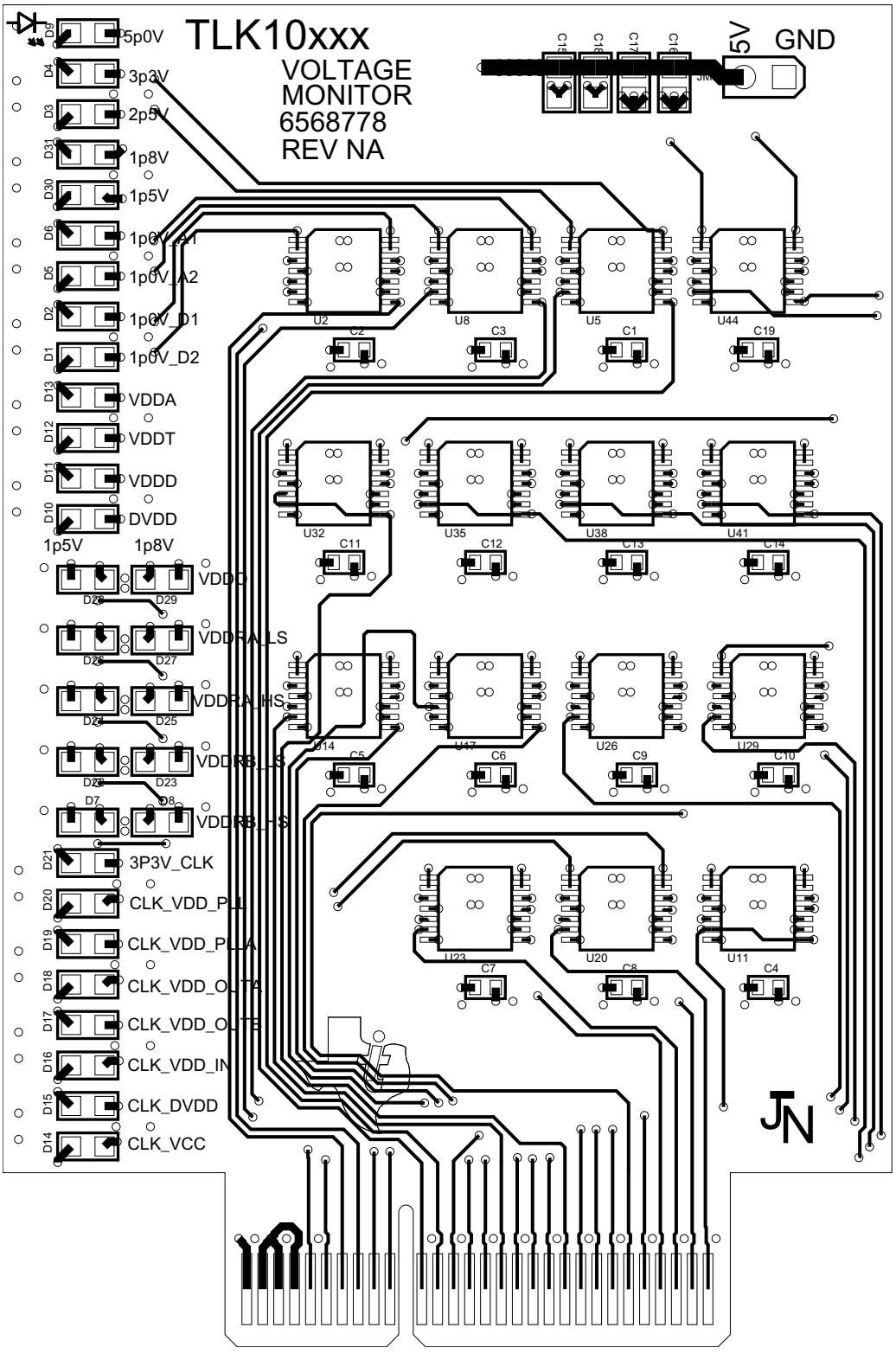

Figure 51. TLK10232 EVM Voltage Monitor Board Layout, Top Signal Layer

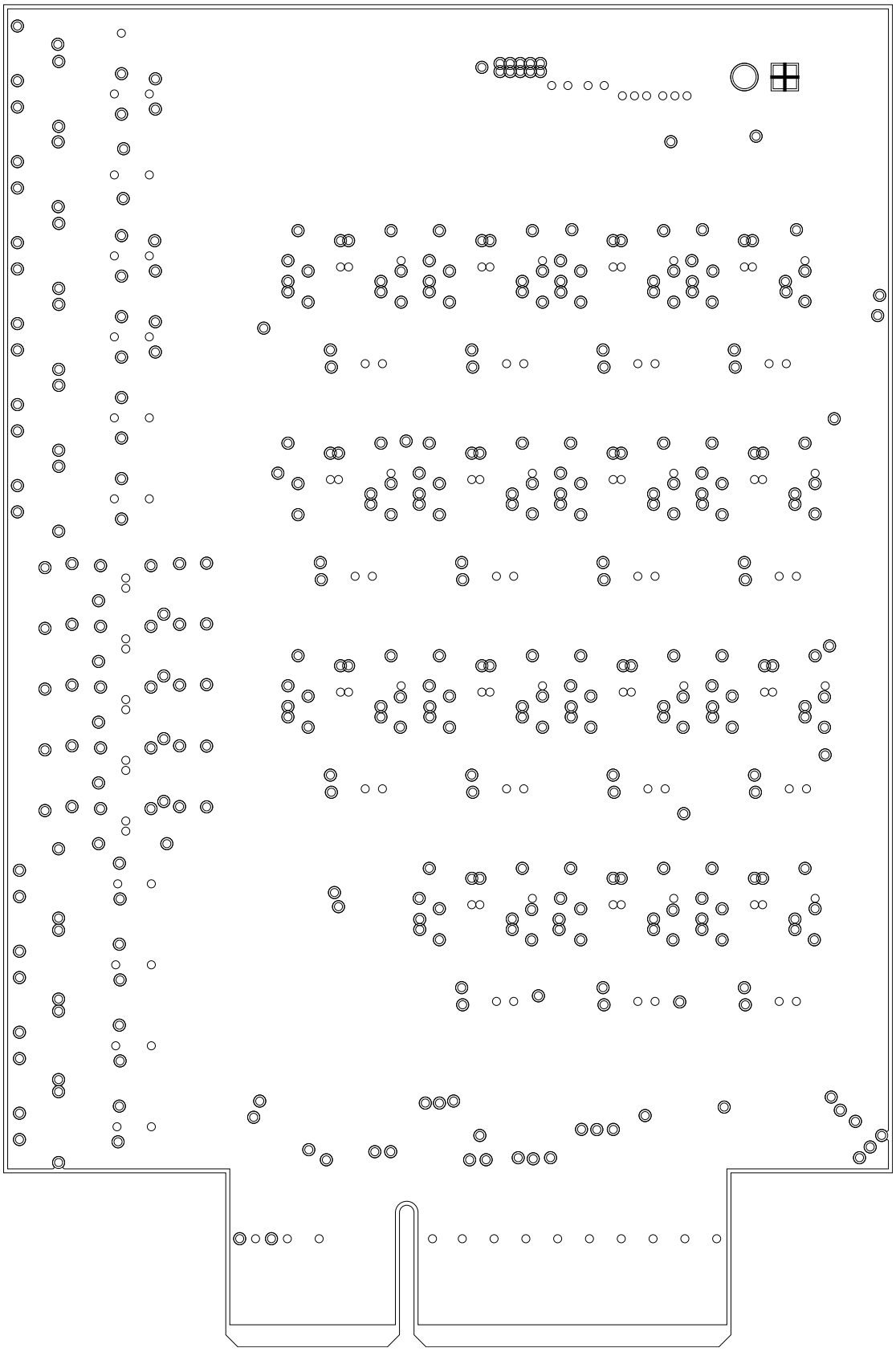

Figure 52. TLK10232 EVM Voltage Monitor Board Layout, Internal Ground (Layer 2)

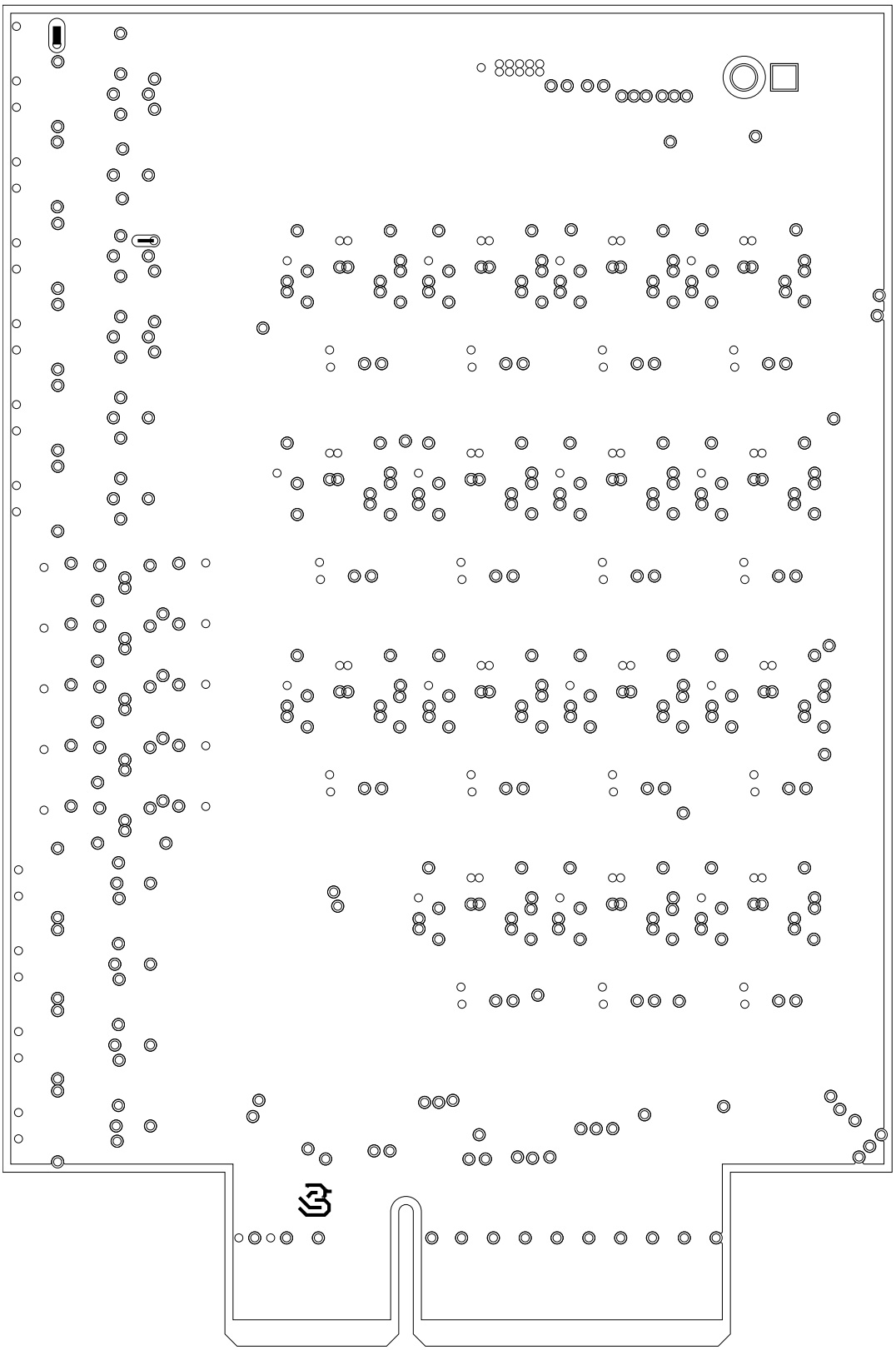

Figure 53. TLK10232 EVM Voltage Monitor Board Layout, Internal Power (Layer 3)

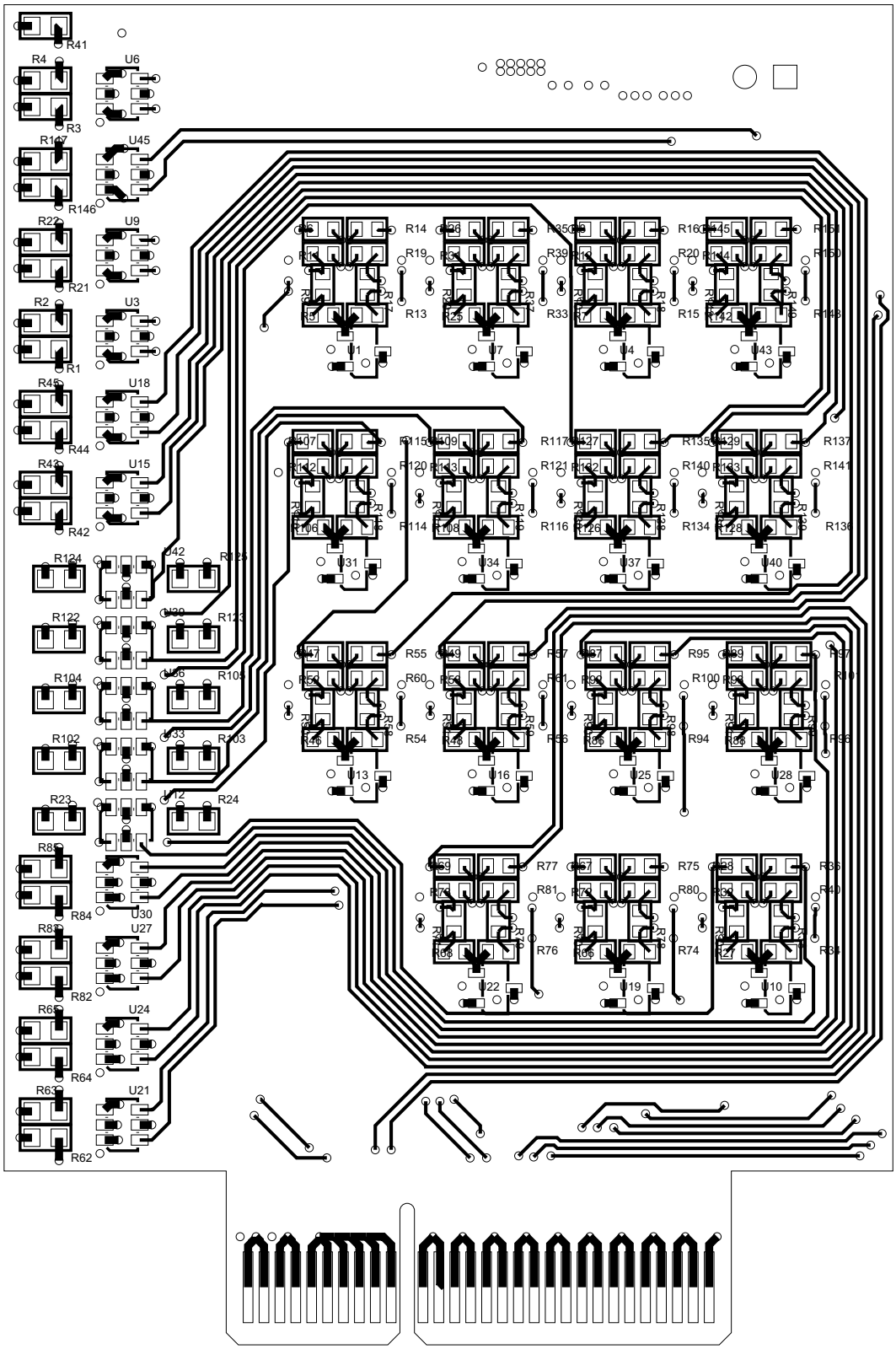

Figure 54. TLK10232 EVM Voltage Monitor Board Layout, Bottom Signal (Layer 4)

Table 3 shows the EVM voltage monitor board layer construction.

Table 3. TLK10232 EVM Voltage Monitor Board Layer Construction

Subclass Name	Type	Material	Thickness (MIL)	Dielectric Constant	Width (MIL)	Coupling Type / Spacing (MIL)
	SURFACE	AIR		1		
TOP	CONDUCTOR	COPPER	2	1	8.5 (Single)	None/None (Single)
	DIELECTRIC	FR-4	5	4.5		
L2_GND	PLANE	COPPER	1.2	1		
	DIELECTRIC	FR-4	45	4.5		
L3_PWR	PLANE	COPPER	1.2	1		
	DIELECTRIC	FR-4	5	4.5		
BOTTOM	CONDUCTOR	COPPER	2	1	8.5 (Single)	None/None (Single)
	SURFACE	AIR				

Note: The impedance is set to be slightly less than 50 Ω or 100 Ω on the traces in order to compensate for slight over-etching during the manufacturing process. The end impedance after etching should result in a 50- or 100-Ω impedance. Always consult with your board manufacturer for their process and design requirements to ensure the desired impedance is achieved.

17 TLK10232 EVM USB Dongle Board Schematics

Figure 55 through Figure 56 are illustrations of the USB Dongle board schematics.

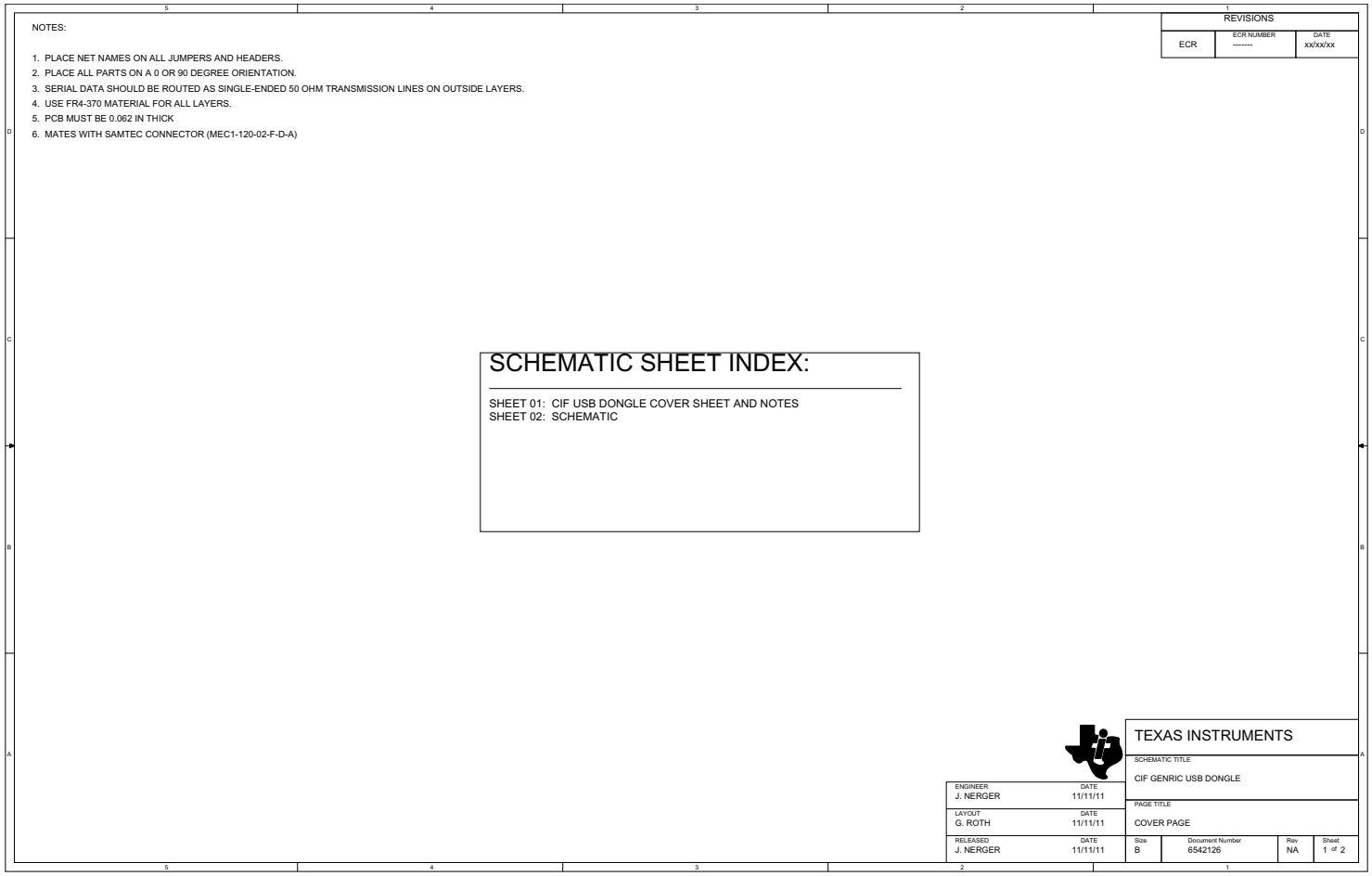

Figure 55. TLK10232 EVM USB Dongle Board Schematic, Sheet 1 Cover Page and Index

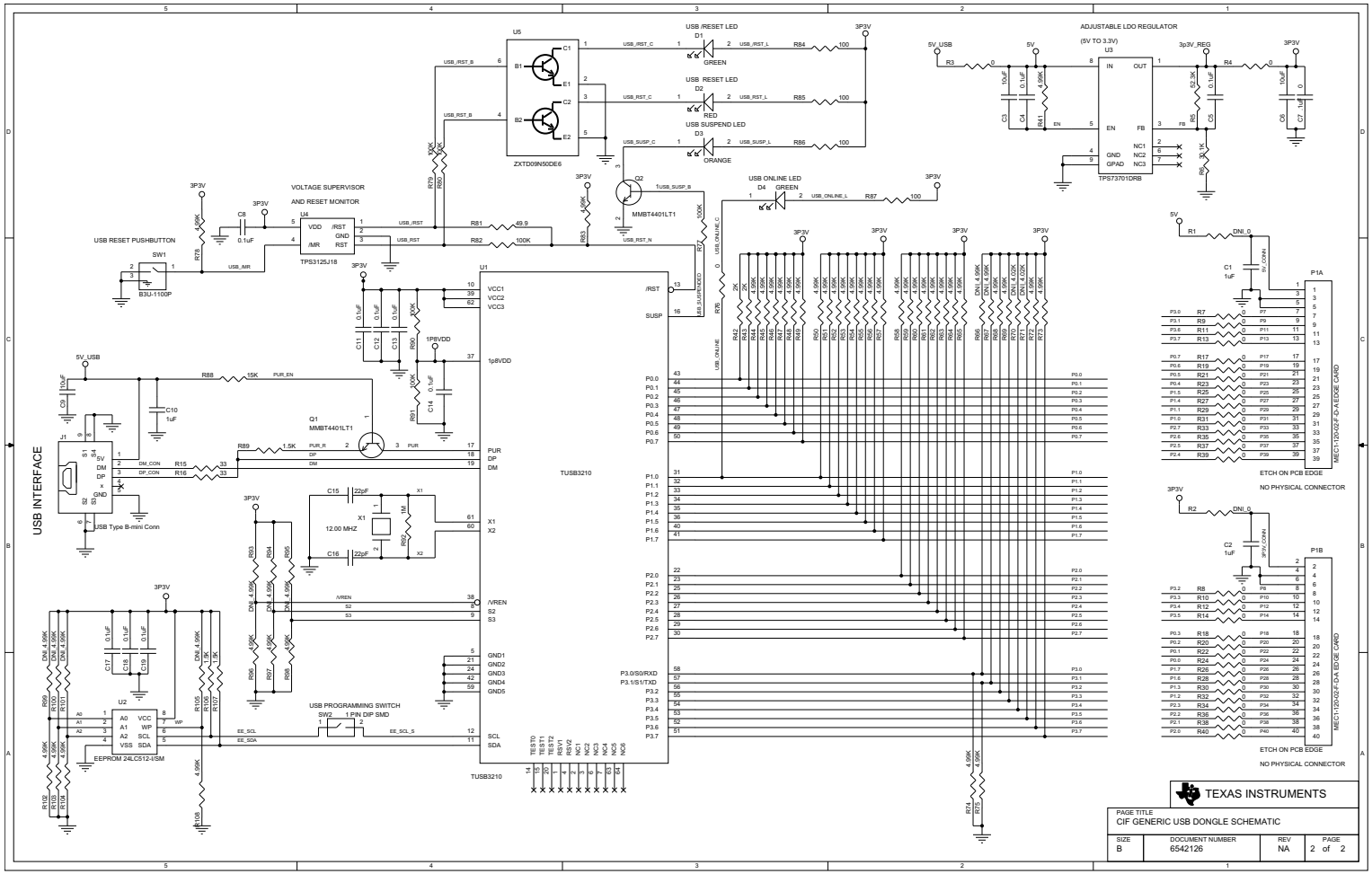

Figure 56. TLK10232 EVM USB Dongle Board Schematic, Sheet 2 Schematics

18 TLK10232 EVM USB Dongle Board Layout

Figure 57 through Figure 60 are illustrations of the USB Dongle board layout.

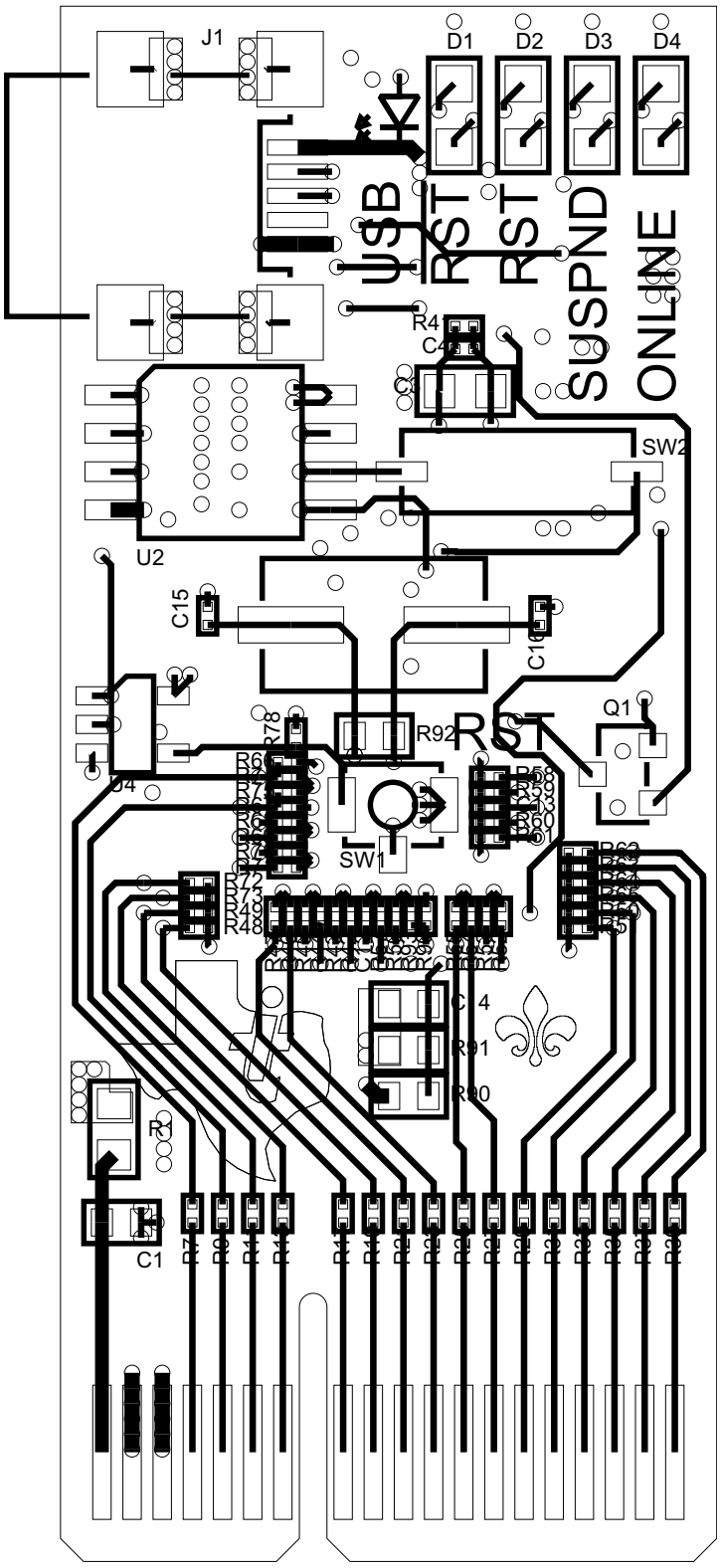

Figure 57. TLK10232 EVM USB Dongle Board Layout, Top Signal Layer

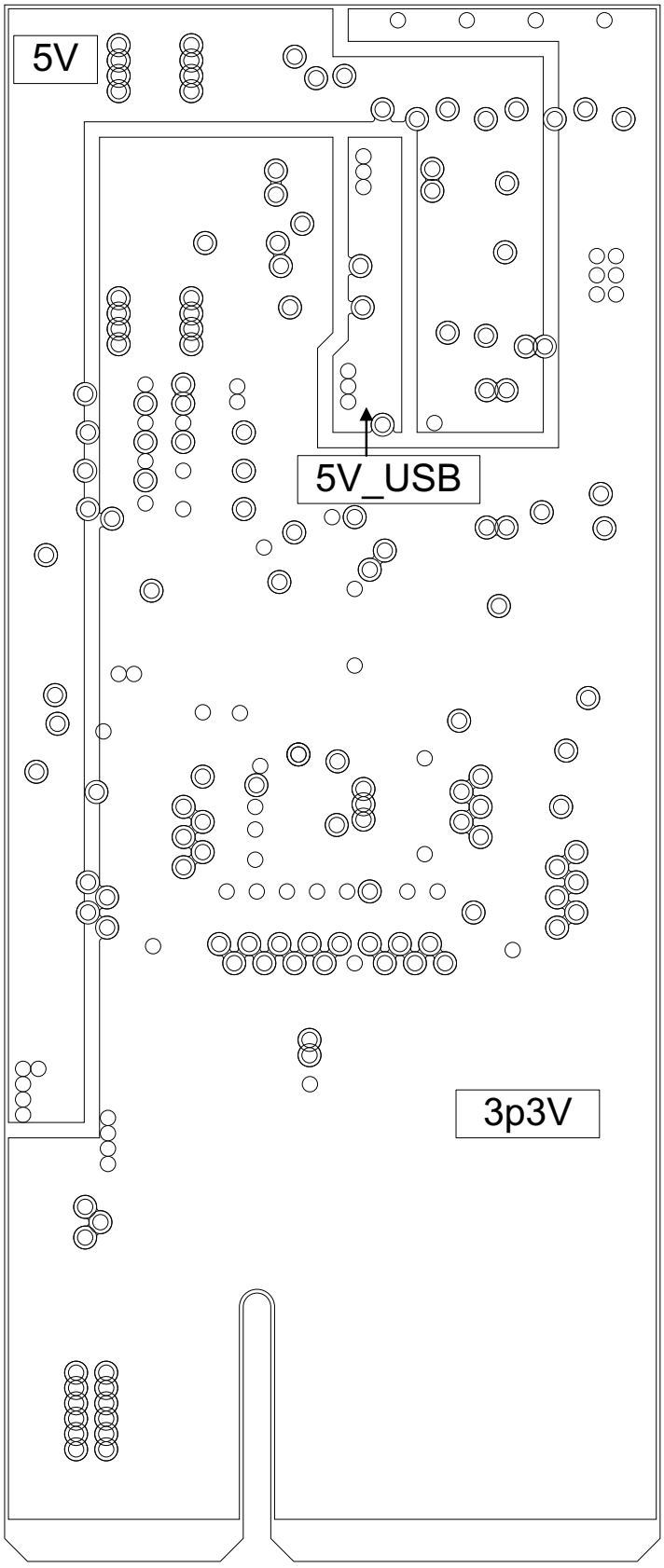

Figure 58. TLK10232 EVM USB Dole Board Layout, Internal Power (Layer 2)

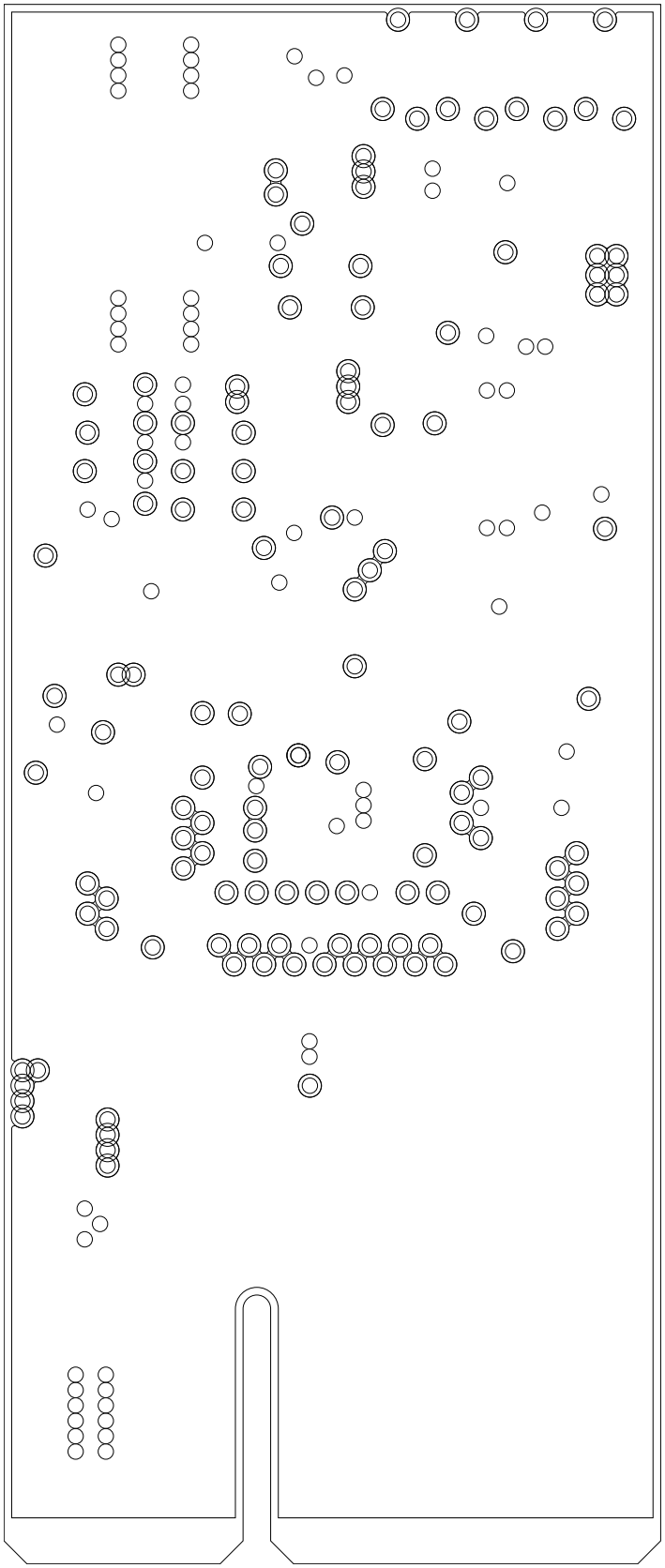

Figure 59. TLK10232 EVM USB Dongle Board Layout, Internal GND (Layer 3)

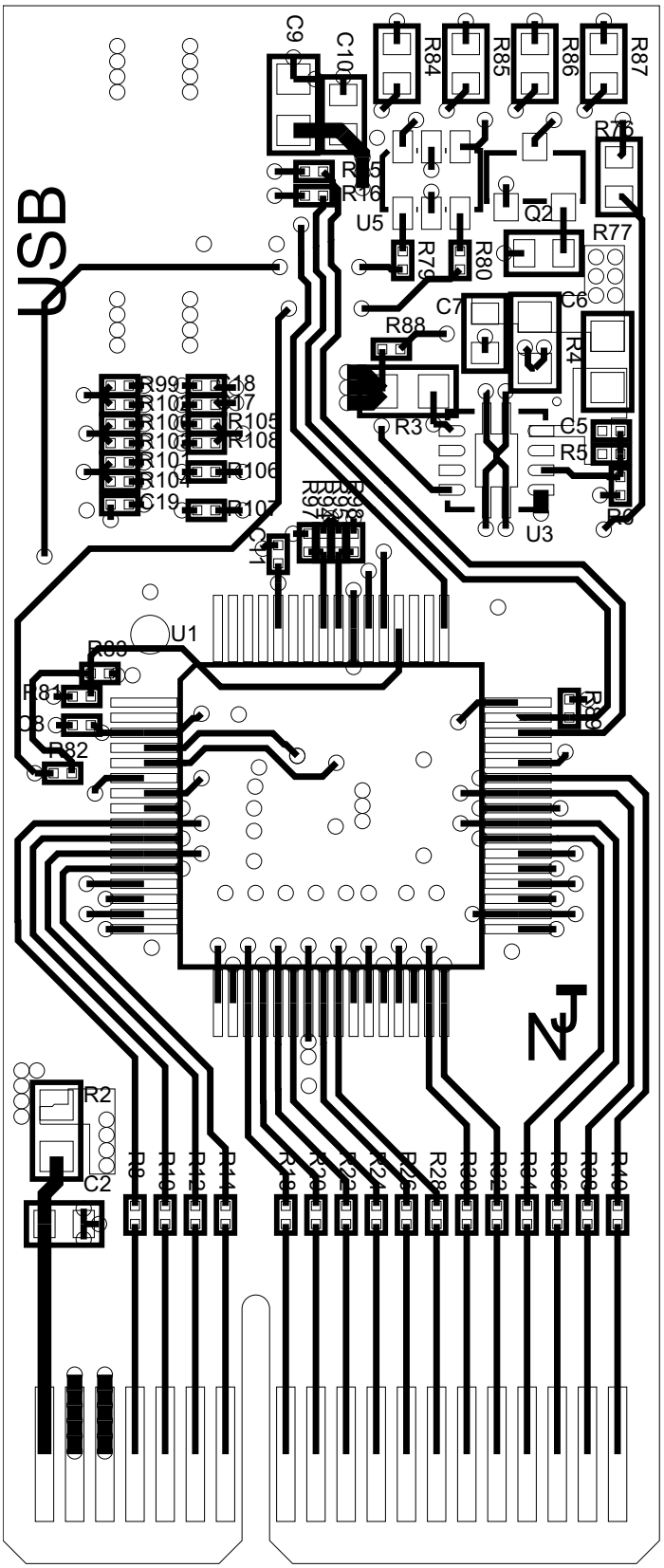

Figure 60. TLK10232 EVM USB Dongle Board Layout, Bottom Signal (Layer 4 Top View)

Table 4 is the USB dongle board layer construction for this EVM.

Table 4. TLK10232 EVM USB Dongle Board Layer Construction

Subclass Name	Type	Material	Thickness (MIL)	Dielectric Constant	Width (MIL)	Coupling Type / Spacing (MIL)
	SURFACE	AIR		1		
TOP	CONDUCTOR	COPPER	2	1	8.5 (Single)	None/None (Single)
	DIELECTRIC	FR-4	5	4.5		
L2_GND	PLANE	COPPER	1.2	1		
	DIELECTRIC	FR-4	45	4.5		
L3_PWR	PLANE	COPPER	1.2	1		
	DIELECTRIC	FR-4	5	4.5		
BOTTOM	CONDUCTOR	COPPER	2	1	8.5 (Single)	None/None (Single)
	SURFACE	AIR				

Note: The impedance is set to be slightly less than 50 Ω or 100 Ω on the traces in order to compensate for slight over-etching during the manufacturing process. The end impedance after etching should result in a 50- or 100-Ω impedance. Always consult with your board manufacturer for their process and design requirements to ensure the desired impedance is achieved.

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REGULATORY COMPLIANCE INFORMATION

As noted in the EVM User's Guide and/or EVM itself, this EVM and/or accompanying hardware may or may not be subject to the Federal Communications Commission (FCC) and Industry Canada (IC) rules.

For EVMs **not** subject to the above rules, this evaluation board/kit/module is intended for use for ENGINEERING DEVELOPMENT, DEMONSTRATION OR EVALUATION PURPOSES ONLY and is not considered by TI to be a finished end product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC or ICES-003 rules, which are designed to provide reasonable protection against radio frequency interference. Operation of the equipment may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

General Statement for EVMs including a radio

User Power/Frequency Use Obligations: This radio is intended for development/professional use only in legally allocated frequency and power limits. Any use of radio frequencies and/or power availability of this EVM and its development application(s) must comply with local laws governing radio spectrum allocation and power limits for this evaluation module. It is the user's sole responsibility to only operate this radio in legally acceptable frequency space and within legally mandated power limitations. Any exceptions to this are strictly prohibited and unauthorized by Texas Instruments unless user has obtained appropriate experimental/development licenses from local regulatory authorities, which is responsibility of user including its acceptable authorization.

For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant

Caution

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

For EVMs annotated as IC – INDUSTRY CANADA Compliant

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Concerning EVMs including radio transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs including detachable antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada.

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

【Important Notice for Users of this Product in Japan】

This development kit is NOT certified as Confirming to Technical Regulations of Radio Law of Japan

If you use this product in Japan, you are required by Radio Law of Japan to follow the instructions below with respect to this product:

1. Use this product in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use this product only after you obtained the license of Test Radio Station as provided in Radio Law of Japan with respect to this product, or
3. Use of this product only after you obtained the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to this product. Also, please do not transfer this product, unless you give the same notice above to the transferee. Please note that if you could not follow the instructions above, you will be subject to penalties of Radio Law of Japan.

Texas Instruments Japan Limited
(address) 24-1, Nishi-Shinjuku 6 chome, Shinjuku-ku, Tokyo, Japan

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http://www.tij.co.jp

EVALUATION BOARD/KIT/MODULE (EVM)
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For Feasibility Evaluation Only, in Laboratory/Development Environments. Unless otherwise indicated, this EVM is not a finished electrical equipment and not intended for consumer use. It is intended solely for use for preliminary feasibility evaluation in laboratory/development environments by technically qualified electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems and subsystems. It should not be used as all or part of a finished end product.

Your Sole Responsibility and Risk. You acknowledge, represent and agree that:

1. You have unique knowledge concerning Federal, State and local regulatory requirements (including but not limited to Food and Drug Administration regulations, if applicable) which relate to your products and which relate to your use (and/or that of your employees, affiliates, contractors or designees) of the EVM for evaluation, testing and other purposes.
2. You have full and exclusive responsibility to assure the safety and compliance of your products with all such laws and other applicable regulatory requirements, and also to assure the safety of any activities to be conducted by you and/or your employees, affiliates, contractors or designees, using the EVM. Further, you are responsible to assure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard.
3. You will employ reasonable safeguards to ensure that your use of the EVM will not result in any property damage, injury or death, even if the EVM should fail to perform as described or expected.
4. You will take care of proper disposal and recycling of the EVM's electronic components and packing materials.

Certain Instructions. It is important to operate this EVM within TI's recommended specifications and environmental considerations per the user guidelines. Exceeding the specified EVM ratings (including but not limited to input and output voltage, current, power, and environmental ranges) may cause property damage, personal injury or death. If there are questions concerning these ratings please contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, some circuit components may have case temperatures greater than 60°C as long as the input and output are maintained at a normal ambient operating temperature. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors which can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during normal operation, please be aware that these devices may be very warm to the touch. As with all electronic evaluation tools, only qualified personnel knowledgeable in electronic measurement and diagnostics normally found in development environments should use these EVMs.

Agreement to Defend, Indemnify and Hold Harmless. You agree to defend, indemnify and hold TI, its licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, "Claims") arising out of or in connection with any use of the EVM that is not in accordance with the terms of the agreement. This obligation shall apply whether Claims arise under law of tort or contract or any other legal theory, and even if the EVM fails to perform as described or expected.

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