Application Note

Combining Classical RS-485 Systems with TI's RS-485 Based Powerbus

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ABSTRACT

RS-485 is a long-standing differential wired communication heavily relied upon in many industrial applications from factory and building automation, motor drives, medical devices, and grid infrastructure to name a few. The standard is prized for its ability to create long distance wired communication networks across multiple communication nodes while maintaining the robustness required for harsh industrial operating environments. With bus lengths up to 1.2 km (approx. 4000ft) cabling quickly becomes one of the costliest aspects of the system, with cabling requiring at minimum two data lines, neutral, and power cables; it becomes quickly apparent that cost saving measures would be beneficial to end users.

TI's Powerbus is one way to meet this need as it allows power and data to share the same cabling through On-Off Keying (OOK) modulated RS-485. However, Powerbus and Classical RS-485 are not directly compatible so typically they cannot be mixed and matched. This is problematic for some end users that could benefit from Powerbus, but in some of their systems they don't control the design of every communication node, so they can't directly implement Powerbus. This application note aims to guide end users how to design one board that can be placed either in Classical RS-485 systems or systems using Powerbus.

Table of Contents

List of Figures

List of Tables

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1 Introduction

In long distance RS-485 systems the need to find cost effective solutions without risking performance is paramount to a successful system design. TI's Powerbus devices, the THVD8000 and THVD8010, tackle this issue by using OOK modulation of RS-485 and an external coupling network to allow data and power to share the same bus. However due to the nature of Classical RS-485 against Powerbus neither device can properly understand each other preventing communication between Classical RS-485 and Powerbus.

This presents a problem in large systems where the designer may not have control of every communication node connected to the bus and can cause the designer to fall back on Classical RS-485 to ensure compatibility in all of their systems. However combined solutions can exist to allow one board to be designed for multiple systems – Powerbus or not. This note will first cover what Powerbus is and how it works. Next it will delve into the differences between Powerbus and Classical RS-485 analyzing where the incompatibility lies. Finally, a look into a joint solution that can be applied into varied systems.

2 What is Powerbus?

Before any comparison between Classical RS-485 and Powerbus can occur, a thorough understanding of the theoretical underpinnings of TI's Powerbus is required. First a look into the OOK modulation scheme, as well as, the physical modulator and demodulator shows how the data is encoded and decoded. Then a look into the physical transceiver and how the transceiver operates on the bus. Finally, a look into the external coupling network and the function the network serves.

OOK modulation, which is also known as On-Off Keying, is the simplest form of Amplitude Shift Keying (ASK) which represents digital data with the presence or absence of a carrier signal. In TI's Powerbus this is taken a little farther by taking lower speed digital data transmissions and sending out a higher frequency (at least 10 times the data-rate) OOK modulated signal where the presence of the carrier signal indicates a logic low (binary value 0) and the absence of a carrier signal indicates a logic high (binary value 1).

Input Bit	Powerbus OOK Output	Powerbus OOK Input	Output Bit
0	Carrier Active at Modulation Frequency	Carrier Active at Modulation Frequency	0
1	Bus Idle – No Carrier Active	Bus Idle – No Carrier Active	1

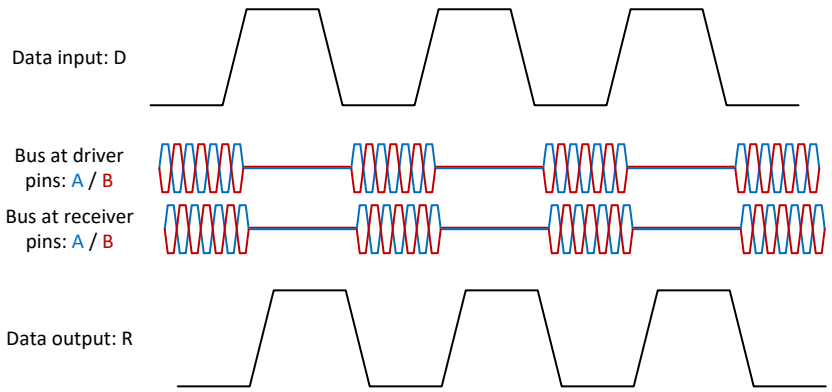


Figure 2-1. THVD80x0: Modulation and Demodulation

Modulation frequency is chosen via a setting resistor on the THVD8000 or THVD8010. The THVD8000 can have a modulation frequency from 125kHz to 5MHz while the THVD8010 is from 125kHz to 300kHz, but is less sensitive to noise than the THVD8000.

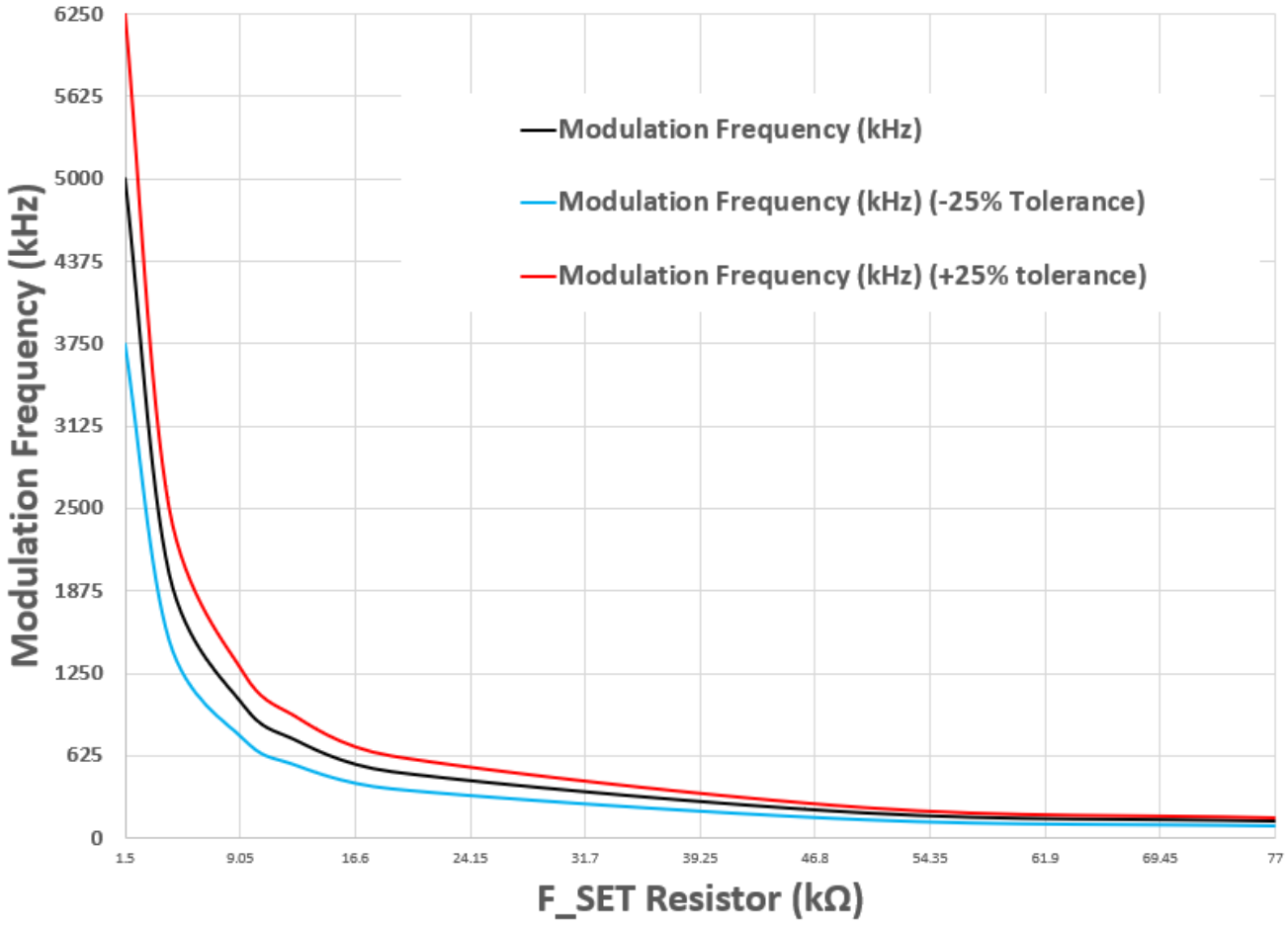


Figure 2-2. THVD8000 Modulation Frequency v. Setting Resistor Value

Demodulation of OOK signals follows the same logic as modulating the signal but in reverse. The demodulator does this by using an integrated variable frequency bandpass filter, controlled via the same setting resistor as before so that is best primed to receive data at the correct frequency. One important nuance here is that the variable bandpass filter has a low-quality factor (Q_0) value which means its passband is wide – this is done because the modulator itself has a ±25% tolerance on the carrier frequency of the signal alone – so the filter itself is not the most selective and using multiple OOK frequencies on one bus can result in communication issues and is not generally advisable.

With an understanding of the modulator and demodulator; the transceiver itself can be looked at in more detail.

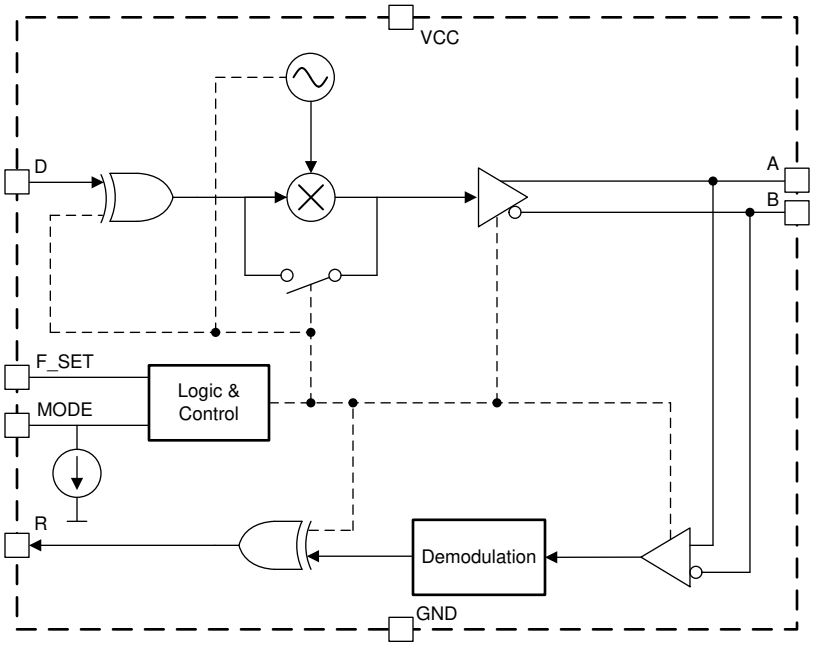


Figure 2-3. THVD80x0: Functional Block Diagram

The functional block diagram shows that Powerbus devices can be broken down into three groups. First, the digital console facing pins (D, MODE, and R) which control the device and allow for transmission to and from a controller of the transceiver. The D and MODE pins are standard logic inputs that follow other logic inputs common to Classical RS-485 devices – an input high is 2V or greater, an input low is 0.8V or less. D is the transmitted data and MODE is the control of the device – where a logic high can put the device into transmit mode while a logic low can put the device into receiver mode. Second is the modulator and demodulator – this is where the OOK modulation and demodulation scheme are physically integrated into the part, they function as previously described. Finally, the actual transceiver bus facing pins A and B. This front end is RS-485 compliant in everything except its input thresholds (due to the modulation scheme) so it won't negatively impact a Classical RS-485 bus – but it will not be able to communicate with the other devices on the line.

Arguably one of the most important aspects of Powerbus design is the external coupling network – as this is what allows power and data to transmit on the same bus.

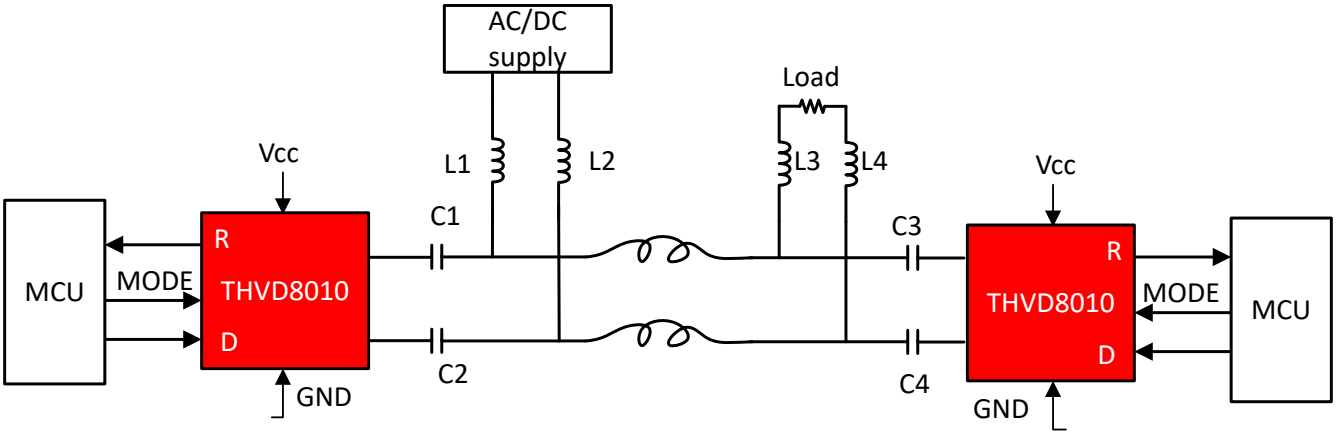


Figure 2-4. THVD80X0 Simplified Schematic (THVD8010 Shown)

Each node's coupling network consists of 2 capacitors and 2 inductors. In the simplified THVD80X0 schematic with THVD8010 shown has C1, C2, L1, and L2 represent the first THVD8010's coupling network while L3, L4, C3, and C4 represent the second THVD8010's coupling network. At a high level the idea behind the shared bus is that of Frequency Division Multiple Access (FDMA) – where the data signal is at a much higher frequency than that of the power signal (which is either going to be 0Hz (DC) or low frequency AC (50Hz – 60Hz)) and

the intended load for each target can filter the unwanted signal out. In practice this means the capacitors in the network should be low impedance to the THVD8000 or THVD8010 but high impedance for the power signal to allow the transceiver to only interact with the data signal itself. Conversely the inductors need to be low impedance for the power signal to conduct through without much attenuation while being high impedance to the OOK data signal to prevent the transceiver from being overloaded and to help prevent noise on a power source or load. It is assumed the power sources and power loads have bulk capacitance to help create an *AC* ground for the OOK signal – this is an important consideration when working with AC power supplies versus the simpler DC power supplies. The capacitors and inductors are sized according to the following equations which assume the system is properly terminated (two 120Ω terminations, one at each end node).

$$C_{min} = \frac{1}{2 \times \pi \times f_{mod} \times 5\Omega} \quad (1)$$

$$L_{Min} = \frac{1}{\left(\frac{1}{375\Omega} - \frac{N}{R_{in}}\right) \times \frac{2 \times \pi \times f_{mod}}{N}} \quad (2)$$

The capacitor sizing sets the capacitor to be at 5 Ω at modulation frequency for the minimum allowable capacitance on each node. If this process is not followed, the data signal can suffer from higher attenuation. This value can be lower than 5 Ω, but not higher.

The inductor sets the minimum effective inductance value per inductor used (for example, if you had 2 nodes and 4 inductors each one needs at least L_{Min}). N is the number of other Powerbus nodes on the same bus. For small values of N, the inductance value is not affected by transceiver loading that strongly, but as N grows larger, it becomes an important part of the calculation. This keeps the common mode loading of the bus to be equal to or greater than 375 Ω which represents the approximate common mode loading of 32 Unit Loads – which is the maximum allowable by RS-485. This equation only gives the effective inductance – as the power supply current can cause derating – it is critical to make sure the effective inductance is at this level during operation. Other inductor parameters are determined by the power system needs – not that of the THVD8000 or THVD8010.

The coupling network ultimately works as a filter while the modulation scheme is the one that allows robust communication on the same line as a power signal. This network is not needed for the THVD8000 or THVD8010 to operate, but to protect itself from potentially damaging power signals and preventing bus overload.

This is not an exhaustive list of potential modifications with Powerbus, but the list does show the basic design principle behind a standard Powerbus application.

3 Powerbus vs. Classical RS-485

How is Powerbus different from Classical RS-485? With the same bus facing architecture as a standard RS-485 device with similar electrical characteristics Powerbus and Classical RS-485 share many of the same features. However, even with a large degree of similarity between the standards they are unable to communicate with one another. This section will guide the end user on how to navigate the similarity and differences between these similar types of devices.

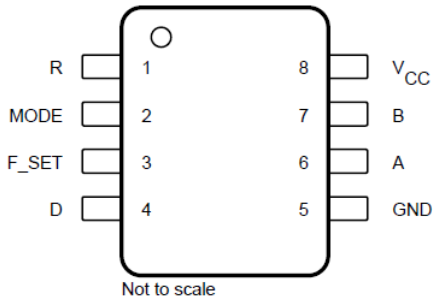


Figure 3-1. Powerbus Standard Pinout

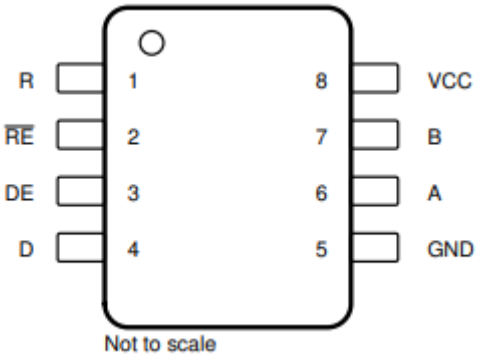


Figure 3-2. Standard Pinout for 8-Pin Half Duplex RS-485 Transceivers

Since both Classical RS-485 and Powerbus share a similar bus facing architecture as well as a similar controller facing architecture the standards will have a few commonalities. When looking at the controller side pins there are two pins that function equivalently between the two standards – that being the “D” and “R” pins. R sends single ended data signals to the controller when the receiver is active and high-z otherwise. While D transmits single ended data onto the differential bus. Standard VIH (min) is 2V and VIL (max) is 0.8V between Most Classical RS-485 and Powerbus.

The mode pin on the THVD8000 is equivalent to the /RE and DE pins if they are shorted together. A logic low of MODE = THVD80X0 in RX Mode and a logic high on MODE = THVD80X0 in TX Mode. All of these pins allow the controller to determine the flow of data either coming to the controller or flowing away from the controller. The key distinction being that the THVD80X0 does not have a true disabled state due the MODE pin only allowing for 2 distinct but active modes – whereas Classical RS-485 with enables will allow for shutdown/disabled mode of the device with an active VCC level. It should be noted that the enables are not explicitly defined in RS-485 standard, but are a very common aspect of many RS-485 devices and the Powerbus family is using a less standard method of control to allow for additional functionality in that of the F_SET pin. The F_SET pin is used to set modulation frequency with a resistor to ground – to keep Powerbus in a typical 8-pin package common to RS-485 the control pins had to be moved into a single control pin.

The similarities do not end with the console facing pins. The power pins are equivalent, but more interestingly – so are bus facing pins. The bus interface will conform to all of the RS-485 required specs except for 1 – which is the differential input thresholds. Powerbus devices have the same drive strength, loading as a 1/8 unit

load device, common mode input voltage range, and short circuit current limit to name a few key specifications. Ultimately what this means is that the THVD80X0 line of devices, if placed onto a standard RS-485 bus will not cause damage and not receiver damage under normal operating conditions. Due to Powerbus's inability to disable the transceiver without cutting power to the device external methods of separation may need to be utilized if working with both types of devices on a board.

As previously mentioned the one specification that Powerbus is not aligned with for RS-485 are the input thresholds. This is largely due to the modulation scheme implemented by the THVD80X0 line of devices. In Classical RS-485 -200mV and less is a logic low and 200mV or higher is a logic high – this is the base line for input thresholds. Powerbus devices can't use this logic as a logic high is ideally 0V and a logic low is going to alternate between positive and negative values. What this means is that for older RS-485 systems without integrated fail-safes if the THVD8000 sends a logic 1 it will be read as undefined by the Classical RS-485 device. If the RS-485 system is using modern transceivers with integrated fail-safes then a logic 1 will actually be read as a 1 as 0 V are read as logic one on more modern devices. However, on older and modern RS-485 transceivers if a logic 0 is sent from the THVD8000 the Classical RS-485 transceiver will read that as an alternating bit pattern with a data rate of 2 × Modulation frequency. Assuming that the transceiver is rated for the higher data-rate, the data read will not be correct. If this though experiment is flipped to where the THVD80X0 device is receiving data – the THVD80X0 family of devices looks at signal magnitude and it also passes the signal through a bandpass filter – so the data signal will either look like a solid string of 0's or like nothing is being transmitted at all due to the signal being rejected by the internal bandpass filter. It can be thought that Powerbus devices and Classical RS-485, while very similar, do not speak the same language and can't be used to communicate to one another.

4 Guidelines for a Combined System

With an understanding of the basic differences between Classical RS-485 and Powerbus it has been shown that the device cannot communicate with one another, but will not directly harm one another if communication does occur between devices. However, this presents a unique issue for designers of large networks of communication nodes in factory and/or building automation use cases where the designer may not have full control over every node in the system, but Powerbus would help significantly reduce system overall cost due to halving cabling costs. Traditionally this means the designer would implement Powerbus on internal projects where they had full control over the network and implement Classical RS-485 otherwise while having to suggest a more expensive solution to the customer until the designers of the other nodes decided to move towards Powerbus for the significantly cheaper implementation – if they do at all. This creates a situation where multiple boards will need to be designed to fit multiple niches and upgrading a system from Classical RS-485 to Powerbus would require a completely new board design. However, there is a quicker approach – a dual use board that can be configured to work as Powerbus or Classical RS-485. The remainder of this note will cover the original design parameters, schematic design, and finally a proposed layout of what a universal board could look like and the benefits and trade-offs of pursuing this type of application.

Powerbus is very flexible in its design. To be able to show an illustrative example the parameters of the design were fixed to the following requirements.

Parameter	Requirement
Main Power Rail	36 V DC
Max Current from Power Rail	3 A
Total Number of Power Nodes	4
Device VCC	5 V or 3.3 V
Modulation Frequency	5 MHz

Using the equations from section 1 it yields us the following results. The minimum series capacitance is 6.4nF – so any capacitance 6.4nF or larger should work, so for this design 1uF capacitors will be chosen. To avoid too much derating due to voltage 50V to 100V ceramic capacitors should be chosen – in general the max voltage across capacitor multiplied by 2 is a good voltage rating to have to avoid derating on ceramic capacitors. One thing to note is that capacitors of 255nF or larger can work in any Powerbus application regardless of modulation frequency in DC systems - in AC systems the capacitance value matters much more as the AC signal will conduct through the series capacitor. The minimum effective inductance per node (since there are 4 nodes – there will need to be 8 inductors) will be 48.5uH of effective inductance per power node connection. It is important to consider the saturation current of the inductor – as depending on inductor manufacturer the saturation current is the current needed to decrease inductance by either 10%, 20%, or 30% of nominal value – so while the power supply current doesn't matter to the Powerbus device – it will matter to the inductor portion of the coupling network. With the Powerbus parameters discussed the joint schematic design can now be analyzed.

Classical RS-485 system design is much more simplistic that Powerbus – so this joint schematic would work for any device in an 8-Pin SOIC package – which is the most common package for Half-Duplex RS-485 transceivers. The Combined design can be thought of in three distinct parts: the power connections, single ended I/O, and the direct transceiver interface.

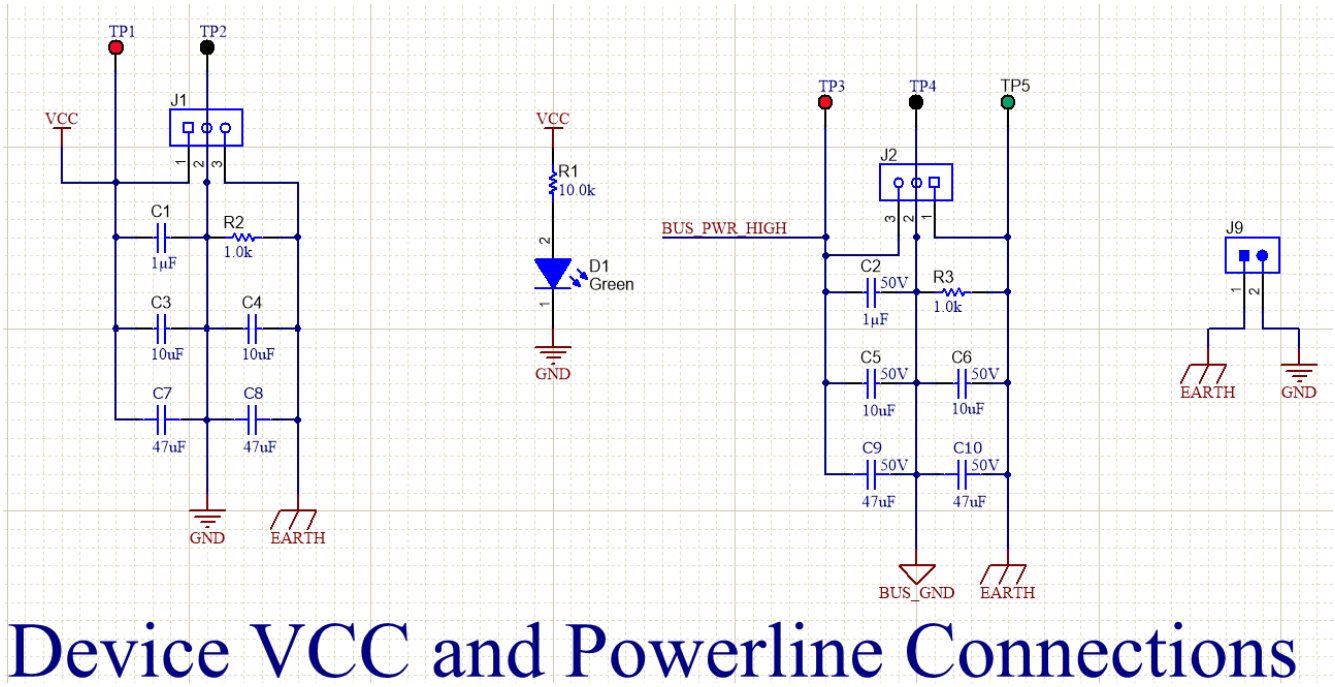


Figure 4-1. Generalized Power Input Schematic

The power connections comprise themselves of two terminal block/test point inputs for the device VCC and in case of Powerbus the main power line that will comprise half of the signals on the shared bus. They are both constructed in the same way – a simple three prong input (Live, Neutral/GND, and Earth/Chassis Connection) with J1 for device VCC and J2 for the higher power signal. They both contain bulk capacitance between positive and negative terminals of source with the additional option of having additional capacitance between negative terminal of power supply and an EARTH/Chassis connection. The bulk capacitance is not necessary for the device VCC, but bulk capacitance is assumed to exist on the power source and loads by the Powerbus devices. The values of capacitance can change depending on exact use case. There is also the option included with a resistor from GND to EARTH to reduce ground loop current and therefore decreasing risk of noise issues. Beyond the power inputs there is also two more features, an LED indication light for device VCC and a shunt between GND and EARTH if an Earth connection is not present in the system. Depending on exact use case is what determines connections.

Component	Classical RS-485	Powerbus	Comment
J1	Device VCC Input	Device VCC Input	Accepts 3.3V to 5V
TP1	Device VCC Input + Terminal	Device VCC Input + Terminal	Same between use cases
TP2	Device GND Input	Device GND Input	Same between use cases
J2	Not Used	Power Line Input	Only used in Powerbus
TP3	Not Used	Power Line “Live” Input	-
TP4	Not Used	Power Line “Neutral” Input	-

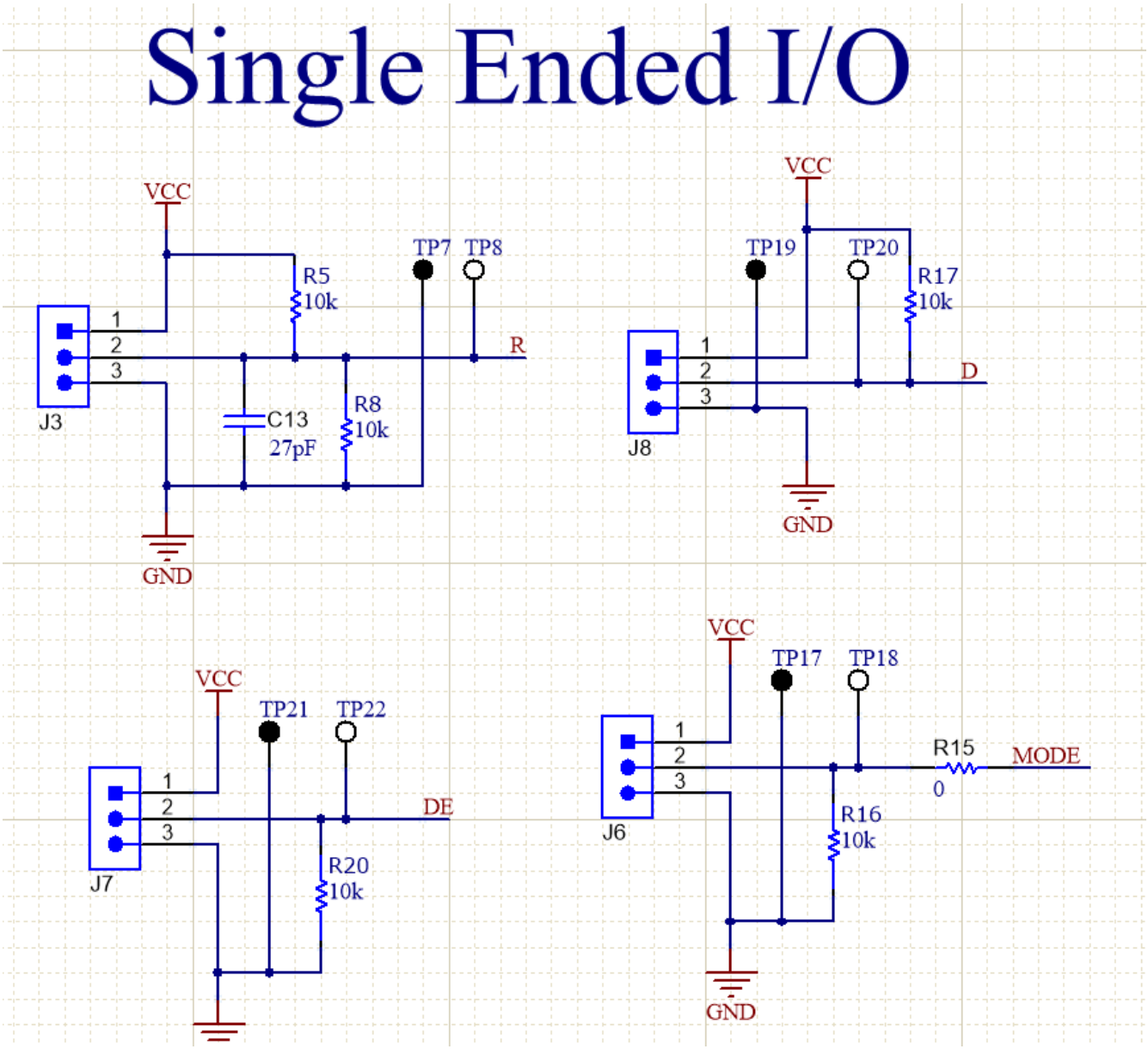


Figure 4-2. Generalized Single Ended I/O Schematic

After the power connections, the next concern is single ended I/O. Luckily as discussed previously the D and R pins function identically between Classic RS-485 and Powerbus. In the most use case R and D can be directly connected to the controller of the wired communication subsystem – however loading, pull-ups and pull-down resistors can be implemented. The “R” pin above, attached to J3, has options for a pull-up, pull-down, and / or capacitive load – where a common use case would be to have a pull-up resistor and a capacitive load so an Idle state is always read as “high”- this is very common with the UART protocol. The D pin, attached to J8, shows an option of a pull-up resistor to ensure a guaranteed level at startup. It is always best practice to have a predefined “default” state on logic inputs to prevent glitching at the output – but it doesn’t have to be a pull-up as it could also be a pull-down resistor. The two other signals a bit more involved on a combined board. First looking at the DE signal, attached to J7, it is important to note that this input is only used for Classical RS-485 subsystems as the Powerbus devices do not have a DE pin. Finally, the “MODE” input on J6 is going to change its operation based on what type of application is being used. In Powerbus applications the input at J6 will be used to switch the mode (either RX (logic low) or TX (logic high)) of the transceiver and in Classical RS-485 this input is used to turn the receiver on (logic low) or off (logic high).

Component	Classical RS-485	Powerbus	Comment
J3	R Pin Single Ended Output	R Pin Single Ended Output	No difference between standards
R5	Optional Pull-Up	Optional Pull-Up	No difference between standards
R8	Optional Pull-Down	Optional Pull-Down	No difference between standards
C13	Optional Capacitive Load	Optional Capacitive Load	No difference between standards
J8	D Pin Single Ended Input	D Pin Single Ended Input	No difference between standards
R17	Optional Pull-Up	Optional Pull-Up	No difference between standards
J7	Driver Active High Enable (DE) Control Signal Input	Not Used	DE only exists on Classical RS-485 with Standard Enables
R20	Optional Pull-Down	Not Used	DE only exists on Classical RS-485 with Standard Enables
J6	Receiver Active Low Enable (/RE) Control Signal Input	Mode (Mode) Control Signal Input	/RE only controls RX; Mode controls RX and TX
R16	Optional Pull-Down	Optional Pull-Down	Pull-Down can exist in both standards.

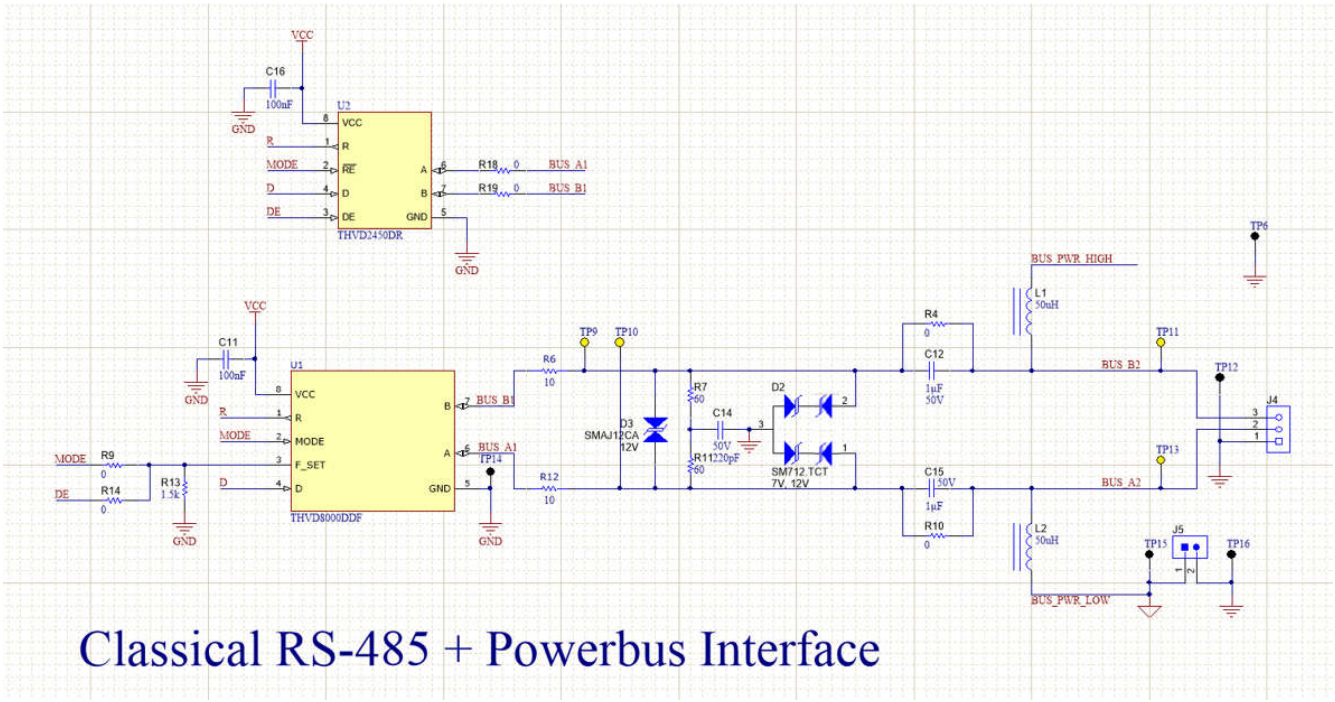


Figure 4-3. Classical RS-485 + Powerbus Interface Schematic

Finally, the most important aspect of the combined Classical RS-485 and Powerbus is the transceivers themselves. This can be broken down into three sections – the power connection, the single ended inputs (controller facing pins), and the differential bus facing pins.

The power pins have largely already been covered previously the only adjustment is that it is required that at least 100nF of decoupling capacitance is added close to the VCC pin of the IC – this is true for both the THVD8000/THVD8010 and most other modern RS-485 devices (older devices may suggest larger capacitors such as 1uF – but most modern devices will be at 100nF) – since the board has two distinct IC footprints two 100nF capacitors were used – one by each devices VCC.

Next the single ended signals have also been largely covered – however there is an important consideration with respect to the MODE, DE, and F_SET pins between Classical RS-485 and Powerbus. The input of the Mode signal will lead to the MODE pin of the THVD8000/THVD8010 and the /RE pin of the Classical RS-485 device. In applications where the Classical RS-485 device has DE and /RE shorted together, resistors R9 and R14 can be added to create a short between these pins. When using this in Powerbus mode the resistors R9 and R14 should be removed as DE is not present in Powerbus and there are no direct inputs onto F_SET for a Powerbus application. This leaves the F_SET pin – which is unused in Classical RS-485 systems, but would be utilized in

Powerbus applications by applying a resistor to device GND -the resistor chose, R13, is at a value that will set the modulation frequency to 5MHz.

Lastly, the bus pins can be discussed. Ideally Classical RS-485 has two terminations between A and B in the system (120Ω each) with the only other circuit components being protection diodes, EMI mitigation, and/or biasing resistors; whereas Powerbus has that plus the coupling network to contend with. The first issue that may be noticed is the trouble that a Classical RS-485 transceiver will have communicating over the series capacitance; while this technically can be done it generally requires an encoding scheme that will reduce overall throughput of the system while increasing complexity of the data transmission. To get around this potential issue the board gives an option of a resistive series connection or a capacitive one. In Powerbus the capacitors would be installed while the 0Ω links would not be installed and vice versa for Classical RS-485. The next primary concern is that of the inductive coupling – technically speaking common mode inductance towards an “AC” ground reference is not expressly forbade by RS-485 standard, but minimum common mode impedance to ground is alluded to in the standard. Once again – this value is approximately 375Ω. Since the inductor’s impedance is based on frequency and there is no guarantee that the base frequency component of the unmodulated RS-485 datastream is going to maintain the correct frequency to prevent overloading on the bus without additional encoding schemes, is going to create a mismatch between overall bus loading between Classical RS-485 and Powerbus. This can be resolved by just keeping pads available for the inductors when Powerbus is needed and do not populate otherwise. The other components largely comprise of what is suggested for both Classical RS-485 and Powerbus – including a split termination, protection diodes, and a resistive link between Classical RS-485 and Powerbus connections that can be implemented when using Classical RS-485.

Component	Classical RS-485	Powerbus	Comment
R9	Install if both control pins are controlled via 1 signal	Do Not Install	-
R14	Install if both control pins are controlled via 1 signal	Do Not Install	-
R6 and R12	Optional Pulse Proof Series Resistors	Optional Pulse Proof Series Resistors	Protects input pins during surge/ transient before protection diodes begin to conduct
D3	Bidirectional Protection Diode (+/-12V)	Differential TVS Protection Diode	Protects with Reference to Differential Wire
D2	Dual Channel Bidirectional Protection Diode (-7V/12V)	Dual Channel Bidirectional Protection Diode (-7V/12V)	Protects with Reference to Device GND
R7, R11, and C14	Split Termination – EMI mitigation; can use 120Ω resistor instead	Split Termination – EMI mitigation; can use 120Ω resistor instead	Split termination helps filter off common mode noise
C12 and C15	Do Not Install	Install	Series Coupling Capacitors for Powerbus
R4 and R10	Install	Do Not Install	-
L1 and L2	Do Not Install	Install	-

With an understanding of the schematic and how to use under which circumstances a possible layout can be constructed.

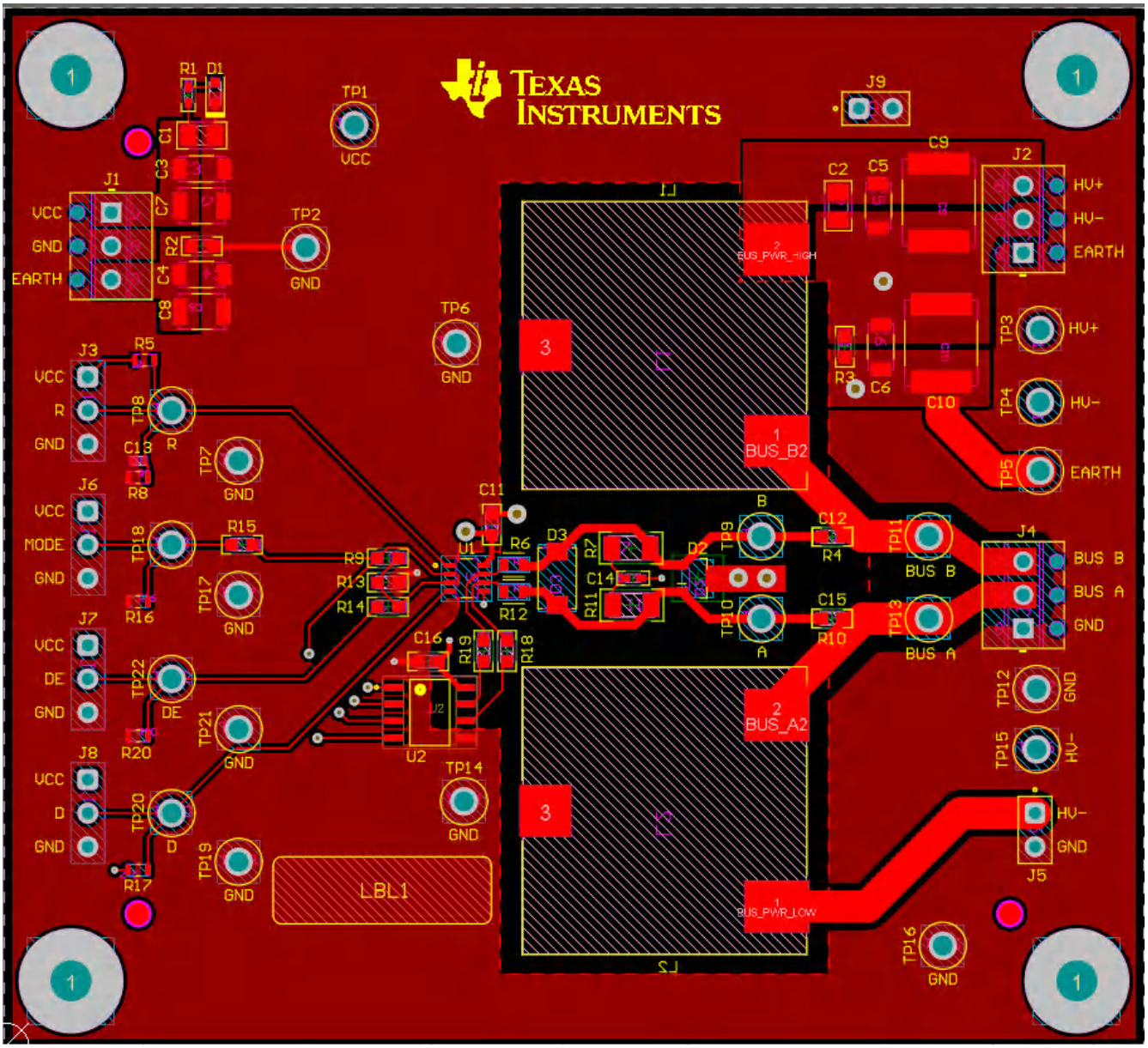
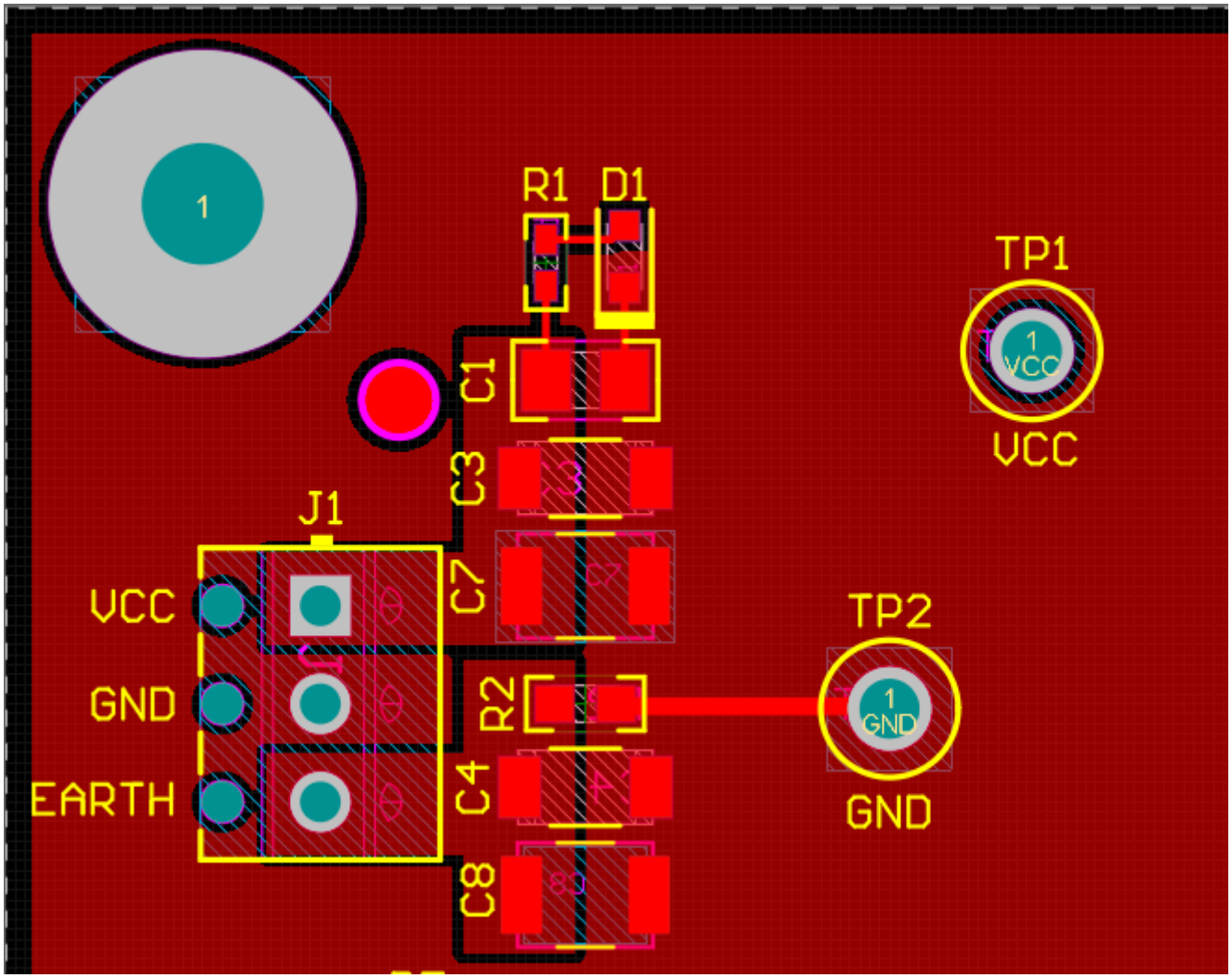
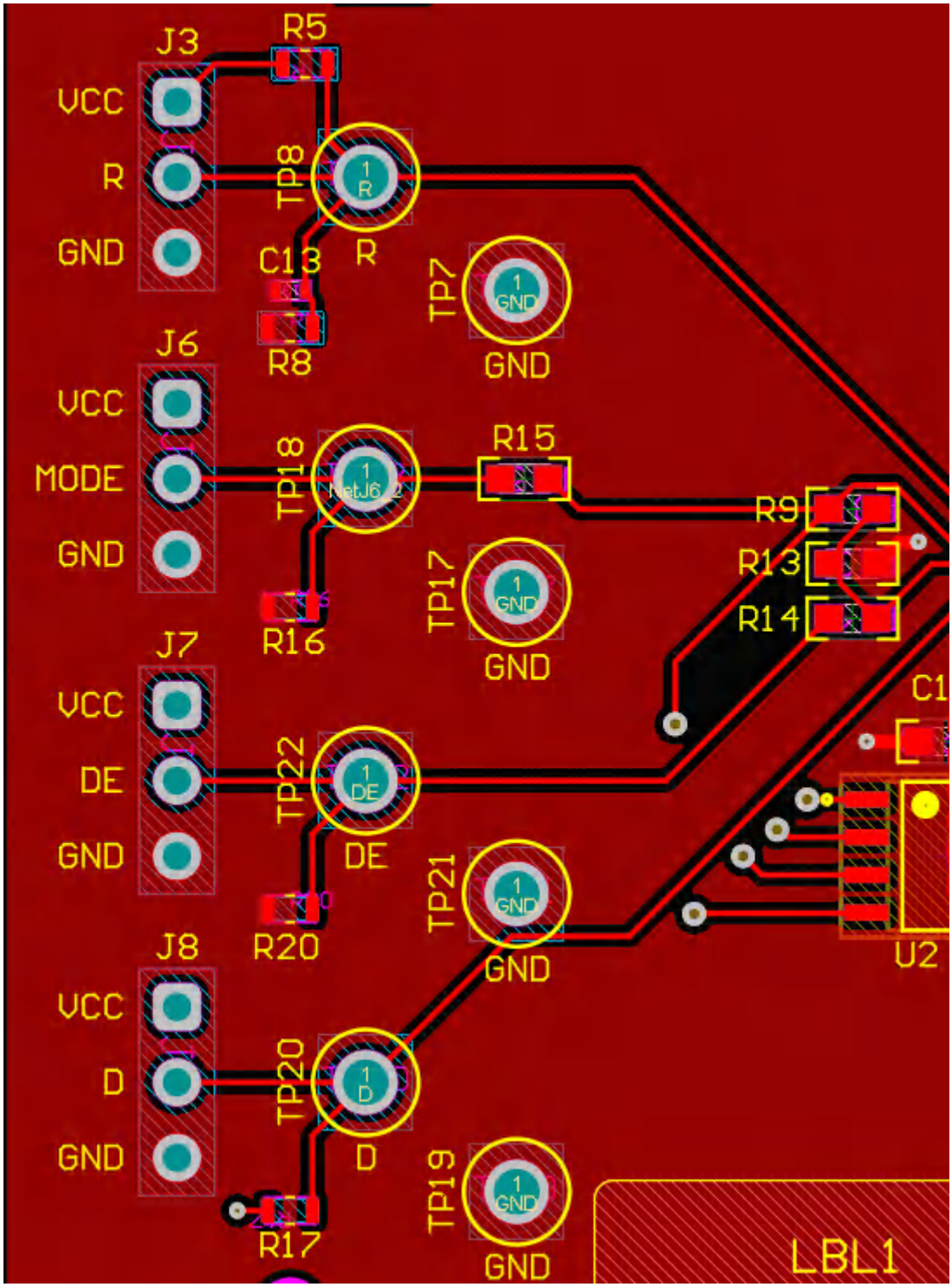
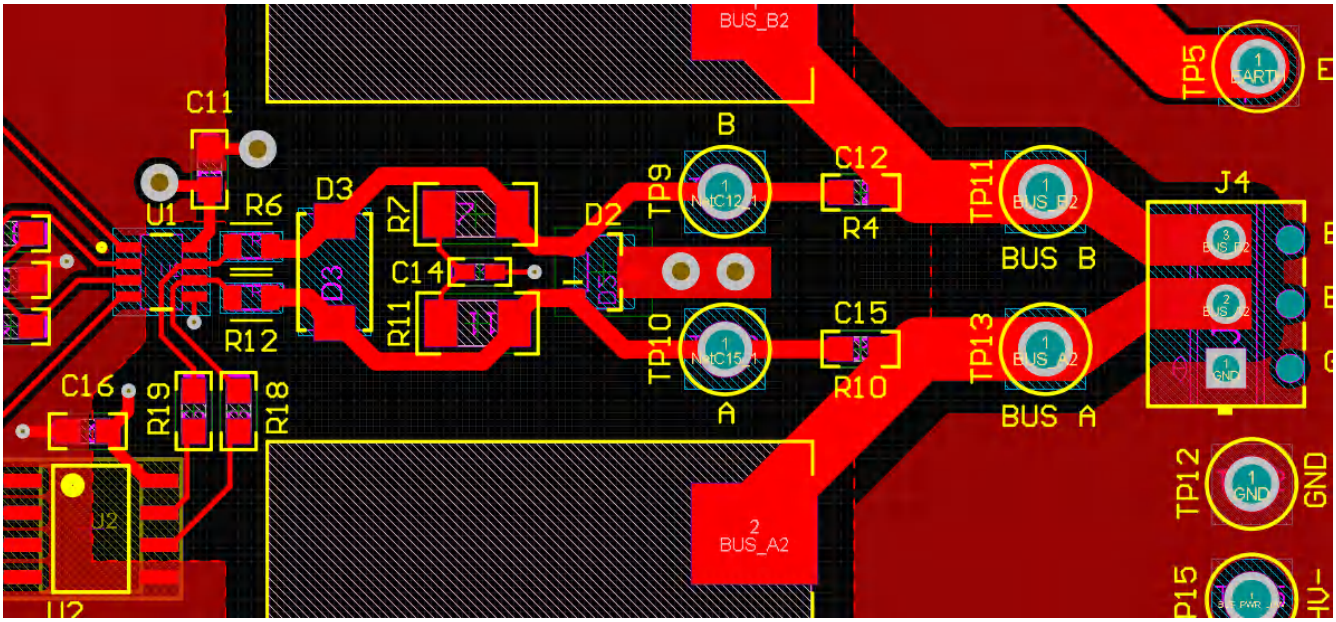


Figure 4-4. Example Layout - Top Layer







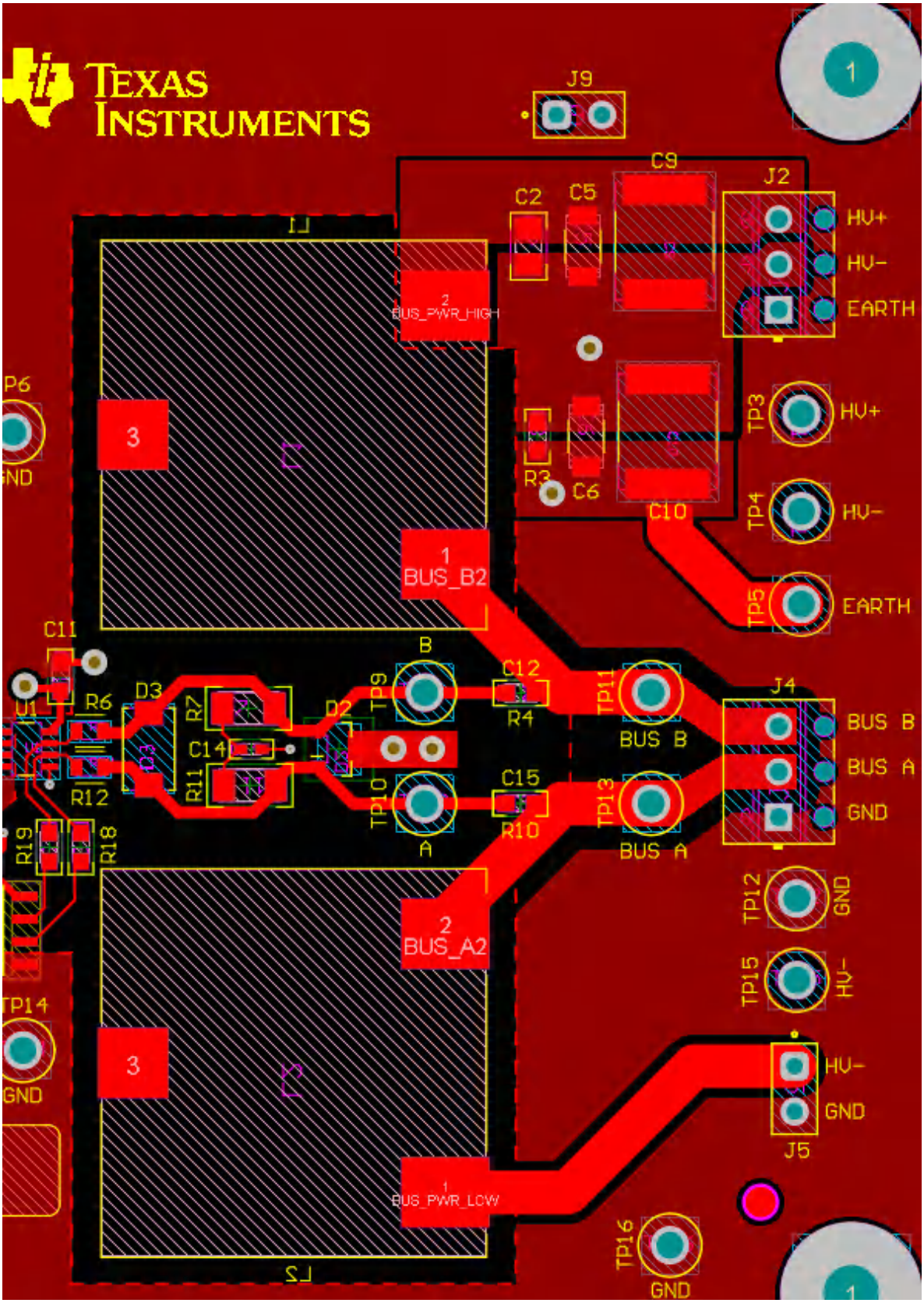


Figure 4-5. Close Up of Layout for IC PWR, IOs, Differential Bus, and High Power Interface

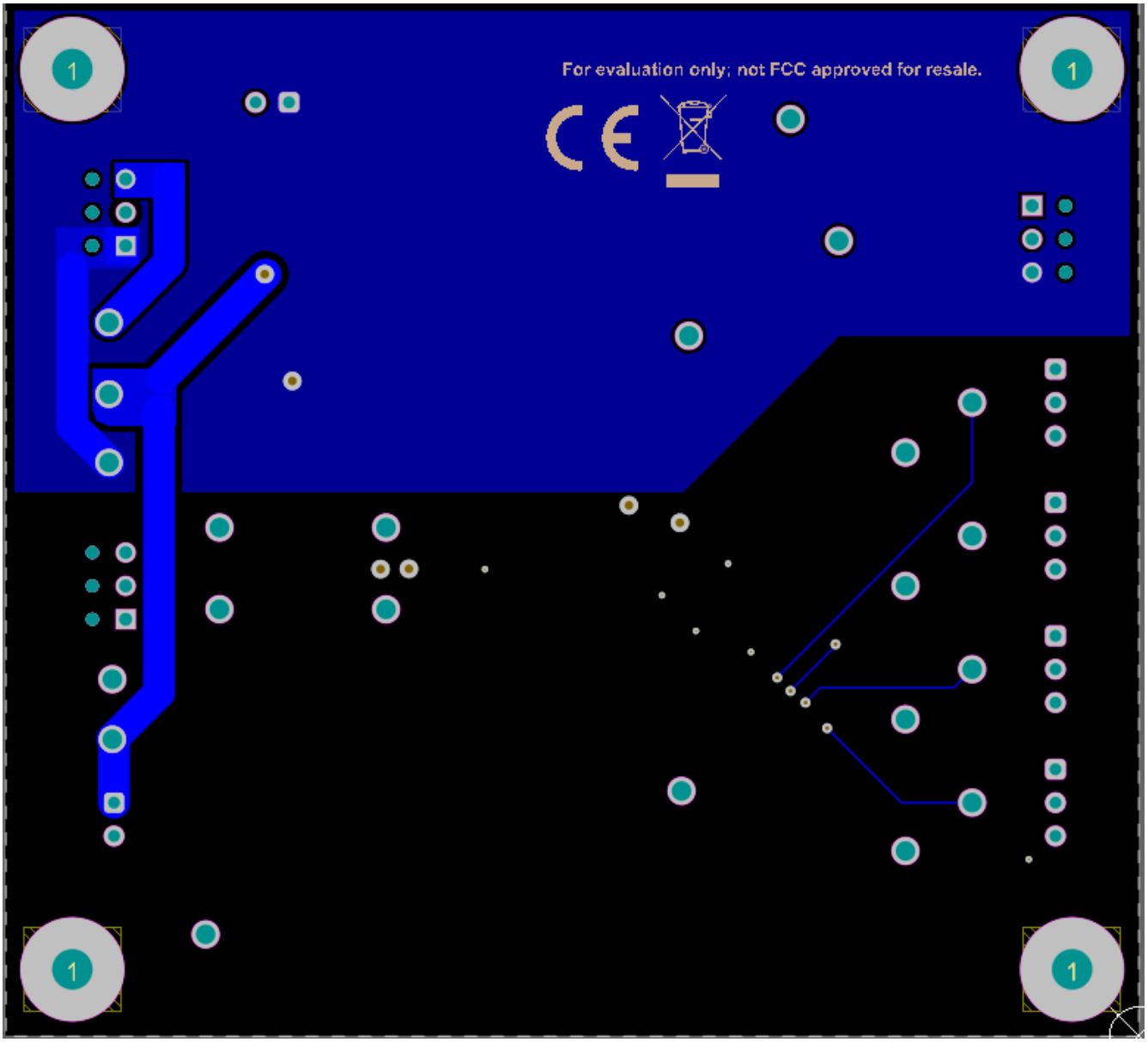


Figure 4-6. Example Layout - Bottom Layer

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	SM-001	1.00mil	4	
3	Top Layer	Copper	1.38mil		
4	Dielectric 1	PP-017	5.10mil	4.3	
5	Dielectric 2	PP-017	5.10mil	4.3	
6	Int1 (GND)	Copper	1.38mil		
7	Dielectric 3	Core-039	28.00mil	4.8	
8	Int2 (PWR)	Copper	1.38mil		
9	Dielectric 4	PP-017	5.10mil	4.3	
10	Dielectric 5	PP-017	5.10mil	4.3	
11	Bottom Layer	Copper	1.38mil		
12	Bottom Solder	SM-001	1.00mil	4	
13	Bottom Overlay				

Figure 4-7. Example Layout - Layer Stackup

The layout uses a 4-layer board to keep device VCC and GND internal to the board for ease of routing – this is not required – but can make layout easier.

With a layout and schematic, a semi-universal board is created. The benefits of which allow a single design for multiple systems. The largest tradeoff comes with solution size and Powerbus variability. Classical RS-485, due to the lack of inductors, generally will offer a smaller solution size. In space limited applications a purely Classical RS-485 approach is most likely needed. The other main tradeoff is the needs of power bus – the inductance value and size can greatly vary depending on needs of the application or end equipment – for a truly universal board inductors should be chosen at 256 nodes at 125KHz modulation with worst case power supply current considered – as this type of board will work in any power bus application at the cost of the largest solution size due to the large inductance values.

5 Summary

Classical RS-485 and Powerbus both have their place amidst an ever-changing landscape of industrial applications and end equipments. While these standards cause devices to speak slightly different languages that are unintelligible to one another it still may be worthwhile to have a dual use board that can be applied to multiple systems regardless if they are Classical RS-485 or Powerbus to either act as a universal board or as a stop gap while the rest of the systems nodes are upgraded to be Powerbus capable. This application note gave a generalized overview of a potential solution – one other solution could be to implement switches every place there is a 0Ω link and at the inductive coupling to allow for a fully populated dual use board.

6 References

- Texas Instruments, *The RS-485 Design Guide* application note.
- Texas Instruments, THVD24x0 ±70-V Fault-Protected 3.3-V to 5-V RS-485 Transceivers With IEC ESD data sheet
- Texas Instruments, THVD24xxV ±70-V Fault-Protected 3 V to 5.5 V RS-485 Transceivers with Flexible I/O Supply and IEC ESD data sheet
- Texas Instruments, THVD8000 Design Guide application note.
- Texas Instruments, THVD8000 EVM User's Guide user's guide.
- Texas Instruments, THVD8000 RS-485 Transceiver with OOK Modulation for Power Line Communication data sheet.
- Texas Instruments, THVD8010 RS-485 Transceiver with OOK Modulation for Power Line Communication data sheet.

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