Application Note

Why use a Gate Drive Transformer?

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ABSTRACT

There are several different options available to drive the gates of high-voltage power switches used in a variety of applications such as HEV/EV DC/DC converters and server PSU 400V to 48V DC/DC converters. One option is to use a transformer-coupled gate drive design using a non-isolated gate driver such as UCC27624 and a discrete transformer.

A gate drive transformer brings some benefits compared to alternatives. However, there are unique design considerations that are important to understand when implementing a gate drive transformer. This document covers the system-level benefits to transformer coupled gate drive, as well as the design considerations required to implement them.

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Trademarks

1 Introduction

Switching converters operating at over 400V are commonly used in electric vehicles, server power supplies, appliances, and communications equipment. Half-bridge based topologies require a gate driver IC that can be referenced to the switching node, which matches the bus voltage of the converter. Today, there are many options for gate drive ICs that can drive 400V, 800V, and even higher voltage FETs and IGBTs. Gate drive ICs can accomplish high blocking voltage with *junction isolation* which uses a built-in, high voltage FET to level-shift the low-voltage input signal to the high-voltage output. Alternatively, there are isolated gate drive ICs which use various methods to transmit an AC control signal while blocking DC voltages.

Before gate driver ICs which integrated high-voltage level-shifting or isolation existed, the only option for high-voltage gate drive was to build circuits with discrete elements. One common way to achieve high-voltage gate drive was to use a transformer in the gate drive loop (also called a gate drive transformer). Physically small transformers that can transfer a square wave of a PWM signal with minimal distortion were used. These transformers are called *pulse transformers*, and also see use in communications and other applications.

Level-shift gate driver ICs and isolated gate driver ICs have become very popular, and many applications which used to use gate drive transformers have switched to using half-bridge or isolated gate driver ICs. Despite the existence of these half-bridge or isolated gate driver ICs, there are still benefits to using a gate drive transformer in conjunction with non-isolated gate driver ICs that make people use them to this day.

2 How a Gate Drive Transformer Works

There are many ways to configure a gate drive transformer, but the most common is the push-pull type shown in Figure 2-1.

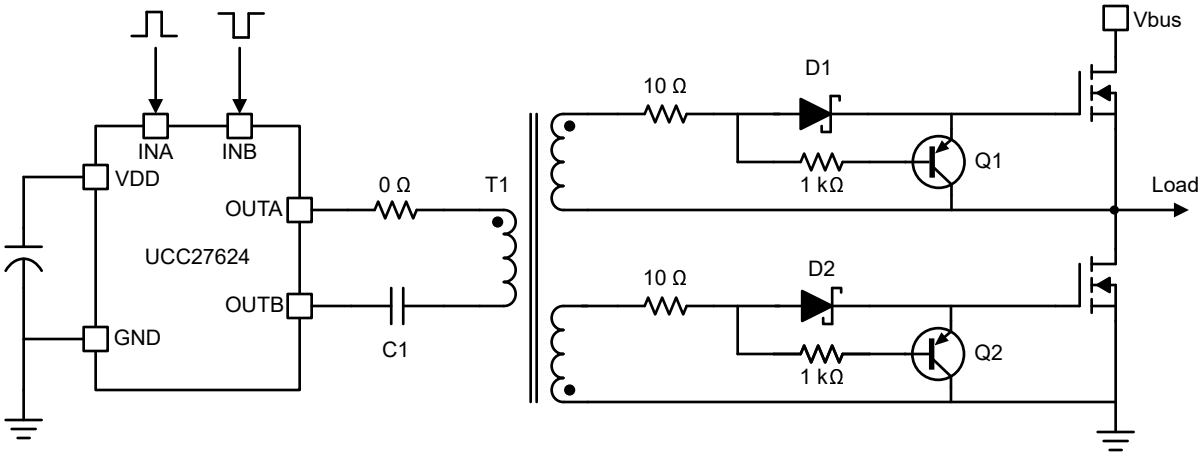

Figure 2-1. Example Schematic of a Push-Pull Gate Drive Circuit Used to Drive a Half-Bridge

In this configuration, a dual-channel low-side driver is used with a pulse-transformer to drive a high-voltage half-bridge. In Figure 2-2, the internals of OUTA and OUTB are separated to show the functionality.

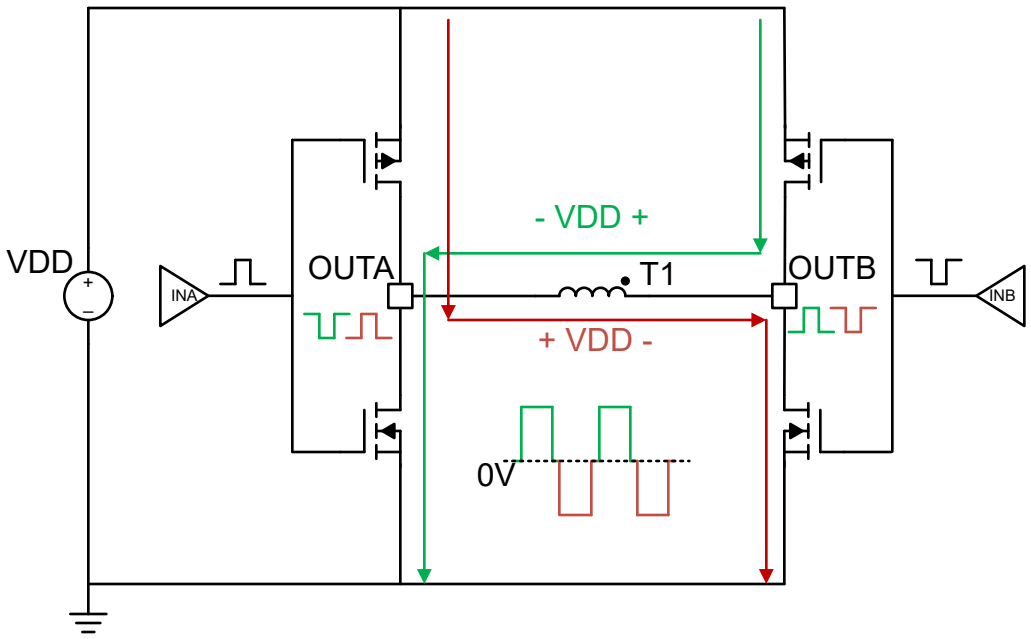

Figure 2-2. Simplified Schematic Showing Current Flow Through the Driver Output Stage in a Push-Pull Topology

By toggling OUTA high and OUTB low, and vice versa, a square wave of $\pm V_{DD}$ is created across the primary side of the pulse transformer. Note the dot notation in Figure 2-1 ; when the voltage across the primary is positive, a corresponding positive voltage is created on the high-side branch, and a negative voltage is created on the low-side branch. When the voltage across the primary is negative, there is a positive voltage created on the low-side branch and a negative voltage on the high-side branch.

The secondary side toggles between $\pm V_{DD}$ (multiplied by the turns ratio). The negative voltage is an issue for two reasons. First, energy is wasted to pull the C_{GS} capacitance below ground, so the power dissipation in the gate drive IC and transformer is higher than needed to turn off the switch. Second, this voltage can sometimes exceed the allowable voltage ratings of the switch. This negative bias can be useful in some cases, but in many applications, negative bias is not needed.

One circuit that addresses the negative voltage issue is the PNP turn-off circuit shown in Figure 2-1. The diodes (D1 and D2) allow forward conduction to charge V_{GS} when V_{DD} is high. When V_{DD} is low, D1 and D2 block reverse conduction. After V_{DD} falls, the PNP BJTs (Q1 and Q2) turn on and sink current to pull down V_{GS} and turn off the FET. Because the PNP BJTs turn off when VDD falls to 0, but the gate only goes high when VDD goes high, this local-turn off implementation also supports the addition of dead-time.

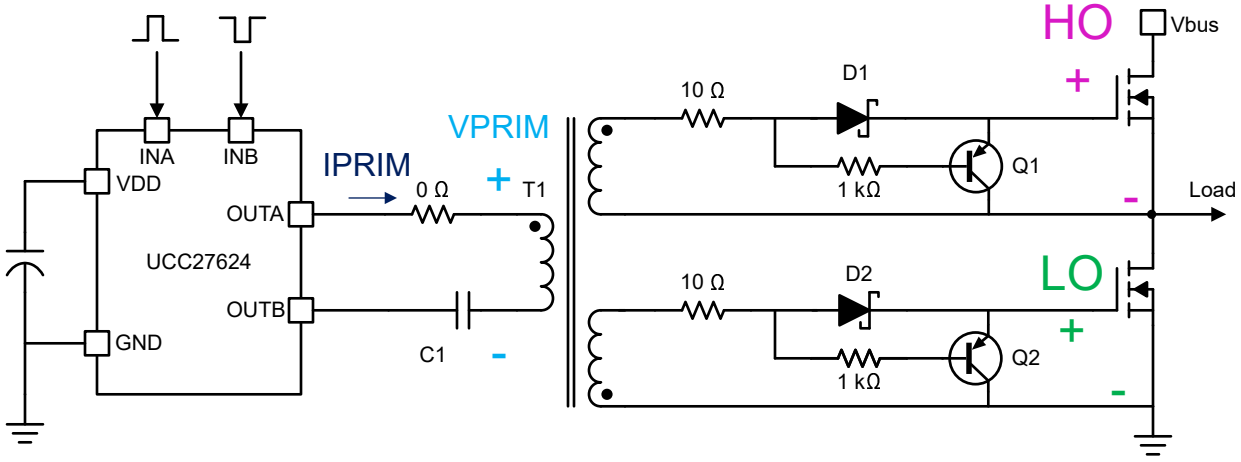

Figure 2-3. Schematic of a Push-Pull Gate Drive Circuit With Colored Labels for Primary Current, Primary Voltage, and HO and LO

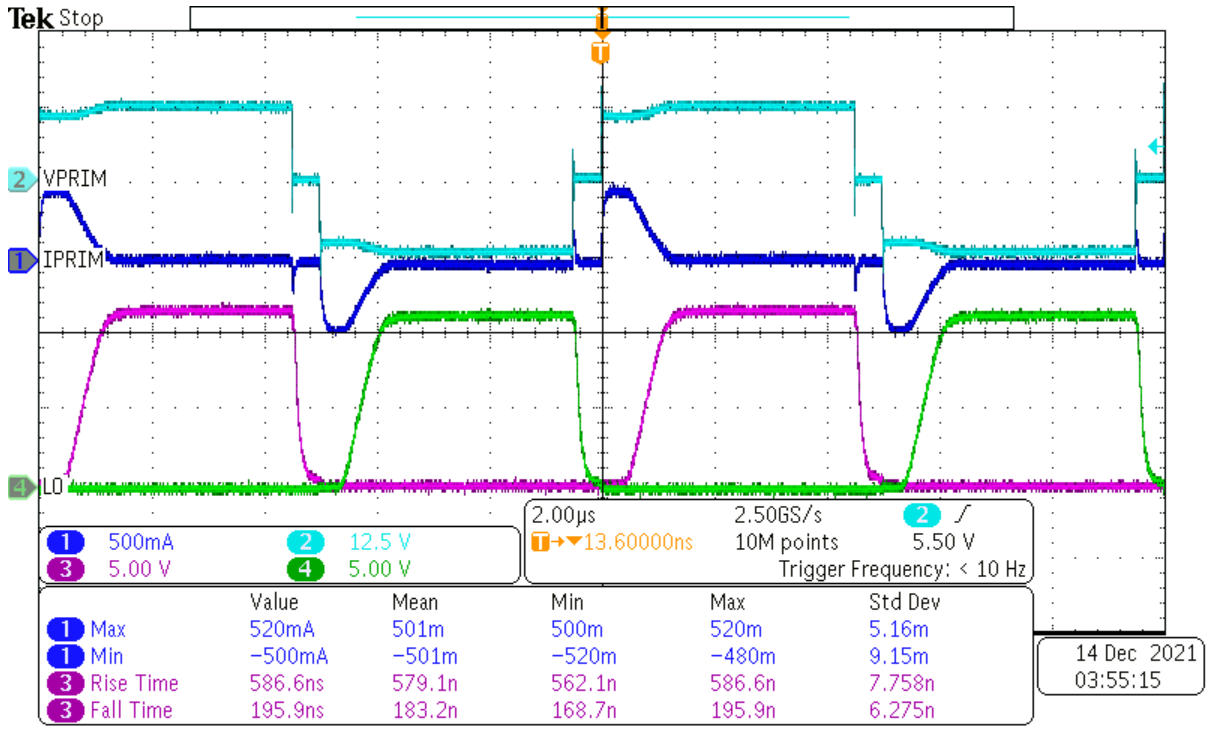

Figure 2-4. Corresponding Oscilloscope Capture to the Waveforms

The voltage across the primary toggles from ±12V, with some added dead time where both OUTA and OUTB are off. Current is transferred from primary to secondary to turn on both the high-side and low-side FET. Due to the local turn-off circuit, there is very little current transfer through the transformer during turn-off. The local turn-off circuit also allows for separate tuning of turn-on and turn-off times. In this example, the rise time was around 580ns and the fall time was around 200ns. Tunable rise and fall times enable greater slew-rate control and EMI reduction. Changing Rg allows tuning of the turn-on time, and changing RB allows tuning of the turn-off time.

Overall, the circuit shown in Figure 2-1 allows for the control of a high-voltage half-bridge using only a low-side gate driver IC, a transformer, and some extra components. There is no need for level-shifting, isolator ICs, or a bias supply as the gate drive transformer fulfills all of those roles at once.

3 Benefits of a Gate Drive Transformer

There are a few advantages to using a gate drive transformer. To summarize, gate drive transformers include the following:

- Provide galvanic isolation to the gate drive circuit
- Transfer signal and power, removing the need for a bias supply
- Enable easy negative gate bias
- Can enable a short propagation delay
- Scale voltage and current based on the turns ratio
- Allow more customization for extreme or unusual end applications

Of these benefits, one of the most notable is that the gate drive transformer eliminates the need for a bias supply. High-voltage half-bridge gate drive ICs require a floating supply to power the high-side driver. This is often done with a bootstrap circuit. In isolated gate drive ICs, a separate isolated bias supply is sometimes required to preserve the isolation barrier. The gate drive transformer can transfer the gate current from the primary side gate driver to the secondary side power switch. Because power is transferred through the gate drive transformer, there is no need for a bias supply on the secondary side. Isolated bias supplies add a significant cost to the system, so a gate drive transformer-based approach can reduce system cost.

Another benefit from gate drive transformers is the inherent negative bias provided by the push-pull topology. The PNP turn-off circuit in Figure 2-1 rectifies the bipolar gate drive signal from $\pm V_{DD}$ to $+V_{DD}$. However, omitting the PNP turn-off circuit allows for a $-V_{DD}$ bias during the off period. In some high-power systems, a negative

bias is applied to the power switch to improve immunity to miller turn-on. When the switch node transitions between high and low states, a parasitic current is injected through the C_{GD} capacitance, also known as *Miller capacitance*. The injected current causes the gate voltage to increase, and can cause a false turn-on if the gate voltage exceeds the threshold voltage of the power switch. A negative bias increases the voltage difference between the gate voltage and threshold voltage, and results in higher immunity to the miller turn-on effect. Many SiC FET and IGBT data sheets recommend a negative bias to alleviate miller turn-on.

Gate drive transformers can also enable low propagation delay. The gate drive signal propagates through the transformer at effectively the speed of light. In terms of gate drive circuits, this delay can be treated as 0.

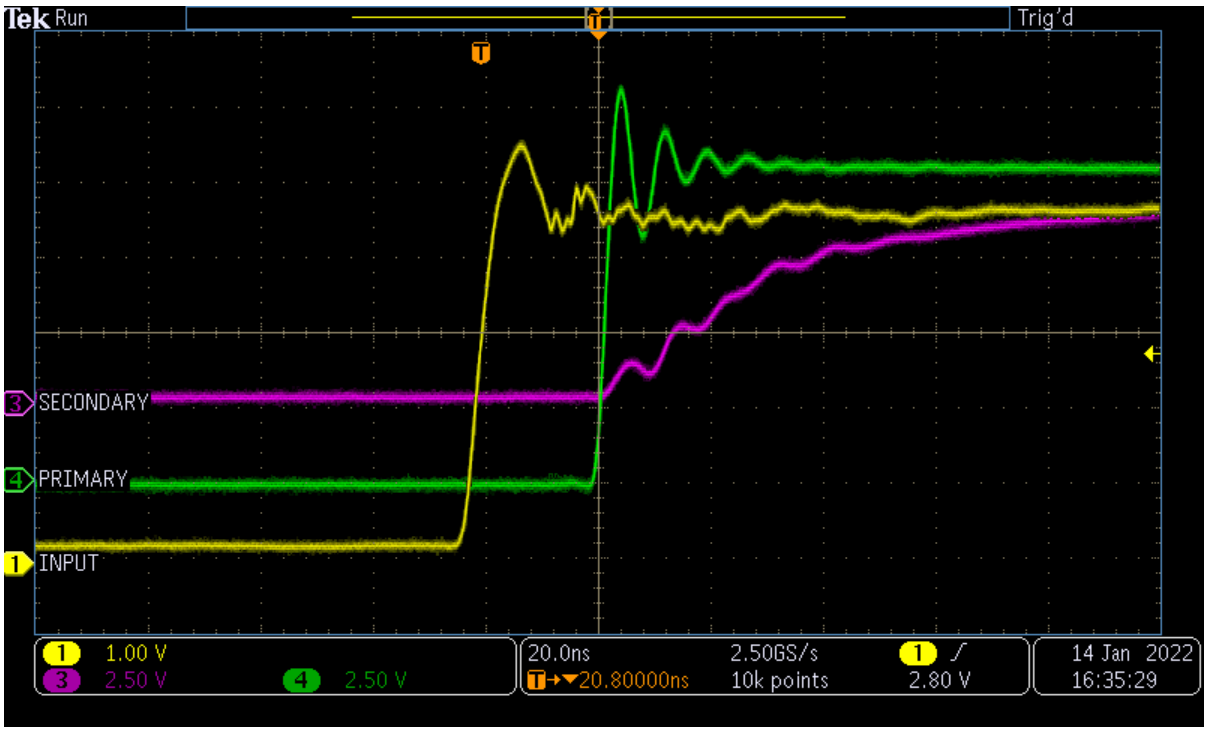

Figure 3-1. Oscilloscope Capture Showing Propagation Delay From the Driver IC and Transformer From a Circuit

The total delay comes from the propagation delay of the low-side driver IC, and rise or fall time added by circuitry on the secondary side. In Figure 3-1, the driver propagation delay appears between input and the primary voltage. However, the secondary voltage starts to rise as soon as the primary voltage is applied. The low inherent propagation delay means that gate drive transformer circuits can achieve very low propagation delays compared with other options. Other isolation methods can often use modulation techniques such as on-off keying. Any modulation and demodulation circuits can add propagation delay to the system. There are digital isolator ICs available such as ISO6521 that have typical propagation delays as low as 11ns. However, a gate drive transformer-based circuit can still be used to achieve a very low propagation delay system in applications where a fast response is necessary.

The last major benefit offered by a gate drive transformer is easy voltage scaling. The turns ratio of the transformer results in a multiplier effect on the voltage. While many designers can opt for a 1:1 turns ratio transformer, different ratios can allow for flexibility in system design. For example, a 5V bus can be used on the primary with a 1:3 turns ratio to yield a 15V gate drive voltage on the secondary. However, when voltage is scaled up, current is scaled down proportionately. In this case, the primary current can be roughly three times larger than in a 1:1 transformer system. Overall, the ability to easily scale voltages can save DC/DC converters and improve overall system efficiency and flexibility.

4 Design Considerations of a Gate Drive Transformer

4.1 Duty Cycle Limitation

The most important consideration for gate drive transformers is saturation. The average voltage across the transformer must be 0, or the average current in the primary loop can increase until the transformer saturates. When the transformer saturates, the gate drive signal can be distorted and cease to function as intended.

The requirement for the average voltage across the transformer to be 0 imposes a limitation on this push-pull topology; the duty cycle of the half-bridge must be nearly symmetrical. There is some flexibility because the primary resistance dissipates excess DC current due to duty cycle offsets, but large duty ratios can cause saturation unless circuitry is added. This duty limitation makes gate drive transformer circuits less attractive for duty-controlled topologies such as buck converters. However, phase-controlled topologies such as phase-shifted-full-bridges (PSFB) and frequency-controlled topologies such as LLCs can still operate within the symmetrical duty limitation.

A DC blocking capacitor on the primary with a corresponding DC restore circuit on the secondary side enables driving of duty-controlled topologies. However, the DC restore circuit requires extra design and components to achieve. See section 7.1 in *Fundamentals of MOSFET and IGBT Gate Driver Circuits* for more information about the DC restoration circuit. Because alternate designs are available, gate drive transformers are more common in topologies which work well with symmetrical duty cycles such as LLCs and PSFBs.

4.2 Transients and Noise

Another consideration for gate drive transformers is transients on the gate driver IC. There are multiple factors that can make gate driver transformer topologies more stressful on the gate driver IC. One factor is the EMI generated by the transformer. The magnetic field generated by the transformer can couple into different traces on the PCB. This coupling can cause ringing on pins such as the input or enable pins which do not usually experience much ringing. This is one reason why gate drivers such as UCC27624 are designed to tolerate negative voltages and the input and output pins. Negative transient tolerance in the gate driver IC can reduce the need for external clamp diodes and save on system cost and size.

Another factor is the capacitive coupling to the high-voltage switch node. Push-pull type transformers tend to have relatively high inter-winding capacitance compared to LLC transformers. The inter-winding capacitance allows current to couple from the switch node to the primary. This current can also cause ringing and transients on the gate drive IC, which can lead to damage in some cases. This factor is why some designers use two primary-side resistors, as the resistors protect the gate driver IC from the injected current on both OUTA and OUTB, rather than just one.

4.3 Calculations

Pulse transformer selection is based on two main requirements; the minimum volt-seconds (VS) and voltage drop (droop). The volt-seconds specification is related to the saturation of the transformer. Voltage drop on the primary is relevant because the drop can result in increased conduction losses in the power stage.

The VS is the product between the voltage across the transformer primary, and the duration of that voltage. Because we are applying a square wave to the primary, this is easy to calculate. The area under the curve of the square wave applied to the transformer is given by Equation 1. To make sure the transformer never saturates, the VS must be calculated to account for the worst-case condition.

$$VS = V_{DD} \times t_{on} \tag{1}$$

Droop is the gate voltage loss due to magnetizing current. This voltage drop is given by Ohm's law, so we need to find the magnetizing current and the resistance. Magnetizing current is the current from the transformer primary inductance. When a voltage is applied across the primary of the transformer, a current builds according to the following equation:.

$$V = L \times \frac{di}{dt} \tag{2}$$

The magnetizing current is one component of the total current in the primary. The other current components are the gate drive current, and the current into the base of the PNP.

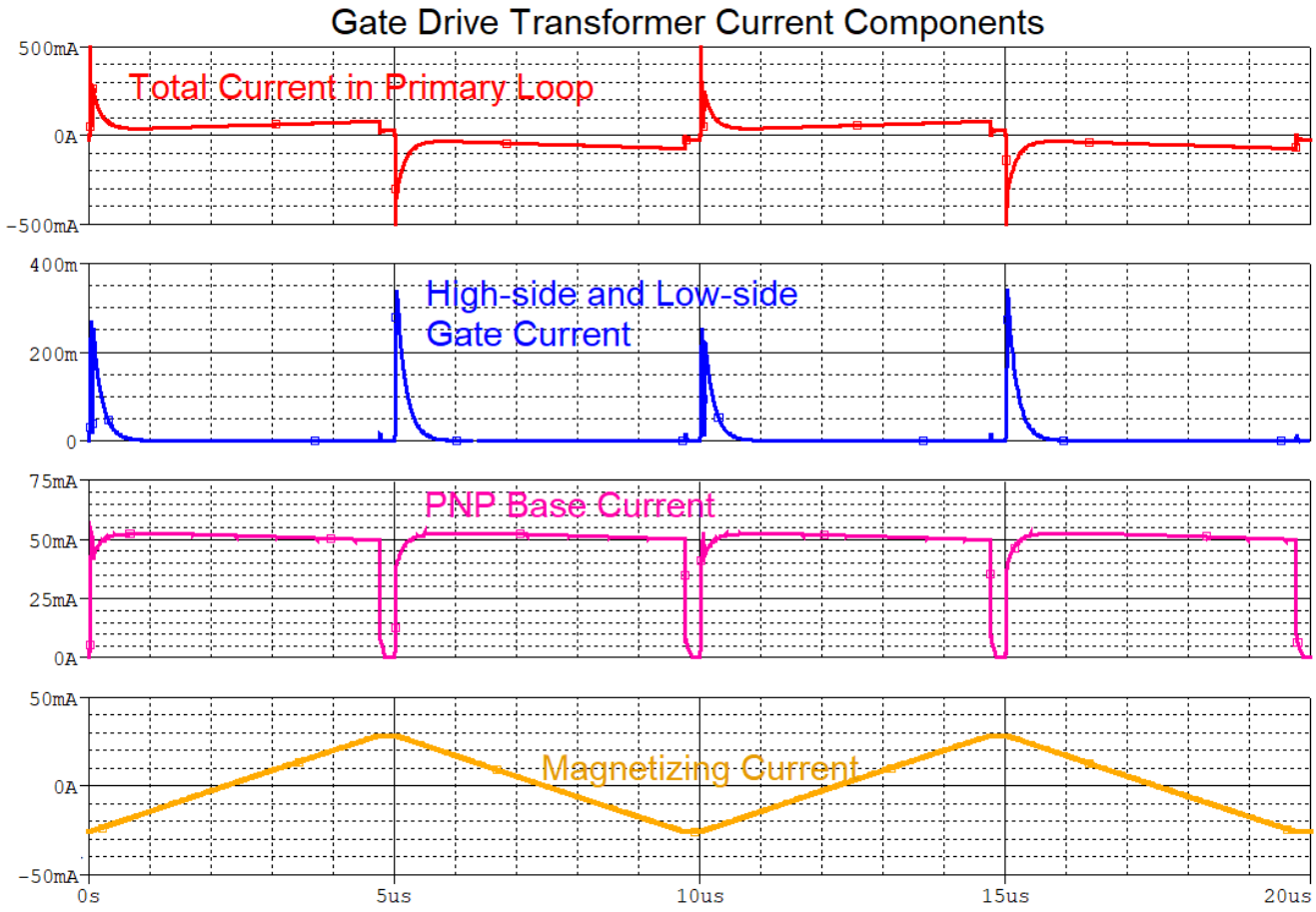

Figure 4-1. Simulation Showing the Major Current Components in the Gate Drive Circuit

In Figure 4-1, the total current appears very similar to the gate drive current, because that is the largest component. However, there is still a magnetizing current circulating through the primary. Using Equation 2, we can calculate this current. By re-arranging the terms we find:

$$\Delta I = \frac{V_{DD}}{L_{mag}} \times t_{on} \tag{3}$$

The current across the primary rises and falls by ΔI as the polarity of V_{PRIME} alternates. This current is centered around 0, so the peak current is given by:

$$I_{peak} = \frac{\Delta I}{2} \tag{4}$$

As dead-time approaches 0, the magnetizing current becomes a triangle wave centered around 0V. The root-mean-square (rms) of a triangle wave is given by:

$$I_{rms} = \frac{I_{peak}}{\sqrt{3}} \tag{5}$$

By substituting all of these terms, we can build an equation for the rms of the magnetizing current:

$$I_{rms} = \frac{V_{DD} \times t_{on}}{L_{mag} \times 2 \times \sqrt{3}} \tag{6}$$

The droop is given by the following equation:

$$V_{droop} = I_{peak} \times R_{primary} \quad (7)$$

By substituting the Ipeak equation from before we find that:

$$V_{droop} = \frac{V_{DD}}{2 \times L_{mag}} \times t_{on} \times R_{primary} \quad (8)$$

Designers often target a droop of less than 5%. This can also be written in terms of V_{DROOP} and V_{DD}:

$$\frac{V_{droop}}{V_{DD}} \leq \frac{1}{20} \quad (9)$$

By substituting this into the equation for V_{DROOP}, the simplified equation becomes:

$$L_{mag} \geq 10 \times t_{on} \times R_{primary} \quad (10)$$

By meeting this condition, the droop is kept under 5%. In this case, $R_{PRIMARY}$ is the sum of all resistances in the primary loop. The main components of $R_{PRIMARY}$ are as follows:

$$R_{primary} = R_{OH} + R_{OL} + R_{loop} + R_{primary} \quad (11)$$

When the driver is in the push-pull configuration, the current flows through the pullup of one output and the pull-down of the other output. See Figure 2-1 for an illustration that shows this effect. In addition to the resistance of the output stage, any additional resistance from discrete resistors and the transformer primary coil resistance adds to the total resistance.

4.4 Power Loss Calculations

The equations for power losses in gate driver data sheets are in terms of capacitive loads. In the case of a pulse transformer circuit, the load is inductive and these equations do not apply.

$$P = V_{DD} \times Q_g \times F_{sw} \quad (12)$$

The usual power loss equation for capacitive loads takes the charge added and removed from the gate in a switching cycle (Q_g), and multiplies by the switching frequency (F_{sw}). This multiplication gives the average current from the charging and discharging of the gate. By multiplying the average current by the VDD, the power loss due to switching is given. This equation is per FET, so the number is doubled in a dual channel driver or half-bridge driver.

Even with the transformer coupling, this charge-based method still works to estimate power dissipation. Assuming a lossless transformer, we can divide our initial equation by a factor of two to remove the pull-down (as that is dissipated by the local PNP pull-down). Additionally, we can add the DC leakage of the PNP during the off time. To demonstrate the PNP DC current, here is the same circuit as Figure 2-4 with a 100Ω base resistor.

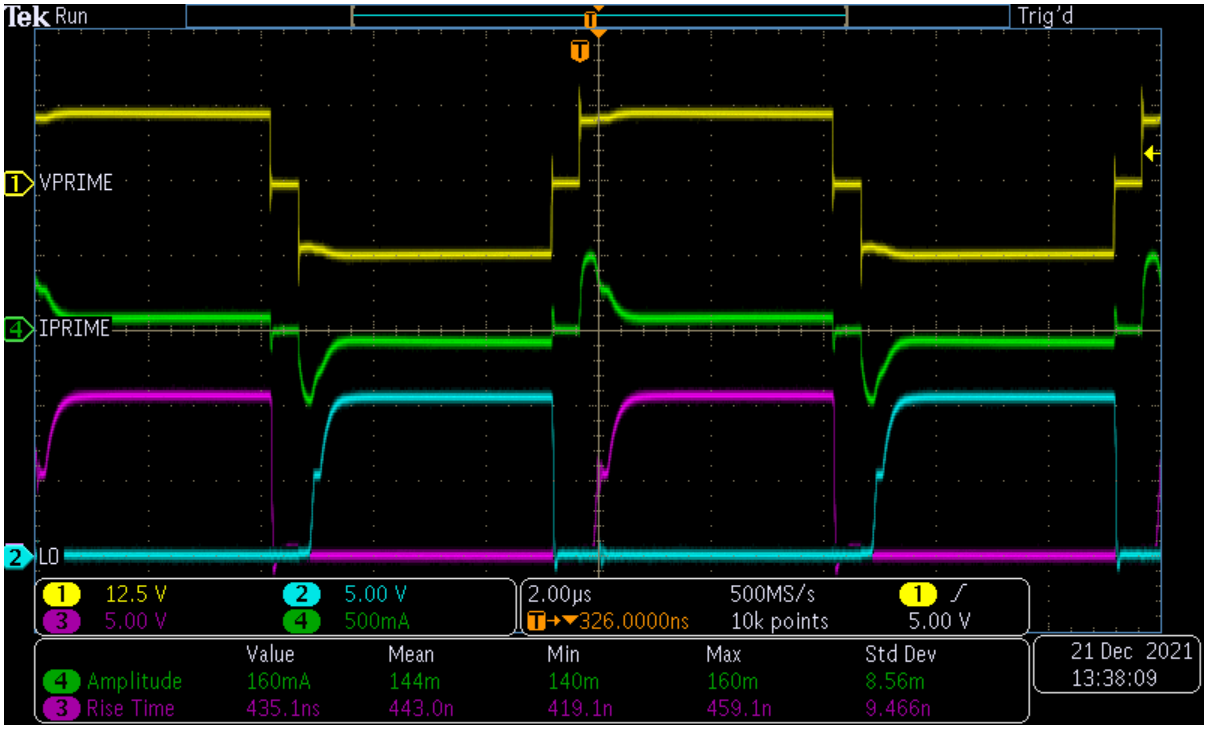

Figure 4-2. Oscilloscope Capture of Gate Drive Transformer Waveforms With 100Ω R_B

With this R_B change, the leakage current becomes more noticeable than in Figure 2-4. Notice how I_{prime} does not return to 0A, but stays closer to 100mA. The current in the primary loop is offset by a DC current caused by the PNP. The offset current can be calculated as following:

$$I_B = \frac{V_{DD} - V_{BE}}{R_B} \tag{13}$$

DC current sourced by the driver during a high output state is the worst-case for this driver due to the hybrid pullup structure. This is because the higher resistance PMOS must source this current. By adding the PNP base current, and RMS magnetizing current into our power dissipation equation, we get the following equation:

$$Ptotal = P_{SW} + P_{DC} + P_{MAG} \tag{14}$$

$$P_{SW} = \frac{V_{DD} \times Q_g \times F_{sw} \times 2}{2} \tag{15}$$

$$P_{DC} = {I_B}^2 \times R_{driver} \tag{16}$$

$$Ptotal = V_{DD} \times Q_g \times F_{sw} + (Roh + Rol) \times \left[\left(\frac{V_{DD} - V_{BE}}{R_B} \right)^2 + \left(\frac{V_{DD} \times t_{on}}{L_{mag} \times 2 \times \sqrt{3}} \right)^2 \right] \tag{17}$$

The numbers can be multiplied to account for transformers with different turns ratios. This equation also demonstrates an important factor in the selection of the PNP. PNPs with high gains are preferable because high gain allows a stronger pull-down (fewer switching losses) with a larger R_B. With R_B values greater than 1kΩ, the leakage can be negligible.

4.5 Bias Supply Thermal Calculation

Another common use for gate drive transformers is gate drive bias generation. By connecting a full-bridge rectifier on the secondary side, a gate drive transformer can be used to generate a floating DC voltage. This floating bias can be used to power isolated gate drivers.

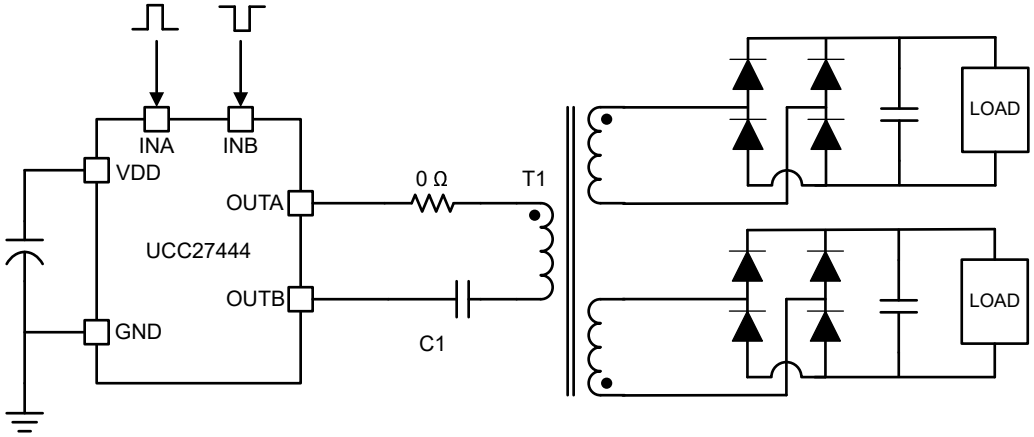

Figure 4-3. Example Schematic of a Push-Pull Bias Supply Using the UCC27444 Gate Driver IC

Gate driver ICs are designed to drive the gates of power switches, which is a capacitive load. In a bias supply, the gate driver is providing power to a bias supply, which is a mostly resistive load for the gate driver IC. Because of this difference in loads, the power dissipation equations in the gate driver IC data sheets do not apply to bias supply circuits.

Calculating the power dissipation in this application is straightforward. Assuming a 1:1 turns ratio, the load current from the bias supply appears as a DC current in the gate drive IC. Therefore, we can use the following equation as an estimate:

$$P = {I_{load}}^2 \times (R_{oh} + R_{ol}) \tag{18}$$

To improve the accuracy of the equation, we can add the RMS current due to magnetizing current in the primary:

$$P = (R_{oh} + R_{ol}) \times \left[{I_{load}}^2 + \left(\frac{V_{DD} \times t_{on}}{L_{mag} \times 2 \times \sqrt{3}} \right)^2 \right] \tag{19}$$

As an example, suppose that instead of driving a half-bridge as shown in Figure 2-3, we instead used the same setup to generate two 12V, 3W bias supplies. Neglecting magnetizing current, we can estimate the power dissipation as shown:

$$P = \left(\frac{3W}{12V} \times 2 \right)^2 \times (5 + 0.6) = 1.4W \tag{20}$$

This estimate uses the typical values for R_{oh} and R_{ol} from the UCC27624 data sheet, and ignores the magnetizing current factor because magnetizing current is determined largely by the transformer. In this case, we can expect to dissipate about 1.4W in the driver output stage. Multiplying by $R_{\theta JA}$ to get a rough estimate of heating, we can expect the D package to self-heat significantly, as the $R_{\theta JA}$ is 126.4ºC/W. The DGN package, which has a much lower $R_{\theta JA}$ of 48.9ºC/W, self-heats less. Thermal performance also depends on other parameters such as board layout and copper thickness, but $R_{\theta JA}$ is designed for package to package comparisons in the same condition.

Another option can be to use a driver such as UCC27444. The UCC27444 driver uses a PMOS only pullup structure. The PMOS only structure results in a lower R_{oh} to DC current compared to the hybrid structure driver UCC27624. The typical R_{oh} of UCC27444 is about 1.2Ω. By re-calculating Equation 20 with the UCC27444 parameters, we can expect to dissipate about 0.475W. In this case, UCC27444 is estimated to dissipate about one-third of the amount of power UCC27624 dissipates.

5 Summary

Even after the invention of high-voltage and isolated gate drivers, there are still applications where a gate drive transformer paired with a non-isolated driver is a competitive option. Push-pull gate drive transformers offer various benefits in applications which work well within the duty cycle limitation of the transformer. Particularly, gate drive transformers are useful in LLC converters and PSFB converters. Gate drive transformers can be used to eliminate a bias supply, provide negative gate drive bias, and flexibility by taking advantage of the transformer turns ratio. In addition, gate drive transformers can be used to generate bias supplies for isolated gate driver ICs and other ICs. With all of these potential advantages, gate drive transformers still have a place in many systems.

6 References

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- Texas Instruments, *Designing an LLC Resonant Half-Bridge Power Converter*.
- Texas Instruments, *UCC27624 30-V, 5-A, Dual-Channel, Low-Side Gate Driver with –10-V Input Capability*, data sheet.
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