Application Report

How to Bridge LVDS/OLDI to HDMI/DVI

Ikechukwu Anyiam

ABSTRACT

This document provides an overview of how to connect an LVDS (Low Voltage Differential Signaling), OLDI (OpenLDI) or RGB source to an HDMI (High-Definition Multimedia Interface) or DVI (Digital Visual Interface) panel or display. The two-chip solution receives 4 LVDS data pairs and a clock, and output 3 TMDS (Transition Minimized Differential Signaling) pairs and a clock.

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Trademarks

1 Introduction

For parallel RGB to DVI/HDMI, the TFP410 by itself can be used. The TFP410 is a DVI compliant bridge/ transmitter that converts up to 24 bits of parallel RGB data to DVI. DVI is equivalent to HDMI without audio, so this device can also be used to convert to HDMI if the application does not require audio.

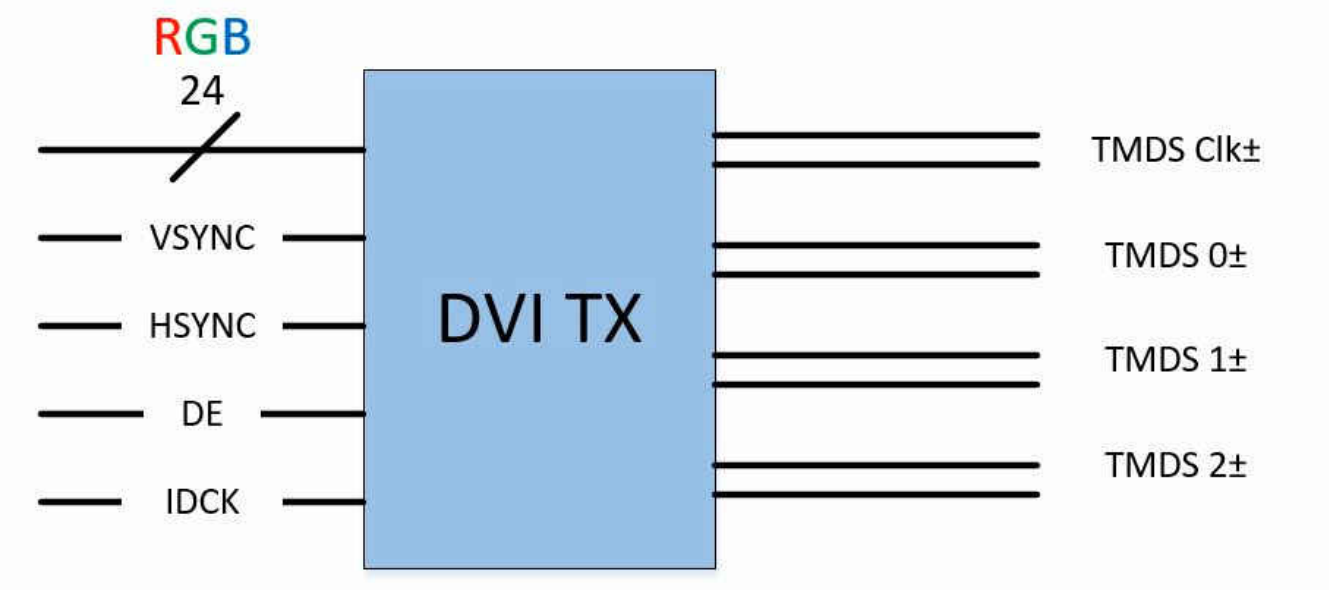

Figure 1-1. RGB to DVI/HDMI Conversion

For LVDS to DVI/HDMI, an intermittent LVDS receiver (also known as a deserializer) is needed. The LVDS deserializer will synchronously deserialize 4 LVDS data pairs carrying 7 bits of data each (including HSYNC, VSYNC, and DE) into 24 bits of parallel RGB data. This output is compatible with the TFP410's input, so the TFP410 can then be used to convert the parallel RGB input to a DVI/HDMI output.

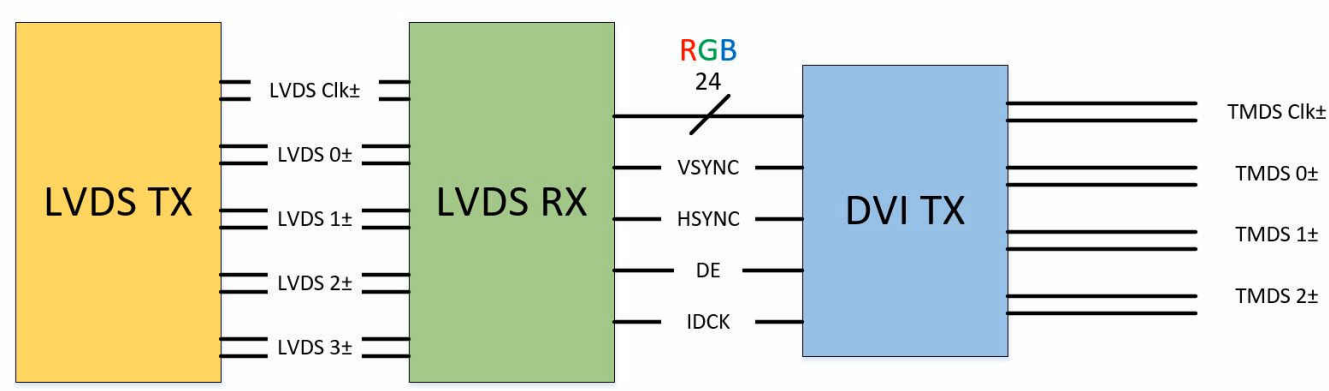

Figure 1-2. LVDS to HDMI Conversion

2 Design Considerations

The TFP410 supports pixel clock frequencies in the range of 25 MHz to 165 MHz. However, most LVDS deserializers do not support a frequency range this wide. If your application is LVDS to HDMI, you should ensure that the LVDS deserializer and the TFP401 both support the frequency for the desired resolution.

The table below provides some options for LVDS deserializers for LVDS to HDMI conversion:

Table 2-1. LVDS Deserializer Conversion Options

Part Name	Color Depth	Frequency Range [MHz]	Clock Edge
DS90CR218A	18bpp (RGB666)	12 - 85	Rising
DS90CF366	18bpp (RGB666)	20 - 85	Falling
DS90CR288A	24bpp (RGB888)	20 - 85	Rising
DS90CF386	24bpp (RGB888)	20 - 85	Falling
DS90CR486	24bpp (RGB888)	66 - 133	Rising
DS90CR484A	24bpp (RGB888)	33 - 112	Rising
DS90CF388	24bpp (RGB888)	40 - 112	Rising

3 Design Guidelines

1. Set the same clock edge for the LVDS deserializer and the TFP410. For example, if using the DS90CR218A, the *EDGE* pin on the TFP410 should be pulled high so that data is latched on the rising edge for both devices. If used with the DS90CF386, *EDGE* should be pulled low for falling edge latching.
2. Length match all data and control signals between devices.
3. The incoming TMDS data must be DVI-compliant, and not contain HDMI island data (audio) or deep color (more than 24 color bits).

4 References

- Texas Instruments, How to Bridge HDMI/DVI to LVDS/OLDI application report.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265